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Enhanced Self Checking Carry Select Adder using Dynamic Logic Based Full Adder

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Abstract: ***Fast adders are constructed mainly by Carry select adders (CSLA). Area is one of the main concerns as far as any VLSI design is considered. In connection this paper enhances the performance of self checking carry select adder by introducing un footed dynamic logic based full adder cell instead of a regular CMOS based adders. The adder is constructed with 10 transistors based on the optimization of truth tale of a full adder. A 3 transistor X-NOR gate circuit is also used instead of a conventional X-NOR circuit in the self checking path. Adders of size 4 bit and 8 bit are constructed in various technologies. The results show that the proposed structure reduces the transistor over head by almost 47% and 46% for 4bit and 8bit structures respectively. By achieving this much of reduction in area this work could be suggested for higher order VLSI structures like BIST,DCT etc.,***

Keywords: Full adder, CSLA, self checking, dynamic logic.

I. INTRODUCTION

Mathematic manipulations are daily utilized almost by many digital systems [1]. The implementation of quicker, more precise and area efficient adders are of high concern in those systems. Self checking facility had been included and a new scheme to encode the addition bits using two rail codes is proposed [2]. Each one of the adders which have been designed over the years has different trade-offs as shown in [3]. Two terms namely defect tolerance and layout modifications had been discussed for better yield enhancement [4].An easy design is carried in ripple carry adder (RCA), but with increased carry propagation delay. A traditional carry select adder (CSLA) is constructed by two pairs of RCA that produces a couple of outputs namely sum and carry. Final sum and carry will be selected by the applications of actual input carry (C_{in}= 0 or 1) along with a multiplexer arrangement [5]. Many CSLA adders have been proposed [6-10]. Reduced area was the main constraint of [6]. RCA & one add-one circuit has been proposed in [7]. They proposed a square-root CSLA to implement large bit-width adders with less delay. A binary to BEC based CSLA was suggested by Ramkumar & kittur [8]. But drawback is its high delay. Sharing the common Boolean logic term based CSLA has been proposed [9-10]. It has been usual for many of the authors to include reliabilities in terms of getting fault free addition where transient faults are of high important. As the consequence of down scaling in transistor dimensions transients faults have been growing. Self-checking is the solution to these systems transient faults. Adders along with self-analyzed unit based on arithmetic residue codes were proposed by authors of [11-12]. The problem behind these adders are complexity created by checkers and the overhead is too high [13-14]. Some more self-checking CSLA adders have been proposed. Authors failed to detect errors in the carry path [14]. Many error detecting techniques were discussed in and a novel parity based fault tolerant arithmetic logic unit has been proposed in [15-16]. One more technique for an online testable CSLA by 4 bit self analyzing CSLAs as building blocks were also proposed [17]. Here again satisfactory results were not met and it was also not having self checking multiplexers and de-multiplexers. This paper proposes a modification to the circuits that were used by [1-2] using dynamic logic instead of a regular CMOS logic. It uses only ten transistors for constructing the full adder section. It also introduces a three transistor X-NOR circuit which will replace the existing X-NOR circuit. No changes have been made to two pair two rail checker, which has been used by [1-2]. Our work is organized as follows. Section 2 presents the faulty design [1] & corrected design of self checking CSLA by [2]. Section 3 illustrates the proposed and modified design of self checking CSLA using dynamic logic. Section 4 gives the simulation environment and comparison of the implemented design with the existing works and the work is completed in section 5.

II. PREVIOUS WORKS

Faulty CSLA design is depicted in Fig.1 [1]. In that authors proposed a CSLA design based on two-rail encoding [1]. They designed a 2 bit CSLA that detects all one error faults online. They replaced the conventional CSLA structure by introducing self checking multiplexers and two-pair two rail checker (TTRC). With this inclusion they claimed that, their design was totally self checking. But authors showed and proved that it does not work for CSLA with input bits higher than 2 [2].

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To overcome the difficulty, they [2] modified the structure given by [1] by introducing an AND logic (ref. Fig.2). This change in design has given the correct indication of fault at the output of TTRC not only for 2 bit CSLA design but also for n-bit CSLA. Here we furnished the work done by [1] and how it was modified by [2] in detail.

By looking at the table 1 & 2 it is seen that leaving the LSB's (S00, S01), the sum bits calculated when carry-in(Cin) equals 0 (S20,S10) will be opposite to the corresponding sum bits with carry-in equals to 1(S21,S11) only when all the lower sum bits are equal to 1 (i.e. S20=S10=1). If it fails (i.e. if any of the sum bits say S20 (or) S10 =0) then the sum bits calculated will not be complementary to each other. In other words the sum bits calculated when Cin=0 will be equal to the sum bits calculated when Cin=1(leaving the LSB's).The transistor overhead achieved by is ranging from 19.51% to 20.94% [1].In [2], authors gave a modified design solution for the fault which they found in [1]. Author [2] introduced an AND logic structure in addition to the design structure given by [1] to calculate the product terms$S^0_{(n-1)} \times S^0_{(n-2)} \times \ldots . S^0_2 \times S^0_1$.

This evaluation is later used to calculate the input to the two pair two rail checker (TTRC) which then analyze the complementary nature of the inputs which it receives. If TTRC fails to receive proper inputs from its predecessor as is the case of [1], then it ends with wrong fault indication. This has been correctly pointed out and solution was also given by the examples [2]. Fig.2. presents the modified and corrected design of self-testing CSLA with two rail encoding. The authors have achieved 23.2% to 34.5% in transistor overhead as mentioned [2]. Table 3 lists the comparison of the transistor counts given by [1] and [2].

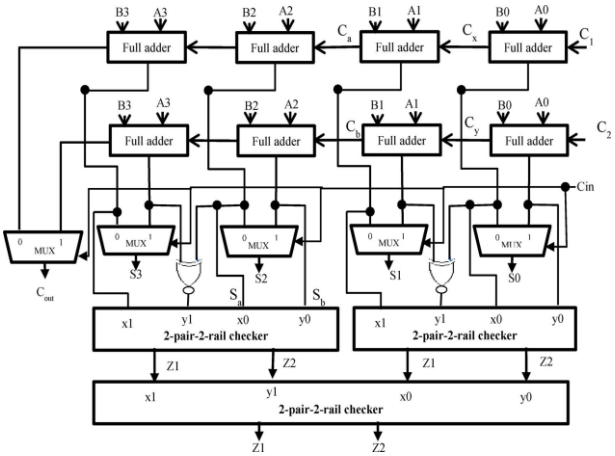

Fig. 1. Faulty CSLA design [1].

Table 1. Addition of two 3 bit numbers with Cin=0 and Cin=1(Example 1)

	A+B(With C_{in}=0)			A+B(With Cin=1)		
Bit Position (i)	***MSB*** 2	1	***LSB*** 0	***MSB*** 2	1	***LSB*** 0
Binary number(A)	0	0	1	0	0	1
Binary number(B)	0	0	1	0	0	1
Sum (S)	0 S20	1 S10	0 S00	0 S21	1 S11	1 S01

Table 2. Addition of two 3 bit numbers with C_{in}=0 and C_{in}=1(Example 2)

	A+B(With Cin=0)			A+B(With Cin=1)		
Bit Position (i)	***MSB*** 2	1	***LSB*** 0	***MSB*** 2	1	***LSB*** 0
Binary number(A)	0	0	1	0	0	1
Binary number(B)	1	1	0	1	1	0
Sum (S)	1 S20	1 S10	1 S00	0 S21	0 S21	0 S21

Table 3. Comparison of transistor counts from [1] & [2]

Number of bits	Vasudevan et al. faulty design [1]	Corrected self-checking CSLA [2]
4	328	350
8	652	718

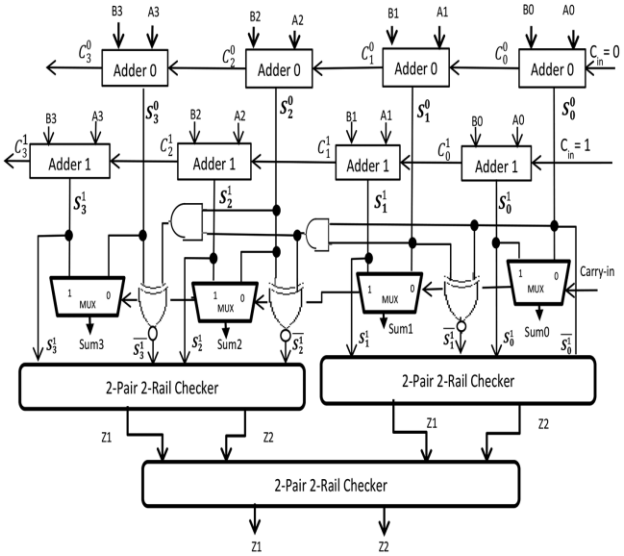

Fig. 2. Corrected CSLA design [2].

III. PROPOSED AND MODIFIED SELF CHECKING CIRCUIT

Still enhancement is required in [2] in terms of transistor count, as the count is almost increasing exponentially with respect to the number of bits. To overcome that issue we propose a novel 1 bit full adder using un-footed dynamic logic structures. This new full adder consists of only ten transistors to calculate both sum and carry which are 18 transistors less than that of the structure used by [2]. Author [2] used CMOS logic style for XNOR section which is replaced by as by a novel three transistor structure.

In the proposed CSLA design novel 10 transistor (T) structure has been incorporated, modified XNOR circuit is introduced and finally based on these changes a novel self checking CSLA in dynamic logic has been presented.

A. Modified 1 bit adder circuit

Based on the full adder truth table a new equation (1) is derived for C_{out} and the Sum expression (2) is not altered. The equations are,

$$C_{out} = \bar{Y} * C_{in} + Y * A \qquad (1)$$

Where $Y = A \odot B$

$$Sum = (A \odot B) \odot C \qquad (2)$$

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With respect to the expression a new eight transistor one bit full adder circuit is constructed. To make it faster, an un-footed dynamic structure has been incorporated in the structure.

The structure is given along its truth table which has been functionally verified in DSCH 2.6 and it is shown in Fig.3 and Table 4 respectively. Table 5 presents the functionality verification of C_{out} expression of the proposed full adder circuit. The capacitance of high impedance nodes are used to store the signal values in dynamic logic circuits. It requires $(n+1)$ N type transistors and one P type transistor (where n is the number of N type transistors used to construct the function).

Dynamic gates follow two work phases namely pre charge and evaluate. Logic function is implemented by bottom N network only. The top P network will take care of charging and discharging the dynamic node. By keep this in mind this paper proposes a new full adder with dynamic logic which will only require ten transistors$(8 * T + 2 * T = 10 * T)$.

This reduction in number of transistor ultimately reduce more switching action, reduce load capacitance due to lower input capacitance, smaller output loading and less short circuit current (I_{SC}) since all the current provided by pull down network goes in to discharging load capacitor (C_L). This ensures faster switching speeds. One more advantage is that full swing outputs are guaranteed.

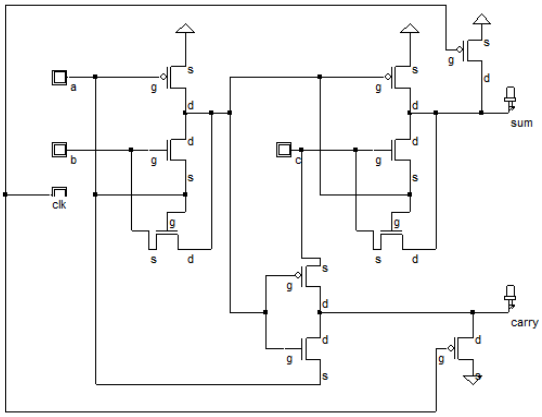


Fig. 3. Ten transistor full adder circuit

Table 4
Ten transistor full adder truth table

A	B	C	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 5
Verification of C_{out} expression for the proposed the full adder

A	B	C	$Y = A \odot B$	$\bar{Y}$	$\bar{Y} \times C_{in}$	$Y \times A$	C_{out}
0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	0
0	1	1	0	1	1	0	1
1	0	0	0	1	0	0	0
1	0	1	0	1	1	0	1
1	1	0	1	0	0	1	1
1	1	1	1	0	0	1	1

B. Modified XNOR circuit

Many authors have proposed variety of XOR-XNOR circuits over the recent past. Some of them are 4T self checking differential XOR, CMOS based XOR-XNOR circuit. By having speed in mind, in this paper we used a 3T XNOR gate which will replace the existing XOR-XNOR circuit. Fig. 4. Illustrates 3T XNOR circuit.

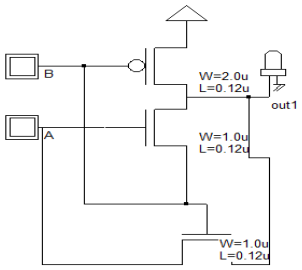


Fig. 4. Three transistor XNOR circuit.

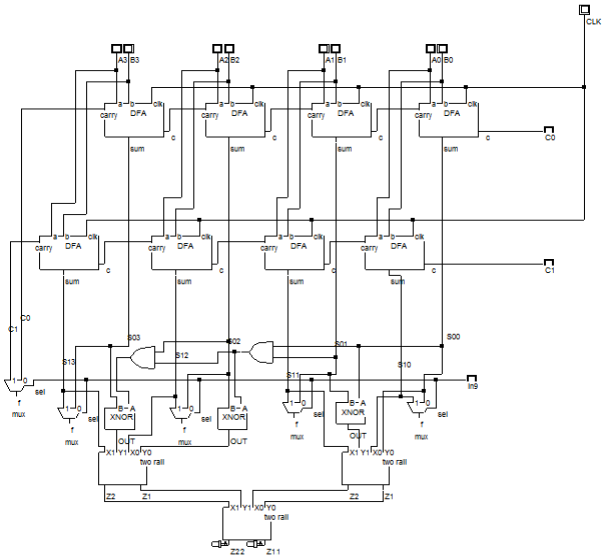


Fig. 5. 4bit Dynamic self checking CSLA.

C. Proposed and modified circuit of self checking CSLA in dynamic logic

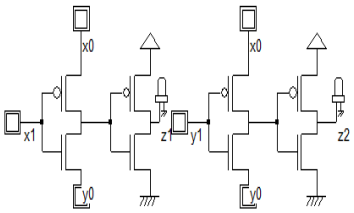
Four bit and eight bit self checking dynamic CSLAs are constructed in 120nm, 90nm, 70nm and 50 nm technologies. All authors were aiming to show the transistor overhead [1-2 & 16]. Our main aim is to project the response of these adders with respect to the various technologies apart from showing the transistor overhead comparison. The advantages of our circuits are, they are dynamic and so offer faster response, they are totally self checking which provide fault tolerance and finally they used dual rail at the final stage their by offer full swing voltage between maximum and minimum. Fig.5. illustrates the 4bit dynamic self checking CSLA.

Fig.6. Illustrates the two pair two rail checker which is taken from [18]. The pairs $(X1, Y1)$ & $(X0, Y0)$ are the inputs derived from the two rows (i.e.$C_{in=0\ row}$ & $C_{in=1\ row}$) are then applied to the inputs of TTRC. ($Z1, Z2$) are the outputs of the TTRC.

1	1	0	1	0	0	1	1
1	1	1	1	0	0	1	1

For a fault free circuit Z1 is complementary to z2(i.e. $Z1 = \overline{z2}$).At any faulty situation of the circuit, our proposed circuit indicates that through the status of the outputs which is verified by DSCH tool.

Fig.7. illustrates the 8 bit dynamic self checking CSLA circuit. It is constructed by appending one 4bit dynamic self checking CSLA with another 4bit structure. Here the six outputs are (from out1 to out6) used to analyze the self checking property of the adder with the help of three two pair two rail checker results (i.e. two outputs per 4bit dynamic self checking CSLA and finally those four outputs are compared in the final checker to yield the last two outputs).



Z1	*Z2*	Condition of the circuit
0	1	Good
1	0	Good
0	0	Fault detected
1	1	Fault detected

Fig. 6. TTRC with its truth table.

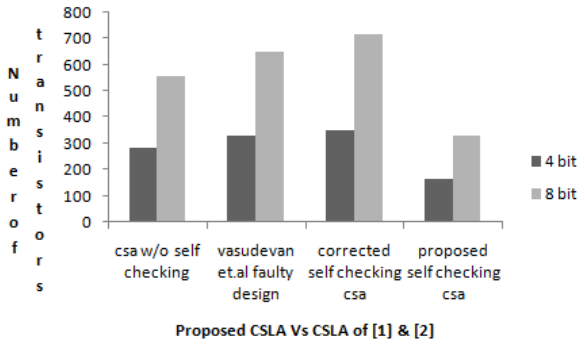


Fig. 8. Transistor overhead comparison.

IV. RESULTS AND COMPARISONS

Delay, frequency and power are calculated with respect to 120nm, 90nm, 70nm and 50nm technologies. The circuit schematic is drawn using DCSH front end and the analysis are made using MICRO WIND back end tool. Various parameters are derived and are listed in the table 6. As usual the transistor count also taken in to account for comparison like the other authors did. The count is calculated for a 4 bit design as given below:

- Dynamic full adder-80 transistors;
- AND gate-12 transistors;
- XNOR gate-9 transistors;
- MUX- 60 transistors;
- TTRC-24 transistors. (Totally 185 transistors per 4 bit CSLA design).

Fig.8 gives the detailed statistics of transistor count

Table 6 Circuit parameter comparison

Parameter	120nm Technology		90nm Technology		70nm Technology		50nm Technology	
Number of Bits	4	8	4	8	4	8	4	8
Area in µm	4060	13794	2873	9396	3534	11490	1392	4541
Output Voltage	1.19	0.49	1	0.43	0.99	0.29	0.50	0.22
Power in mW	2.153	3.3227*10 -3	1.063	2.319*10 -3	2.648	2.278*10 -3	0.202	0.326*10 -3
Delay in pS	62	6000	90	6000	72	6000	359	6000
Frequency in MHz	60	360	140	200	160	70	370	70

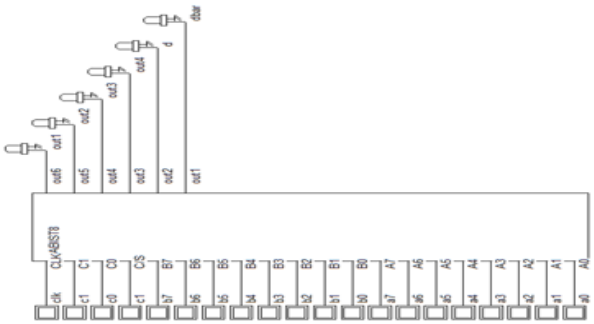


Fig. 7. Eight bit dynamic self checking CSLA.

V. CONCLUSIONS

A 4bit and 8bit self checking CSLA using dynamic logic were constructed. It is verified through simulation results that the proposed design perform well for higher bit structures too. Area has been drastically reduced since our work used 10T full adder and modified XNOR to construct the structure. It is clearly mentioned in Table 6. But one of the drawbacks is, as bit count increases final output voltage attained reduces. It is also visible in the output voltage row of Table 6. The functionality of the structures is working well since we used self checked built-in adder circuits. This is also confirmed by referring Table 5. From table 6 it is seen that for a 4 bit structure the delay is very less compared to 8 bit. Almost constant delay is experienced by the structure even if the technology is scaled down. Our expectation is to reduce the count and their by avoiding frequent switching of transistors to yield low power design. From Fig.8 it is seen that the transistor over head is almost reduced to 50% with respect to the previous work. But we could not compare the power results what we have got with the previous work as they only mentioned the transistor overhead [1-2]. In future work, we will apply our concept of self checking dynamic logic based adder to construct more complicated circuits such as fast self-testing adders and multipliers and later it can be embedded in application circuits like Built in self test (BIST) can be expected.

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