

Optimised Design and Implementation of Band-Pass Filter for Neural Recording System

A.I. Al-Shueli



Abstract: In this paper, an eight order efficient digital infinite impulse response filter is designed to improve the signal to noise ratio (SNR) and minimise the hardware and power consumption. For this task, an optimisation method has been adapted to reduce the root mean square error and hardware usage. The filter has been designed and analysed using Matlab and Modelsim, the implementation has been synthesis on Xilinx Spartan 3E-100 (xc3s100e) field-programmable gate array board. Moreover, an optimisation process using parallel algorithm has been adapted for further reduction in the hardware area and power consumption. The results show the Band Pass Filter effectively functions in real time recording application with significant improvement in the SNR which could achieve high-velocity selective resolution. The present work offers a structure of implementing a band-pass filter on FPGAs using a nonlinear digital filter shows a significant saving of 25.4% in power consumption and 29.9% of the hardware size comparing with the latest algorithm of IIR filter design. Consequently, this is an essential development to enhance the neural signals to be adopted as reference or control signals in artificial limbs devices.

Keywords: Biomedical signal processing, DSP, FPGA, IIR digital filter.

I. INTRODUCTION

The possibility of controlling neuroprostheses with artificial or biological signals has long fascinated humans and this has driven the advance of the application area of functional electrical stimulation (FES) and artificial prostheses [1-3]. The quality of electroneurogram (ENG) signal is very important for neural activity recordings using multi-electrode cuffs (MECs)[4-7]. The MECs method can increase the SNR for the recorded signals. Typically, with electrode cuff interface technology the recorded APs are within the range from 1 - 5 μ V peak to peak in a band from about 1 Hz – 3 kHz [8] and SNR in a range from 1.2 to 3.8 dB [9]. The idea of velocity selective recording (VSR) method revolves around MEC and the nerve signal transmits through the tripolar electrode cuff, which gives the same reaction at the outputs of amplifiers, time delay layout throw depends on the distance between two electrodes divided by the velocity (T, 2T, 3T. NT).

as a result of T is subject to the velocity, the propagation velocity extracted proportional to the artificial time delays match ($N\tau...3\tau, 2\tau, \tau$) (matched velocity) [4]. The amplitude and SNR are affected by many factors such as amplifier gain, the amplifier configuration (eg. unipolar, monopolar or tripolar) and filter performance.

A digital processor employed in digital filter design to implement arithmetic computational on signal sampled values. In addition, the general purpose of digital processor is computer chip design and costume DSP (Digital Signal Processor) chip [10]. The most common advantages of the DSP system such as speed, cost and flexibility are executed through DSP algorithms or using Application Specific Integrated Circuits (ASIC) which offer high speed but they are less flexible and high cost. An alternative method is to employ Field Programmable Gate Arrays (FPGA) because they combined the features of both techniques the DSP and ASIC. Further, the FPGA boards are reprogrammable and reconfigurable devices and easily change to implement diverse functionality if in demand. Consequently, the proposal IIR filter configured using FPGA board. However, the main challenge in IIR filters design is their sensitivity to coefficient quantization that means instabilities in the filter functionality highly possible. Subsequently, they are implemented using cascades or parallel structure based on second order sections, which is called biquads. The poles and zeros group in each biquad optimised to calculate the minimum filter order required for the biquad sub-filters is the key of the IIR configurations.

The opportunities for pipelining and computational latency the main limitation in the design proposed in [11, 12] due to the inner feedback of the repetitive IIR filters. Many studies are presented an optimisations design approach such as dispersed look ahead [13, 14], clustered look ahead [14, 15] and distributed look ahead [16, 17]. All these methods increased the operating frequency using superfluous poles allowing pipelining [18, 19]. Though, towards limitation on scale factors and noise effect, these design approaches need intensive computational time the adequate set for zeros and poles and proper order for the sub-filters. This computation work is required in advance to realise the actual filter. On the other hand, some research works based on optimal design is offered to minimize the consumed computational time, however, the attempt still limited [13–20].

Most of the latest studies [21-24] seek to reduce the filter size by reduction of the set delay deviation. However, the minimizing of filter size only does not fully use for expenses reduction in the physical configuration on ASIC FPGA platforms.

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Moreover, reduction of filter size may lead for longer coefficient size and that cause unwanted hardware increment and dramatic reduction in the SNR.

The current study offers computation time reduction using the parallelism feature of the FPGA without affecting the system complexity.

The current filter implemented in a parallel approach due to the FPGA resource which contains a large number of gates and millions of transistors. In this work, a low power and hardware architecture propose for design IIR band pass filter. The goal of this work is to provide an IIR filter design based on FPGA for ENG signal recording. The system design tools used in this work include a personal computer, Xilinx Integrated Software Environment (ISE) Suite 14.2, Matlab 2010, Modelsim De 6.5e Software and Xilinx Spartan 3E-100 (xc3s100e) FPGA board. The IIR filter coefficients calculated using the fixed-point method in MATLAB Toolbox and then transfer them to embedded design on FPGA to filter ENG signal. The main benefit of this technique is to reduce process time using FPGA parallel

processing ability and minimise the hardware size and power usage. Further, the objective design has been tested and ran on FPGA platform using artificially generated nerve signals already designed by the previous study [25].

II. MATERIALS AND METHODS

A. System Description

Figure 1 illustrates the overall design component for the complete system which is consist from four units. The first unit on the left side is an eleven-channel artificial action potential (AP) generator which is designed and described in [25], to produce the input to the amplifiers and ADC unit previously designed in [26]. The ADC unit produce ten digitised signals and provided to the bipolar channels and handled on an FPGA board using ANN classification method in unit 3 [27-29]. The proposal IIR digital BPF in unit four is used in this study to improve the SNR and enhance the APs distinguish and classification.

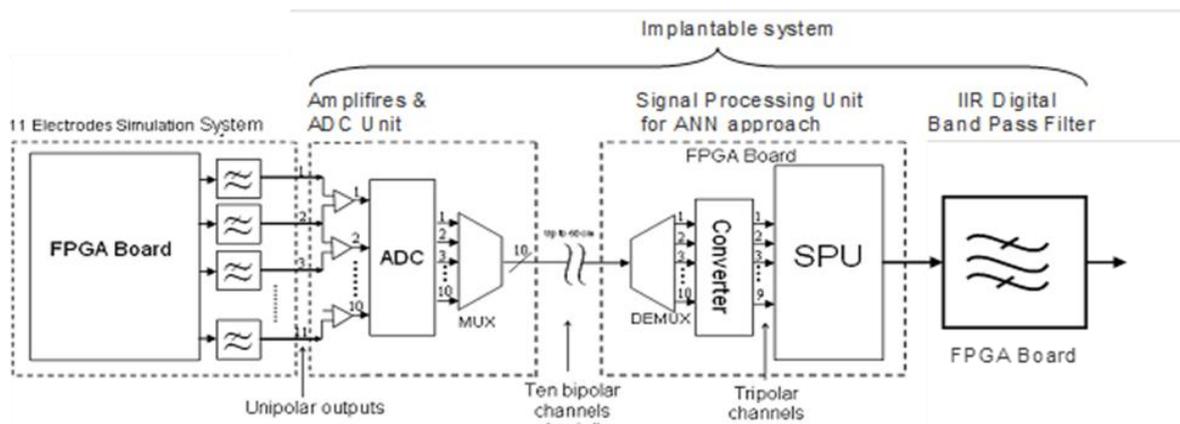


Fig. 1. The block diagram plan of the complete system [26].

B. Algorithm of Filter Design

The overall plan of the design procedure shown in figure 2 [30] which is consists of the steps flowed in this study, the first step is to design the digital BPF with filter design toolbox using Matlab. A 2nd order 4 stages direct form II configuration used for implement infinite impulse response (IIR) Butterworth BPF filter correspond with each matched velocity.

The matched velocities were chosen at these velocities (10, 20, 30...100 m/s) and the centre frequency for BPF filter for each matched velocity shown in Table I[29].

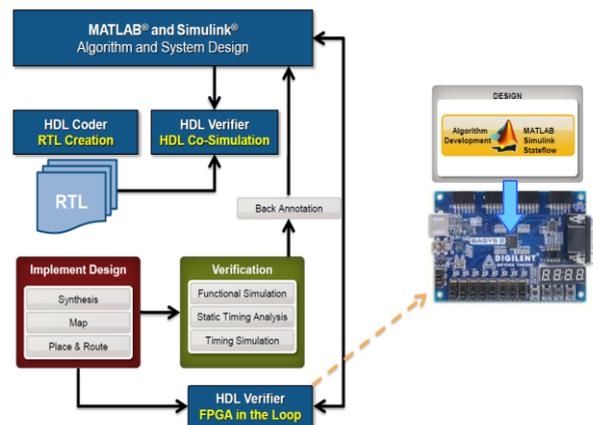


Fig. 1. Model-Based Design flow using MATLAB/Simulink from Algorithm to FPGA Implementation

Table I. The centre frequencies (f_o) for each matched velocity.

Matched velocity (m/s)	10	20	30	40	50	60	70	80	90	100
f _o (kHz)	0.9	1.6	2.4	3.2	4	4.8	5.6	6.4	7.2	8

C. Filter Design

There are different strategies available for digital filter design and implementation. A low power consumption and low hardware design approach is selected because of it suitable for our application. Moreover, the target filter offers a good requirement performance and low complexity in hardware. The direct form-II structure shown in figure 2 is chosen for implementation IIR filter because its advantages compare with other filter structure. The main benefit for this structure, it needs less memory storage for the data samples [31]. Moreover, saving hardware leads for less size and low power consumption. Furthermore, the IIR filters need fewer coefficients as a result of usage feedback and poles, consequently, the IIR filter computationally more efficient than FIR filter [32].

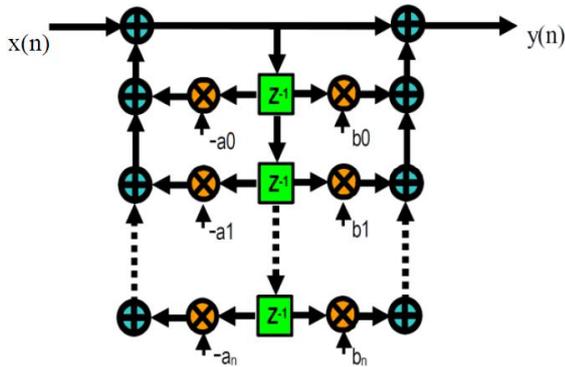


Fig. 3. The direct form-II structure [30].

The generalised equations of IIR filter are:

$$H(z) = \frac{\sum_{i=0}^n b_i z^{-i}}{\sum_{i=0}^m a_i z^{-i}} \quad (1)$$

$$y(n) = \sum_{i=0}^n b_{(i)} x(n-i) + \sum_{i=0}^m a_{(i)} y(n-i) \quad (2)$$

Where H(z) is the filter transfer function, ai and bi are the filter coefficients, x(n) is the discrete input signal and y(n) is the discrete output signal.

The digital IIR Butterworth filter coefficients can be calculated using the digital filter design toolbox with sampling frequency 32500Hz, and centre frequency as shown in Table I for each conduction velocity, and converted using fixed_point arithmetic. The calculation requires an optimisation for the word and fraction length to minimise the hardware requirement. A 16 bit was chosen for word length and 15 bit for fraction length as shown in Table II. Meanwhile, an 8 order direct form-II structure filter is used to optimise the filter performance and characteristics. Several tests and examination carried out to verify the design, such as stability and, time response as shown in figure 3, figure 4 and figure 5.

The 8th order IIR filter implemented is a band pass filter with the specifications shown in Table II.

Table II. Filter constants for conduction velocity 20 m/s

Filter Constants	Values
f _L	1550 Hz
f _H	1650 Hz
f _c	1600 Hz
Nominal Gain	1
Nominal Ripple	0.01
Maximum Ripple	0.0089
Ripple in dB	0.077
Sampling Frequency = 32.5 kHz	

The BPF is designed using a digital filter design toolbox. The filter design tool generates filter constants of the structure shown in Table II. Table II illustrates the filter coefficients that are achieved for the above BPF specification.

Table III. Filter coefficients and gains

Section Number	Quantized Numerator	Quantized Denominator	Quantized Gain
Section 1	b ₀ 1	a ₀ 1	0.0096306800842285156
	b ₁ 0	a ₁ -1.89239501953125	
	b ₂ 1	a ₂ 0.992431640625	
Section 2	b ₀ 1	a ₀ 1	0.0096306800842285156
	b ₁ 0	a ₁ -1.90362548828125	
	b ₂ 1	a ₂ 0.99285888671875	
Section 3	b ₀ 1	a ₀ 1	0.0095810890197753906
	b ₁ 0	a ₁ -1.8858642578125	
	b ₂ 1	a ₂ 0.98211669921875	
Section 4	b ₀ 1	a ₀ 1	0.0095810890197753906
	b ₁ 0	a ₁ -1.89068603515625	
	b ₂ 1	a ₂ 0.98248291015625	

The impulse response analysing is used to evaluate the sample 8th order band pass IIR filter by feeding an impulse signal as input to the filter. A large quantity (7F00h) input is applied to the filter on the first input sample. The analysis was done using Matlab and Modelsim SE 10.1c software. Figure 4, Figure 5 and Figure 6 show the plots of the impulse response, Pole/Zero and the frequency response respectively. While Figure 7 and Figure 8 demonstrate results of the step and Chirp response for the IIR BPF output respectively using ModelSim simulation software.

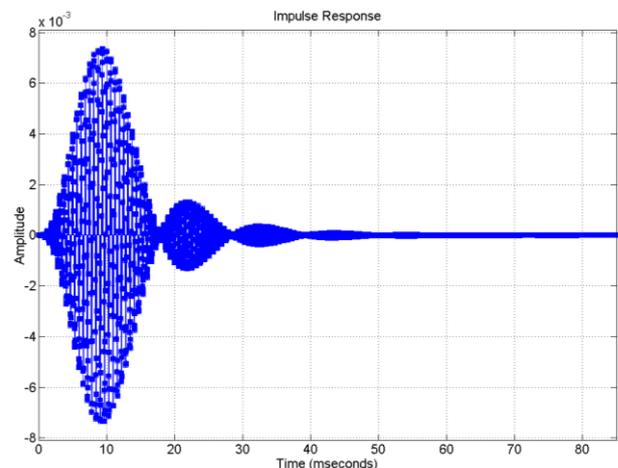


Fig. 2. Filter impulse response plot.

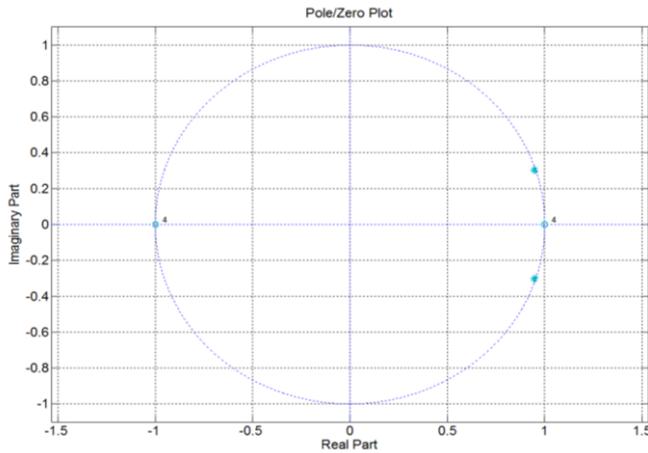


Fig. 5: Pole/Zero plot

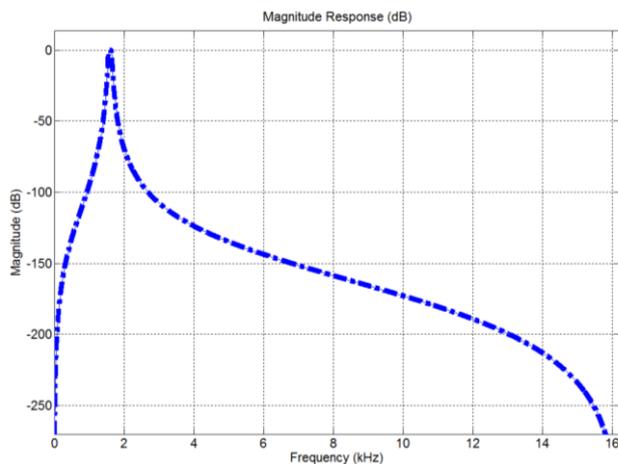


Fig. 3. Frequency response

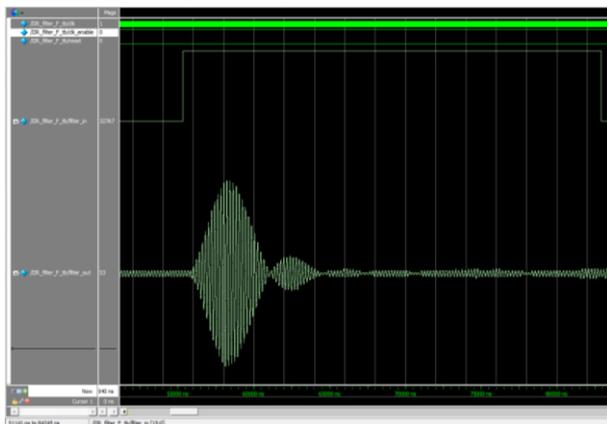


Fig. 4. Filter step response using Modelsim.

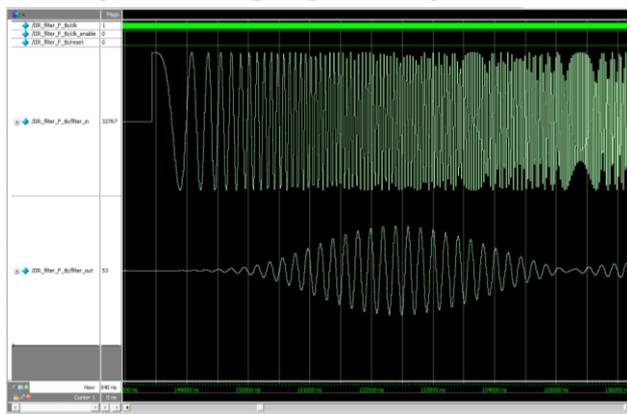


Fig 5. Filter chirp response using Modelsim

$$d(n) = x(n) + d(n-1).a_0 + d(n-2).a_1 \tag{3}$$

$$y(n) = d(n).b_0 + d(n-1).b_1 + d(n-2).b_2 \tag{4}$$

D. Implementation of IIR Filter Using Xilinx.

The Direct Form II structure is demonstrated in Figure 9 and time domain difference equation is presented in eqn. (3) and (4)[30].

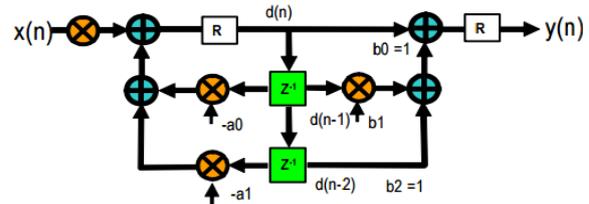


Fig. 6. Direct Form II Structure

The parallel structure using biquads is used as shown in Figure 10. This structure has been utilised by processors. The equation for the parallel form is shown in eqn (5)[30].

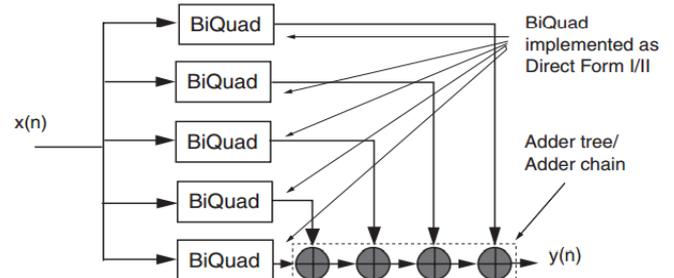


Fig. 7. Parallel BiQuad Structure.

$$H(z) = K + \sum_i^N \left(\frac{c_{i0}Z^{-1} + c_{i1}Z^{-2}}{1 + a_{i0}Z^{-1} + a_{i1}Z^{-2}} \right) \tag{5}$$

The filter structure is illustrated in Figure 10, with the biquads in parallel. The input storage has been used in parallel biquad for the forward filter. Thus, optimisation implemented and adopted in this work to minimise the hardware size.

A real time signal is captured from the output of ANN signal processing unit and filtered using BPF. The filter is implemented on Xilinx Spartan 3E-100 (xc3s100e) FPGA using Verilog HDL language with a personal computer as shown in fig 9. The input signal is converted into a 16-bit data. The hexadecimal multiplication addition and subtraction are done in Verilog HDL using Xilinx ISE Design Suite 14.2. An optimisation implementation is used to reduce the multiplication, addition and subtraction. The optimum design using parallel processing used to capture real time signal.

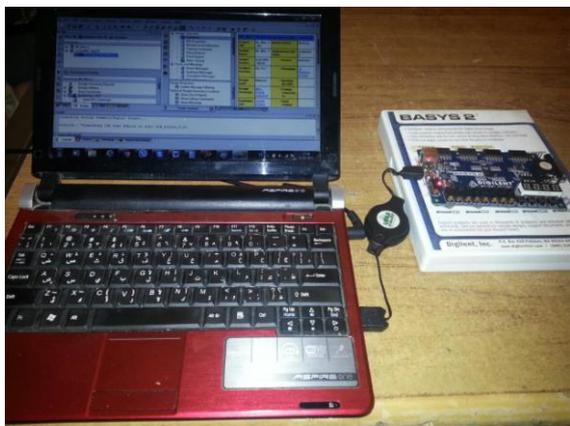


Fig. 8. Implementation of IIR Filter Using Xilinx Spartan 3E and Xilinx Integrated Software Environment (ISE) Suite 14.2.

III. RESULTS

The blocks were written in Verilog HDL using the Xilinx software was used for design entry, synthesis, and simulation. The current design consumed nearly 30% of the resources present in the xc3s100e Xilinx chip as shown in Table IV.

Moreover, more effort is spent for further minimising the FPGA resource usage by using different implementation approach to reducing the number of multipliers and accumulators usage via advanced optimisation techniques. The proposed parallel structure for the IIR filter significantly saved the hardware size and computation time compares with the serial structure for IIR filter and conventional FIR filter structure as demonstrated in Table IV.

Table IV: Device Utilization Summary

Logic Utilization	Parallel structure of IIR		Serial structure of IIR		Conventional structure of FIR		Available
	Used	Utilization	Used	Utilization	Used	Utilization	
Number of Slices	301	3%	369	4%	879	10%	8677
Number of Slice Flip Flops	122	0%	158	0%	159	0%	17344
Number of 4 input LUTs	528	3%	630	3%	1675	9%	17344
Number of bonded IOBs	23	9%	35	14%	35	14%	250
Number of Mult18X18SIOs	12	42%	12	42%	16	57%	28
Number of GCLKs	1	4%	1	45	1	4%	24

The proposed IIR design implementation shows a significant saving of 25.4% in power consumption and 29.9% of the hardware size comparing with the newest algorithm of IIR filter design. Moreover, from the logic synthesis results, the suggested group delay deviation of our approach is on average 15.5% lower, in comparison with other algorithms, as detailed here, the average savings in hardware size and power consumption is 17.5% and 13.4%, respectively.

This is an interesting point in hardware size and complexity reduction. In addition, the SNR across all channels recordings increased by a factor 23% compare with system without PBF.

There are significant differences among digital filters in performance term which is clearly presented on the selected IIR filter design in this study compare with other structures

such as FIR. Moreover, the SNR is improved significantly which could lead for the high accurate selectivity of ENG recordings. Consequently, this is an important improvement to enhance the neural signals to be used as reference or control signals in artificial limbs devices.

IV. CONCLUSIONS

This study proposes an optimum IIR BPS filter to improve the VSR method based on ANN for ENG neural activity classification system. The proposed design successfully works in online neural recording system without missing the velocity selective accuracy which is suggested for it. In this study, an IIR BPF structure implementation based on FPGAs has been suggested. The results show the nonlinear IIR filter could minimise the hardware size by 45% compare with linear Filter (FIR).

The IIR filter implemented using optimised process computation and synthesis on FPGA board using a parallel algorithm to minimize the hardware size and power consumption. As result, The IIR filters are more accurate to implement than FIR filters to satisfy the filter specifications such as passband, stopband filters. In addition, the IIR filter could offer computational time saving due to their implementation structure, which is represent a significant factor in design strategy. The main challenge in these filters design is stability because the output is essentially dependent on frequency domain instead of time domain. However, IIR filters more efficient than FIR because they require less computational time and hardware size as they need fewer coefficients as a result of the utilisation of poles and feedback.

REFERENCES

1. W. F. Agnew, D. B. McCreery, T. G. Yuen, and L. A. Bullara, "Histologic and physiologic evaluation of electrically stimulated peripheral nerve: considerations for the selection of parameters," *Annals of biomedical engineering*, vol. 17, no. 1, pp. 39–60, Jan. 1989.
2. Z. M. Nikolić, D. B. Popović, R. B. Stein, and Z. Kenwell, "Instrumentation for ENG and EMG recordings in FES systems," *IEEE transactions on biomedical engineering*, vol. 41, no. 7, pp. 703–6, Jul. 1994.
3. J. K. Chapin and K. A. Moxon, *Neural Prostheses for Restoration of Sensory and Motor Function: Neuroscience*, 2001.
4. W. Z. Hoffer, J. A., Marks, W. B., and Rymer, "Nerve fiber activity during normal movements," *Soc. Neurosci. Abstr.*, p. 300, 1974.
5. R. B. Stein, D. Charles, L. Davis, J. Jhamandas, A. Mannard, and R.T. Nichols, "Principles underlying new methods for chronic neural recording," *The Canadian Journal of Neurological Sciences. Le Journal Canadien des Sciences Neurologiques*, vol. 2, no. 3, pp. 235–244, 1975.
6. J. Erlanger and H. Gasser, "The comparative physiological characteristics of nerve fibres," in *Electrical Signs of Nervous Activity*. Philadelphia, PA: Univ. Pennsylvania Press, pp. 34–78, 1937.
7. J. A. Hoffer, *Techniques to study spinal cord peripheral nerve and muscle activity in freely moving animals*, in "Nuromethods: Neurophysiological techniques: applications to neural systems, 15th ed., A. A. Boulton, G. B. Baker, and C. H. Vanderwolf, Eds. 1990.
8. R. Carpenter, *Neurophysiology*. London: Edward Arnold, 1984.
9. S. Raspopovic, J. Carpaneto, E. Udina, X. Navarro, and S. Micera, "On the identification of sensory information from mixed nerves by using single channel cuff electrodes," *Journal of neuroengineering and rehabilitation*, vol. 7, p. 17, Jan. 2010.
10. C. Ruggiero, *Segnali Biomedical*. Laboratorio MedInfo.

11. K. Parhi: "Pipelined VLSI recursive filter architectures using scattered look-ahead and decomposition". *Proc. Int. Conf. of Acoustics, Speech, and Signal Processing, ICASSP-88*, April 1988, pp. 2120–2123.
12. K. Parhi, D. G. Messerschmitt: "Pipeline Interleaving and parallelism in recursive digital filters part I: pipelining using scattered look-ahead and decomposition", *IEEE Trans. Acoust. Speech Signal Process.*, 1989, 37, (7), pp. 1099–1117
13. Y.C Lim, B Liu: "Pipelined recursive filter with minimum order augmentation", *IEEE Trans. Signal Process.*, 1992, 40, (7), pp. 1643–1651
14. K.C. Chang, J. Kim: "Pipelined recursive digital filters: clustered look-ahead and scattered look-ahead techniques". *Proc. Int. Symp. on Circuits and Systems, ISCAS 94*, 1994, pp. 89–92
15. M. Soderstrand, A. E. de la Serna, H. H Loomis: "New approach to clustered look-ahead pipelined IIR digital filters", *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 1995, 42, (4), pp. 269–273
16. Y.C. Lim: "A new approach for deriving scattered coefficients of pipelined IIR filters", *IEEE Trans. Signal Process.*, 1995, 43, (10), pp. 2405–2406
17. A.K. Shaw, M. Imtiaz: "A general look-ahead algorithm for pipelining IIR filters". *Proc. Int. Symp. on Circuits and Systems, ISCAS 96*, 1996, vol. 2, pp. 237–240
18. R. Kaur, A. Raman, H. Singh, J. Malhotra: "Design and implementation of high speed IIR and FIR filter using pipelining", *Int. J. Comput. Theory Eng.*, 2011, 3, (2), pp. 292–295
19. S. Samanta, M. Chakraborty: "FPGA based implementation of high speed tunable notch filter using pipelining and unfolding". *20th National Conf. on Communications, NCC*, 2014, pp. 1–6
20. Y.L. Chen, C.Y. Chen, K.Y. Jeng, A.Y. Wu: "A universal look-ahead algorithm for pipelining IIR filters". *Proc. IEEE Int. Symp. on VLSI Design, Automation and Test, VLSI-DAT*, 2008, pp. 259–262.
21. G. Deng, J. Chen, J. Zhang and C. Chang, "Area- and Power-Efficient Nearly-Linear Phase Response IIR Filter by Iterative Convex Optimization," in *IEEE Access*, vol. 7, pp. 22952-22965, 2019.
22. X. Lai and Z. Lin, "Iterative reweighted minimax phase error designs of IIR digital filters with nearly linear phases," *IEEE Trans. Signal Process.*, vol. 64, no. 9, pp. 2416_2428, May 2016.
23. J. Li, G. Deng, W. Wei, H. Wang and Z. Ming, "Design of a Real-Time ECG Filter for Portable Mobile Medical Systems," in *IEEE Access*, vol. 5, pp.696-704,2017.
24. Y. Chen, X. Zhang, Y. Lian, R. Manohar and Y. Tsvividis, "A Continuous-Time Digital IIR Filter With Signal-Derived Timing and Fully Agile Power Consumption," in *IEEE Journal of Solid-State Circuits*, vol.53, no.2, pp.418-430, Feb 2018.
25. Al-Shueli, C. T. Clarke, and J. T. Taylor, "Simulated Nerve Signal Generation for Multi-electrode Cuff System Testing," in *International Conference on Biomedical Engineering and Biotechnology*, 2012, pp. 892–896.
26. T. Clarke, X. Xu, R. Rieger, J. Taylor, and N. Donaldson, "An implanted system for multi-site nerve cuff-based ENG recording using velocity selectivity," *Analog Integrated Circuits and Signal Processing*, vol. 58, no. 2, pp. 91–104, Nov. 2008.
27. A.I. Al-Shueli, C.T. Clarke, N. Donaldson, and J.T. Taylor, "Improved Signal Processing Methods for Velocity Selective Neural Recording Using Multi-Electrode Cuffs," *Biomedical Circuits and Systems, IEEE Transactions on*, vol.8, no.3, pp.401,410, June 2014.
28. A.I. Al-Shueli, "Signal Processing for Advanced Neural Recording Systems," PhD Thesis, University of Bath, Bath, UK, 2013.
29. J. Taylor, N. Donaldson, and J. Winter, "Multiple-electrode nerve cuffs for low-velocity and velocity-selective neural recording," *Med Biol Eng Comput*, vol. 42, no. 5, pp. 634–643, 2004.
30. P. Kumar "Generating, Optimizing and Verifying HDL Code with MATLAB and Simulink", The MathWorks, Inc.
31. M. Francis, "Infinite Impulse Response Filter Structures in Xilinx FPGAs, www.xilinx.com " WP330 (v1.2) August 10, 2009.
32. S. M. Rabiul Islam, R. Sarker, S. Saha and A. F. M. Nokib Uddin, "Design of a programmable digital IIR filter based on FPGA," 2012 *International Conference on Informatics, Electronics & Vision (ICIEV)*, Dhaka, 2012, pp. 716-721.

resistivity, digital filter design, micro-electronic design, digital signal processing. Dr. Al-shueli is a member in IEEE organization, Iraq Section, as well as a member in the Iraqi Engineering Union.

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