Enhanced 32-Bit Adder Implementation using Different Configurations of Adders

L.S.P.Sairam Nadipalli, Sita K, G.Sai Sri Ram Reddy, R.Sudheer, M.Chaithanya

Abstract- Adders play a essential role with in the digital signal process systems. The 32-bit configuration is commonly used in few computerized systems and processors. In this paper, detail study about the implementation of 32-bit adders like Ripple Carry Adder (RCA), Carry Select adder (CSLA) and Carry Increment adder (CINA) is done for various configurational full adders using VHDL. The outcomes are acquired by executing VHDL in Xilinx ISE 14.5 with speed grade -5 of Spartan 3E family device.

Keywords— Ripple Carry Adder (RCA), Carry Select adder (CSLA), Carry Increment adder (CINA), Conventional Full Adder (FA), Configurational Full Adder 1 (FA1), Configurational Full Adder 2 (FA2), Configurational Full Adder 3 (FA3).

I. INTRODUCTION

Mostly in digital circuits, the arithmetic circuits are of high significance. An adder may be a circuit that implementing of addition of two numbers and gives sum and carry as results. For adders like half adder and full adder which add two and three inputs respectively. There are some ways to implement full adder which are efficient than conventional full adder.

Most of the digital systems like computers exists 32-bit architecture like 32-bit registers ,memory address ,integers. For improvement of 32-bit adders entire delay must be decreases so that increases in speed. Performance of various 32-bit adders like Ripple Carry Adder (RCA), Carry Select adder (CSLA) and Carry Increment adder (CINA) for different full adders is design and analyze in terms of look up tables(LUT), slices ,delay, fan-out using VHDL in Xilinx ISE 14.5 for the Spartan 3E family device with grade -5. This paper has 5 parts that is --- part I contains relating to introduction on the adder, part II deals with literature survey on full adder configurations, part III contains the design of 32-bit adders, part IV deals with the simulation results, part V has result analysis of RCA,CINA and CSLA for various full adder configurations, part VI has the conclusion about this work and references of thiswork are at the end of this paper.

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II. LITERATURESURVEY

A. Conventional Full Adder(FA):

The basic full adder circuit is obtained using two XOR gates, three AND gates and an OR gate. The Boolean expressions used are

- sum=a⊕b⊕cin (1)
- carry=(a·b)+(b·cin)+(cin·a) (2)

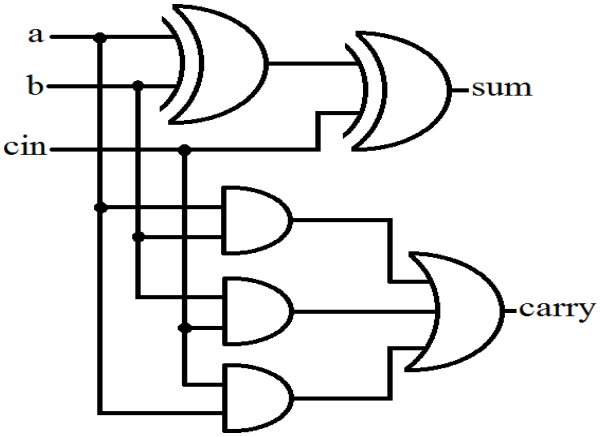

Fig.1 Conventional full adder (FA)

B. Configurational full adder- 1(FA1):

Wallace tree multiplier is done with both normal full adder and configurational full adder-1 and it is shown that configurational full adder-1 implementation occupies the less area.

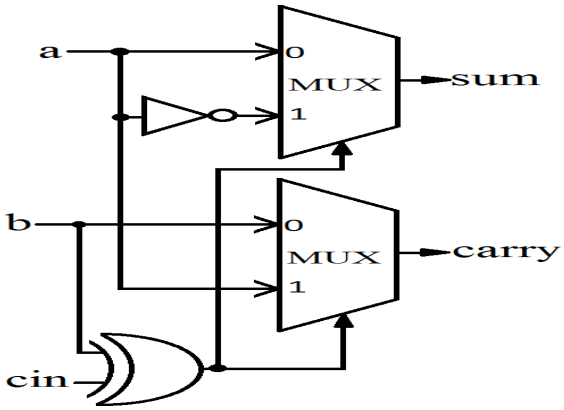

Fig.2 configurational full adder-1 (FA1)

C. Configurational full adder-2(FA2):

Configurational full adder-2 is handling gate level synchronous methods and it is shown that configurational full adder-2 implementation occupies the less area ,less number of gates and less power.

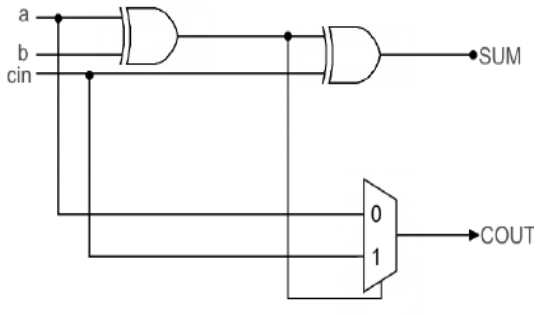

Fig.3 Configurational full adder-2 (FA2)

D. Configurational full adder-3(FA3):

It is also shown that the use of configurational full adder-3 performs better in terms of delay and area .

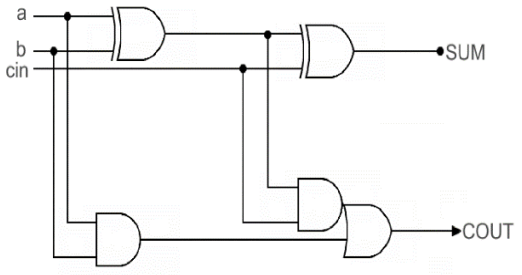

Fig.4 Configurational full adder-3 (FA3)

III. DESIGN OF 32-BITADDERS

A. Ripple Carry Adder(RCA):

Ripple Carry Adder is a logic circuit. It may contains individual full adders and also addition is propagated between the individual adders then carryout generated. Carryout from the previous full adder is carryin to current full adder then only computation of each adder result takes place. In this adder major disadvantage is propagation delays that are occur certainly. The design of the 32-bit RCA is shown in Fig.5.

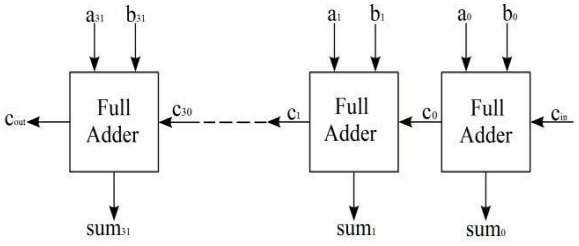

Fig.5 32-bit Ripple carry adder

B. Carry Increment Adder (CINA):

In carry increment adder, various RCA blocks are used to compute the results. The primary RCA block is given carry-in as input along with addends to get carry(c1) and sum. For the rest RCA blocks, the carry-in is given as logic '0' to get temporary sum (sum1) and temporary carry which are given to increment circuit. Increment circuit consists of half adders which add temporary sum and carries to get the actual sum(sum) and carry (cy). The carry-out of increment circuit is obtained by performing OR operation between carry (cy) and carry-out of the previous stage. As the between carry (cy) and carry-out of the previous stage. As the carry-in for the RCA stages is logic '0' and hence the carry propagation delay decreases. The design for the CINA 32bit is given in Fig.6.

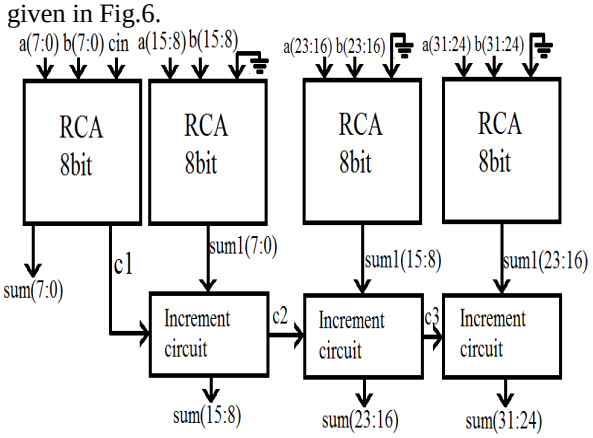

Fig.6 32-bit Carry increment adder

C. Carry Select Adder(CSLA):

A carry-select adder contain seven of these 4-bit ripple carry adder blocks and a single 4-bit ripple carry adder. For carry select adder carry-in(Cin) is given as input for first RCA block and also for the first four bits no carry select block is needed. Mux circuit contain four 2 to 1 multiplexers. Main mux of inputs of RCA blocks of Cin as 0 and 1 for seven 4 bit RCA blocks. The delay of this carry select adder will be eight RCA adder delays and thirty five MUX delays. The design for the 32bit CSLA is given in Fig.7.

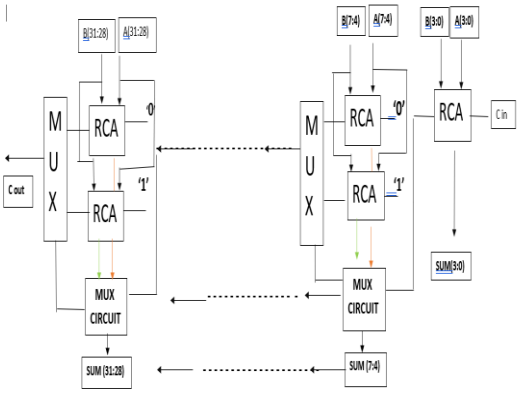

Fig.7 32-bit Carry select adder

IV. SIMULATIONRESULTS

A.Configurational Full Adders:

The RTL schematic diagrams of various configurational full adders are shown in Fig. 8,9,10,11 respectively.

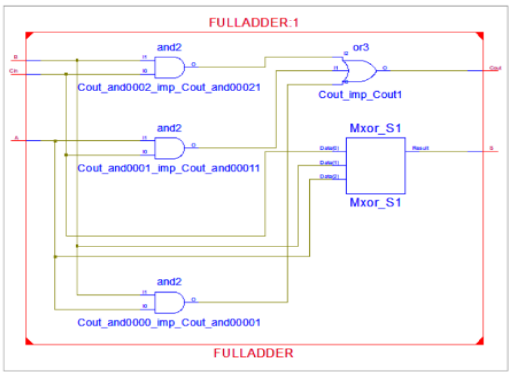

Fig.8 RTL schematic ofFA

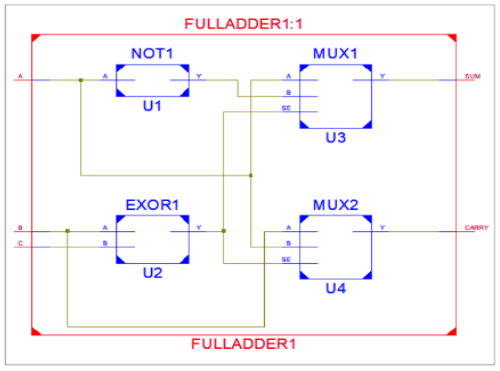

Fig.9 RTL schematic ofFA1

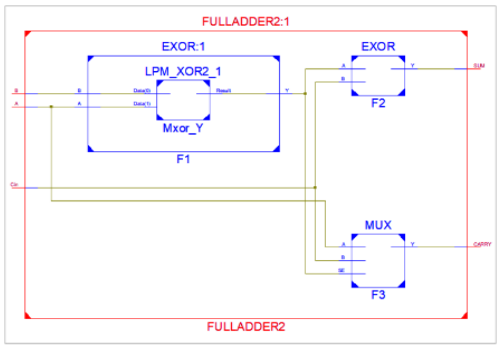

Fig.10 RTL schematic ofFA2

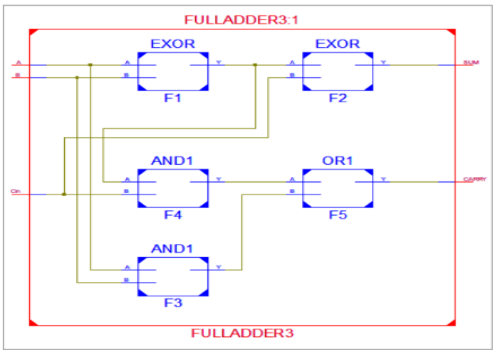

Fig.11 RTL schematic ofFA 3

A. Ripple carry adder (RCA):

The RTL simulation and schematic results for 32-bit RCA is shown in Fig.12 and 13 respectively.

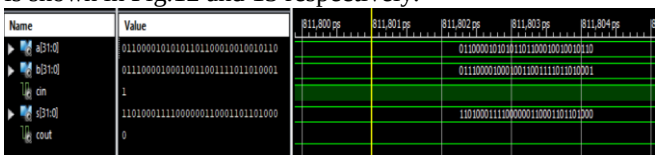

Fig.12 Simulation result of 32-bit RCA

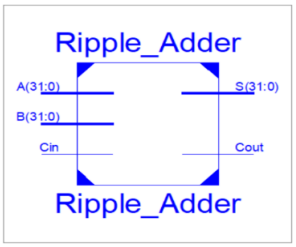

Fig.13 RTL Schematic of 32-bit RCA

B. Carry increment adder(CINA):

The RTL schematic and simulation results for 32bit CINA is shown in Fig.14 and 15 respectively.

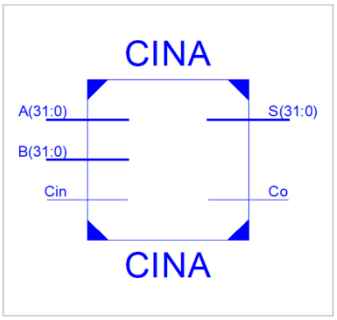

Fig.14 RTL schematic of 32-bitCINA.

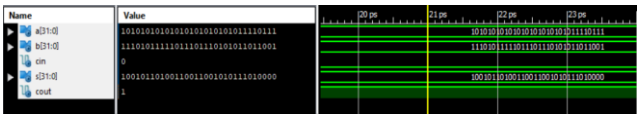

Fig.15 Simulation result of 32-bitCINA

C. Carry select Adder(CSLA):

The RTL schematic and simulation results for 32-bit CSLA is shown in Fig.16 and 17 respectively.

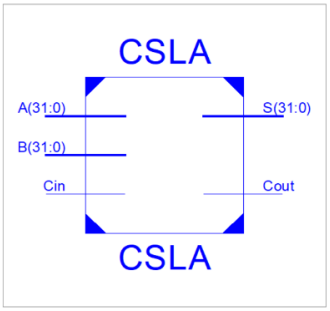

Fig.16 RTL schematic of 32-bit CSLA.

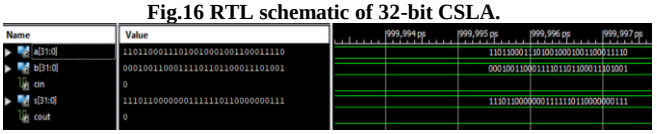

Fig.17 Simulation result of 32-bit CSLA

V. RESULTSANALYSIS

The implemented hardware RCA, CSLA and CINA are designed by using VHDL. These adders are simulated using various full adder configurations. Simulation is executed by using Xilinx ISE 14.5 for the Spartan-3E family device with a speed grade of -5.

Table 1 : Comparison for various 32-bit adders with FA

	LUTs	Slices	Delay(ns)	Fan-out
RCA (FA)	64	48	38.66	1.74
CINA (FA)	88	54	25.3	2.14
CSLA (FA)	85	48	24.1	2.68

Table 2 : Comparison for various32-bit adders withFA1

	LUTs	Slices	Delay(ns)	Fan-out
RCA (FA1)	64	48	38.6	1.74
CINA (FA1)	88	52	25.47	2.14
CSLA (FA1)	87	50	25.25	2.69

Table 3 : Comparison for various32-bit adders withFA2

	LUTs	Slices	Delay(ns)	Fan-out
RCA (FA2)	64	48	38.66	1.74
CINA (FA2)	88	54	25.35	2.14
CSLA (FA2)	85	48	24.1	2.68

Table4 : Comparison for various32-bit adders withFA3

	LUTs	Slices	Delay(ns)	Fan-out
RCA (FA3)	64	48	38.66	1.74
CINA (FA3)	90	54	25.25	2.14
CSLA (FA3)	85	48	24.1	2.68

From the above tables, various comparisons for adders are obtained and observed. The graphs comparing the LUTs, slices(area), delay and fan-out of 32-bit RCA,32-bit CINA and 32-bit CSLA circuits for different full adder configurations are shown in Figs.18, 19, 20, 21, 22, 23, 24 respectively.

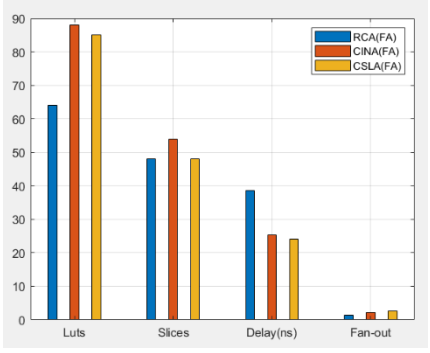

Fig.18 Comparison for adders using FA

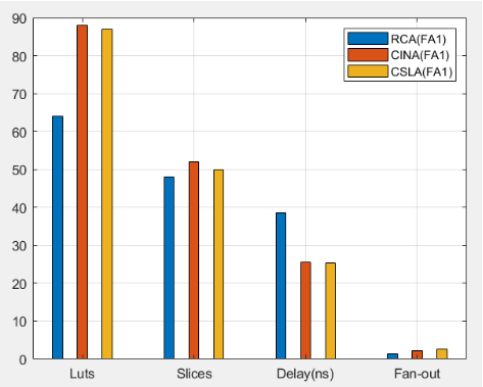

Fig19. Comparison for adders usingFA1

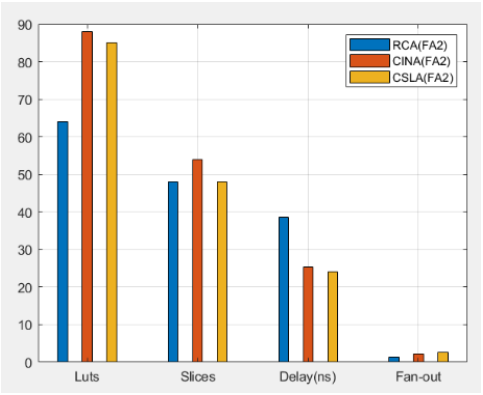

Fig.20 Comparison for adders usingFA2

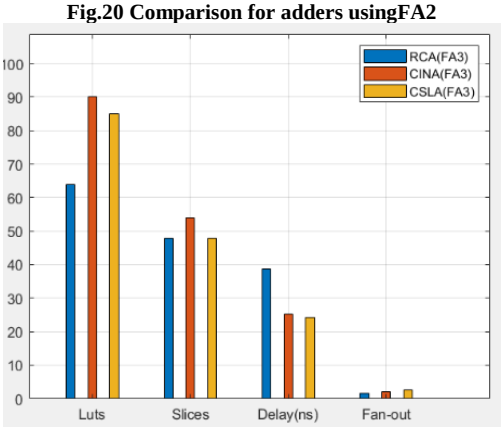

Fig.21 Comparison for adders usingFA3

From Fig. 18,19,20,21 it is evident that using one of full adder cells the LUTs , slices and fan-out is very less for RCA by using any full adder when compared with CSLA and CINA where as CSLA surpasses other two adders in terms of delay performance. The delay for RCA is more than the CINA andCSLA.

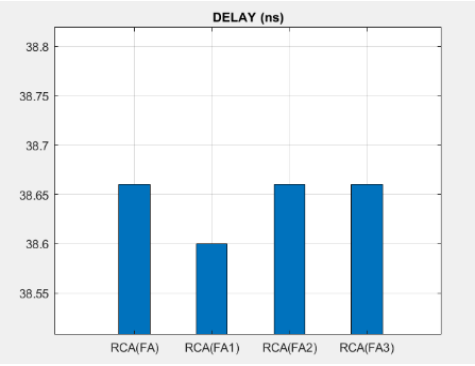

Fig.22 Comparison of delay for RCA using different full adders

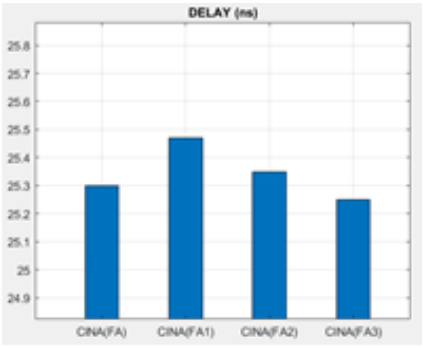

Fig.23 Comparison of delay for CINA using different fulladders

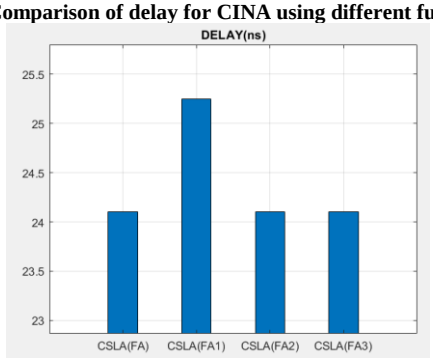

Fig24 Comparison of delay for CSLA using different fulladders

From Fig. 22,23 and 24 it is shown that delay is reduced for RCA, CINA and CSLA using the FA2 and FA3.

VI. CONCLUSION

From above results, it is evident that the LUTs are less for RCA. The LUTs increased by 40% and 36% for CINA and CSLA respectively. The slices (area) are increased by 13% and 4% for CINA and CSLA respectively when compared with the RCA. The more the fan-out the more the load driving capacity. The fan-out is increased by 23% and 55% for CINA and CSLA respectively when compared with the RCA. It is also evident that the delay produced by opting to configurational full adder 2 results in decrease of the delay for RCA, CINA and CSLA . Hence for implementation of RCA, CINA and CSLA, the use of configurational full adder as basic cell will improve the performance in terms of the delayprovided.

Further, this work can be extended in designing and analyzing for various sized adders like 64-bit, 128 bit . The work also can be extended in designing and analyzing other 32-bit adders like carry save adder and carry skip adder.

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