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Design of 8-Bit ALU Design using GDI Techniques with Less Power and Delay

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Abstract—*Arithmetic Logic Unit (ALU) is a substantial fragment of microchip. Cutting-edge computerized processors, legitimate and math activity accomplishes making use of ALU. This paper depicts an 8-Bit ALU operating with a lowest power 11-Transistor Full Adder (11-T FA) and Gate dispersion input (GDI) centered MUX. All structures were simulated using Tanner EDA software version-15 with 32 nanometer BSIM4 innovation. Execution examinations were furnished as for voltage, power, postponement and power delay item. In this paper 8-bit ALU operated in subthreshold region, selected 0.7 V_{DD} for maintain the both power as well as delay. In 8-bit ALU of GDI proposed model, less than 82% power consumption reduced as compare with CMOS 8-Bit ALU due to voltage level improvement.*

Keyword--- ALU (Arithmetic logic unit), FA (Full Adder), GDI (Gate diffusion input), MUX (Multiplexer)

I. INTRODUCTION

The utilization of VLSI innovation has long-drawn-out to that level here a massive amount of transistors be able to be actualized in a solitary Bit. Complementary Metal Oxide Semiconductor (CMOS) remained the spine in blended sign as this one's diminishing force offers great blend segment for modest and computerized structure. The supports of intensity utilization in CMOS circuits are dynamic power (P_d), short out power (P_{sc}) and static power (P_s). Along these lines, the complete power utilization (P_t) is

$P_t = P_d + P_{sc} + P_s$ (1)

P_d expends because of capacitive burden in addition to clock recurrence. P_{sc} is brought about by short out current. P_s is brought about by leakage current between the substrate and dispersion region. Expanding transistor quantityfor every chip territory plus scaling down advances have devoured additional power along these lines.

The principle goal line is in the direction of decreasing the power utilization via employing unique approaches intended to improve the demonstration of Very Large Scale Integration circuits. Arithmetic Logic Unit is the segment of PC processor which accomplishes number-crunching as well as coherent activities [1]. ALU is a solely combinational rationale circuit whose yield deviates with altering information reaction.

II. PREVIOUS WORK

Power diminishing could be achieved at Module Level or at circuit level or at architecture level [2]. In simple switch procedure select info rationale as control rationale and permits additional info signal from gate terminal [3]. Full Adder is a fundamental structure in place of planning an ALU. Various sorts of FA planning in place of limiting force are, for example, Hybrid Full Adder (H-FA) and 10 Transistor reduced power Full Adder (10T-FA) and 11 transistor FA (11T-FA) etc. FA works in mode of ultra-low through utilization of subthreshold current then expends low power [2], [3]. Full Adder is manufactured utilizing near to the ground power XOR gate and 2:1 multiplexer. ALU configuration employing FinFET innovation has dual gates that are electrically free. This limits the intricacy of the circuit and furthermore lessens the power utilization because of diminishing the leakage current. In Fin Field Effect Transistor (FinFET) innovation "Fin" is dainty silicon that shapes the frame of the gadget [4]. Arithmetic Logic Unit plan utilizing the re-configurable rationale of Multiple Input Floating Gate - Metal Oxide Semiconductor (MIFG-MOS) transistor has numerous information that expands the effectiveness of the circuit. MIFG-MOS transistor offers low and high conditions by watching theweighted aggregate of altogether things considered. MIFG-MOS transistor diminishes the quantity of transistors and the unpredictability with the circuit in addition to improving the exhibition of the circuit limit the postponement as well as diminishes the power dissemination [5]. AT the point where channel size is scaled discouraged for organizing the circuits, Gate of metal and higher value dielectric K are to be advertised.

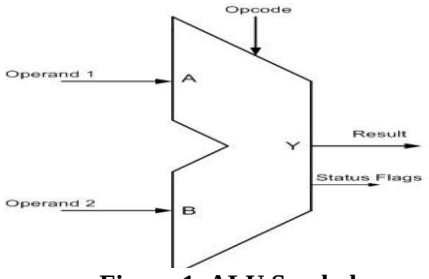

Figure 1. ALU Symbol

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III. CIRCUIT DESIGN FOR ALU

Arithmetic Logic Unit is the center Bit of PC/computerized processor that implements number juggling as well as consistent activity.

For example, increase, decrement, expansion and subtraction as an arithmetic unit and OR, AND, X-OR, X-NOR as a Logic Unit. Arithmetic Logic Unit works through making use of Full Adder and Mux.

Table 1. Truth Table (TT) of 8-Bit ALU

S2	S1	S0	Functionality
0	0	0	Operand1 | operand2
0	0	1	~(Operand1 ^ operand2)
0	1	0	(Operand1 ^ operand2)
0	1	1	Operand1 & operand2
1	0	0	++ Operand
1	0	1	Operand1 + operand2
1	1	0	-- Operand
1	1	1	Operand1 - operand2

A. 11 Transistors Full Adder Circuit Design

11 Transistors Full Adder (11T FA) acts the fundamental utilitarian component of an ALU Structure. 11T utilized structure of FA limits the power besides diminishing the deferral. FA outlined in Figure. 2 operates on a power source (V_{DD}) of 0.9 voltage. Sources of information A is applied to the gate terminal of NMOS-1 and PMOS-1 besides channel terminal of PMOS-2. Sources of information B is applied to NMOS-2 and PMOS-2 of gate terminal as well as the NMOS-1 of channel terminal. At the point as soon as source voltage (V_s) is more noteworthy compared to Threshold Voltage (V_{TH}), the transistor is ON condition and passes the sign deplete point from gate point and passes the gate voltage (V_G) to the drain terminal. Hence, when i/p A is ON, then pass i/p B other way around. FA is assembling utilizing minimal power XOR gates and 2:1 mux. XOR gates give the aggregate yield and multiplexer dependable for complete (Cout).

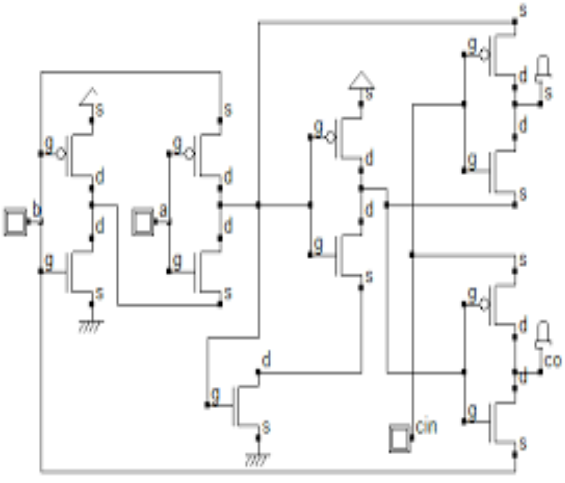

Figure 2. Schematic of 11 Transistor Full Adder

An additional NMOS-6 transistor uses sub-threshold current in ultra-low mode and devours low-control. A solid reversal district gate terminal voltage to voltage of source terminal (V_{GS}) is greater than the voltage of Threshold level (V_{TH}), dominant part bearers expelled from the region of the gate and minority bearers are created, at powerless reversal area V_{GS} is underneath than V_{TH} less minority bearer is delivered, yet their essence produces spillagecurrent this current is called sub-threshold current. If V_{dd} isbelow than the V_{th}, this current can be used and the circuitkeep running in ultra-low mode and utilize less power. 11T FA operate with outside NMOS-6 transistor in subthreshold mode.

B. GDI established MUXs

GDI procedure is an area effective procedure that ingests lesser power in addition to reducing the numeral of transistors required [7]. GDI techniques extends the chip configuration 'twin well' or silicon on insulator [8]. In addition to optimizing gain plus V_{th} of N-Type and P-Type unit, Twin-well system provides isolated optimization for n-type and p-type transistors [9]. Metal oxide semiconductor and bipolar expertise are correlated with silicon on insulator in a solitary phase. GDI practice affords more input to the cell and maintains complexity of circuit. GDI procedure resolves the issue of weak high to low switching condition of PMOS and offers a full swing on the interior point of the circuit [10]. Figure 3 portrays a GDI established 2:1 multiplexer.

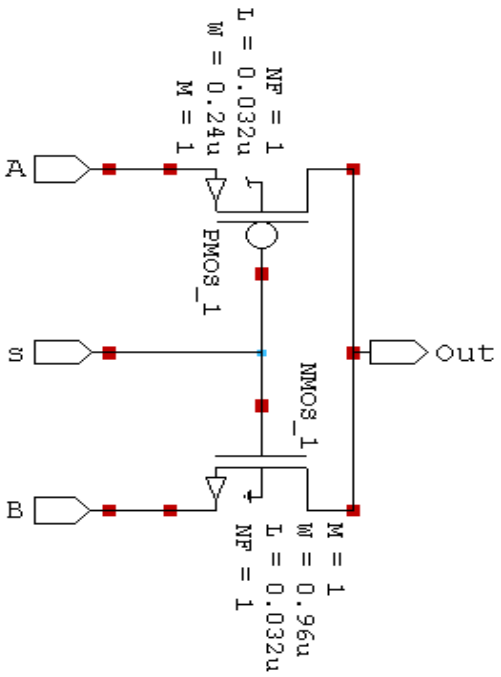

Figure 3. GDI established Mux 2

The select line S of mux is mutual for the input of gate terminals of NMOS-1 as well as PMOS-1. Information of A and B are linked towards the PMOS-1 and NMOS-1 at source terminals individually. At the point where S is low then and there exits the condition were PMOS-1 is in highstate and passes the information A from the terminal of source to terminal of drain. NMOS-1 is high at the point where S is high, while PMOS-1 low. Yield is regular for PMOS-1 and NMOS-1 channel terminals. Fig. 4 outlines the 4:1 multiplexer.

4:1 multiplexer is configured utilizing three 2: 1 multiplexer [10]. The S_0 and S_1 selection lines are filled in as an exchanging input that is responsible for the transistors ON and OFF conditions [11], [12].

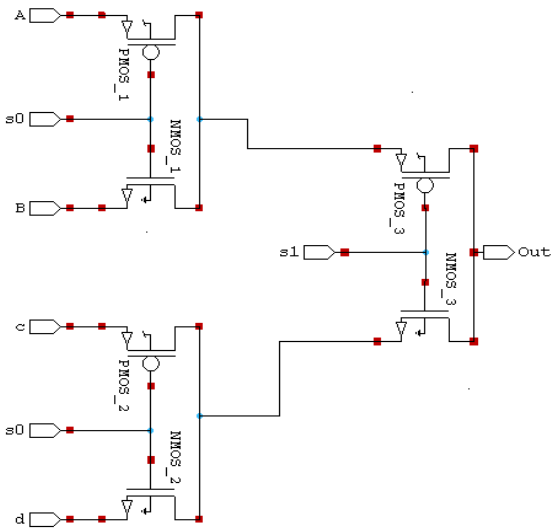

Figure 4. GDI established MUX 4

S_0 is normal to enter in place of NMOS-1, NMOS-2, PMOS-1 and PMOS-2 at gate terminal, S_1 is normal contribution in place of gate terminals of NMOS-3 as well as PMOS-3. Information sources remain associated with the transistor's source terminal.

C. Plan of an 8 bit ALU

FA acts as the backbones for Arithmetic Logic Unit. 8-Bit Arithmetic Logic Unit is planned utilizing 8-Bit Ripple Carry Adder [13], [14]. Ripple Carry Adder is in charge of the number juggling activity performed by ALU. Different building blocks required to structure ALU are 2:1 multiplexer and 4:1 multiplexer. Legitimate activity is performed by utilizing mux [15], [16]. Figure 5 outlines a 1-Bit Arithmetic Logic Unit configuration. It utilizes two 4:1 multiplexer and one 2:1 mux and a FA.

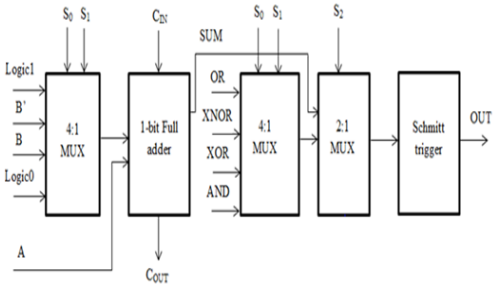

Figure 5. 1 bit ALU

Figure 6 portrays 8-Bit Arithmetic Logic Unit, Ripple carry Adder is the fundamental structure square of 8-Bit Arithmetic Logic Unit which plays out a math activity. Info A (a0, a1,….a8) was applied in head contribution of Ripple carry Adder, Info B (b0, b1,….b8) was applied with the first contribution of 4:1 mux and goes to the second contribution of Ripple carry Adder the yield of 4:1 multiplexer and implements the math activity. Consistent activity performs through the falling mix of 4:1 multiplexer and 2:1 multiplexer.

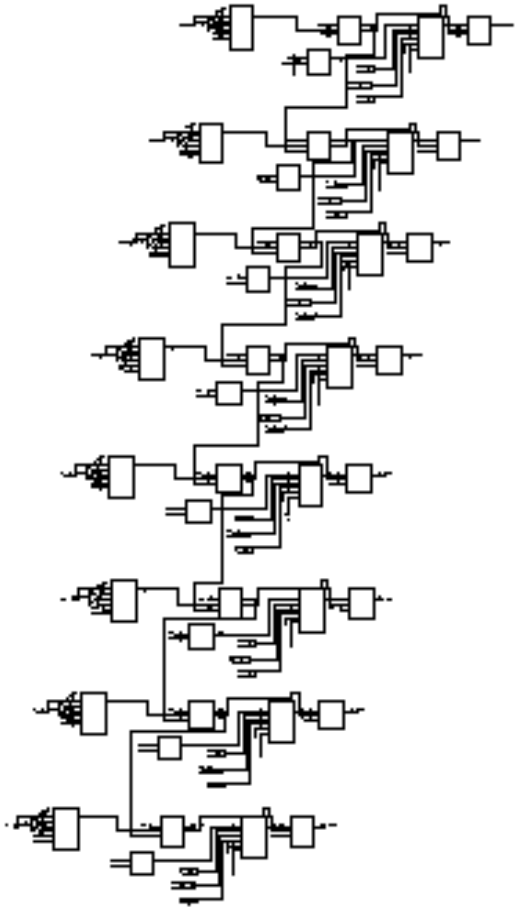

Figure 6. 8 Bit ALU

IV. RECREATION AND RESULTS

All plan were recreated utilizing Tanner EDA apparatus W-alter at progress time 32 nanosecond (ns). Figure. 7 demonstrates the graph obtained for 11-T FA, by input blend 000, 001, 010, 011, 100, 101, 110 and 111. At 000, 010 & 110 issue were spotted. These issue are unraveled via including an additional transistor NMOS-6

Figure 7. Wave shape obtained for 11T

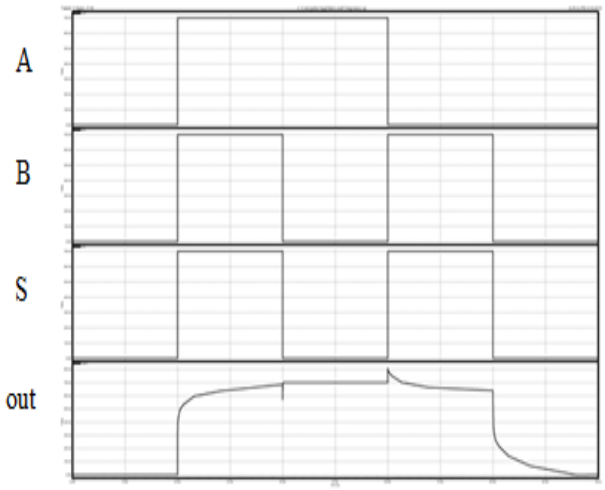

Figure 8 Wave shape of 2:1 MUX

Figure 9. Wave shape of 4:1 MUX

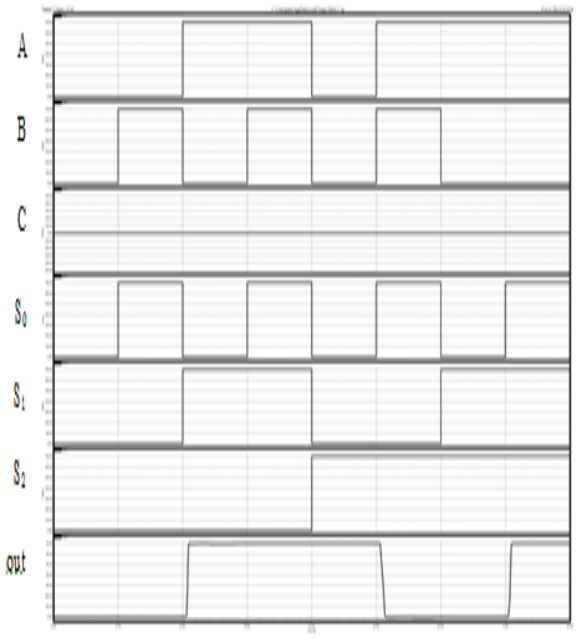

Figure:10. Wave Shape obtained for 1-bit ALU

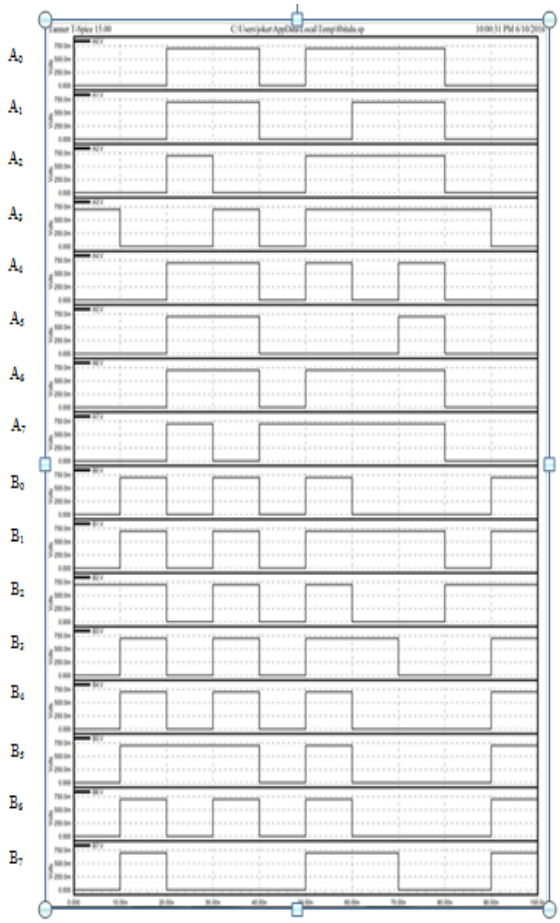

Figure 11. Input Wave shape for 8-bit ALU

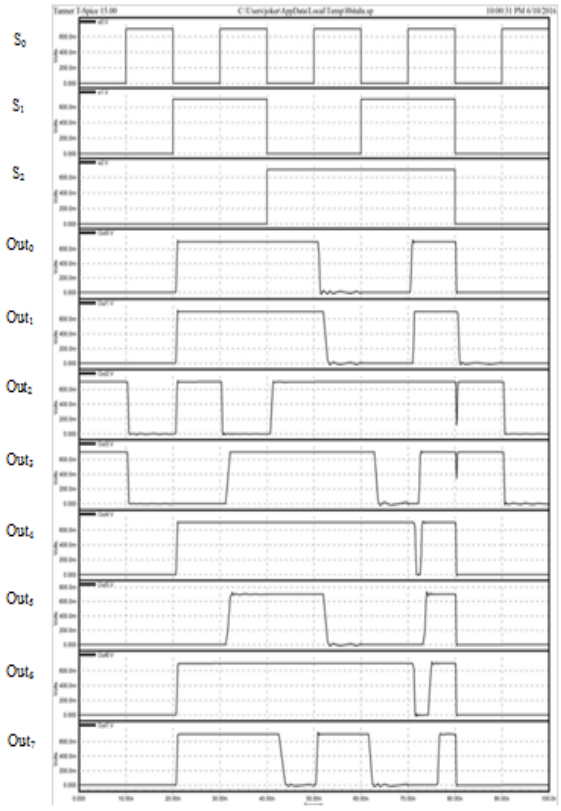

Figure 12. Select line and output wave Shape of 8-bit ALU

Power and Delay varies with the Supply voltages. Table 2 show the results varies with supply voltage from 0.5 volt to 0.9 volt.

Table 2: Power and Delay of 8-bit ALU with the variation of V_{DD}

V_{DD} (in Volts)	Power(in µW)	Delay (in nsec)
0.9	39.23	1.42
0.8	25.48	1.49
0.7	16.34	1.63
0.6	10.12	1.92
0.5	6.16	4.66

The results of proposed model is shown in table 3. That results is obtained by 0.7 $V_{DD,}$

Table 3: Proposed Design Results

Design	11-T FA	MUX2	MUX4	1B ALU	8B ALU
Delay	147pS	113pS	5nS	10nS	2nS
Power	56nW	30nW	514nW	2 µW	16µW
PDP	8232 (nW*pS)	3390 (nW*pS)	2570 (nW*nS)	20 (µW*nS)	32 (µW*nS)

Results comparison between previous work and purposed work shown in table 4.

Table 4 Comparison between Previous work and Purposed work

Ref. No.	ALU type	Technology	Power
1.	FinFET based ALU	45nm	8.38mW
2.	10T FA based ALU	45nm	1197.5µW
3.	RCA based ALU	65nm	413.2µW
5.	Clock gating based ALU	180nm	5.27mW
Purposed model	**8-bit ALU**	**32nm**	**16.34 µW**

V. CONCLUSION

This proposed model design for 8-Bit Arithmetic Logic Un using 11-T FA followed the principal of GDI Techniques. Thi Paper is based on 32 Nanometer Technology. In this paper 8-b ALU operated in subthreshold region that's why consumed les power as compare with previous models. Power decreases wit V_{DD} and Delay increases with V_{DD}. So we have selected 0.7 V_D for maintain the both power as well as delay. In the propose model, less than 82% power consumed as compare with 8-B CMOS ALU.

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