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Performance Efficient Alu using Finfet

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Abstract: ***According to the prophecy of Moore, the concentration of transistors in an integrated circuit doubles every two years. But this is limited by the technologies used in the fabrication of integrated circuits, as the systems are scaled down. FinFET technology aims to combat this challenge. The construction of power efficient high speed Arithmetic & Logical Unit (ALU) using FinFET technology is proposed in this paper. Proposed FinFET based ALU is designed with arithmetic functions like high speed addition, multiplication and logical functions such as AND and XOR. Simulation results of the proposed power efficient high speed FinFET ALU proves to be better with a power saving of 80.5%. FinFET has the advantage of providing low power without compromising on the Performance. The power analysis for ALU is done using CADENCE-VIRTUOSO, which is known for its accuracy.***

Keywords: ALU, FinFET, high speed addition, CMOS technology, leakage current.

I. INTRODUCTION

With the invention of the first Integrated Circuit at 1958 by Jack Kilby, IC technology has progressed at a great pace. MOS transistor scaling has led to high density, highperform ance chips.But many serious issues that occur in MOS devic es as the package size continues to shrink are obstructing thi s miniaturization.Energy dissipation is a major challenge ou t of these problems. It waslisted as one of the obstacles for s emiconductors in the International Technology Roadmap.T hough CMOS technology has the least power consumption compared to bipolar technology, demand for power effective and power efficient circuits is growing at a greater pace.This has culminated in the need for new technology fo r transistors. Another such technology is studied, tested and evaluated for the different gates used in the Arithmetic and Logical Unit in this paper, FinFET technology.From the cir cuit operation perspective, a FinFET is very similar to MOS FET.Two gates, however, have greater control over the flo w, which can alter several output parameters. The FinFET's distinctive feature is that the conducting channelis covered i n a thin "fin" of silicon that forms the device's core. The fin's thickness defines the device's active channel size. The gate wraps around the top, providing better channel control and allowing very little current to escape through the body when the system is in' off' mode. This, in effect, allows lower threshold voltages to be used a nd leads to better output and power. The first section briefly explains FinFET's functionality and the second section describes ALU's function using CMOS and FinFET technology. The simulation analysis of CMOS ALU and FinFET ALU describes the low power consumption obtained during FinFET operation.

In this paper, a comprehensive analysis has been done on un-doped double gate MOSFETs, also known as FinFET which has the potential to improve the channel control and reduce the dopant fluctuations. Short channel effects and leakage current in nanoscale MOS FETs are a significant source of power dissipation.There are many second order effects that affect the scaled down devices like drain induced barrier lowering, gate oxide tunneling of electrons, hot-carrier injection and punch through leakage. But the front and back gates in FinFETs are electrically coupled to effectively control the leakage currents. FinFET devices are therefore best suited for low-power designs. The low-power techniques employed in FinFET circuits diminish the circuit's power while simultaneously addressing the CMOS technical issues. Therefore, the dual-gate technique allows the merging of transistors to save total power and produce low flow and high speed output.

II. BACKGROUND

Many researchers have explored the possibility of the implementation of different circuits using FinFET technology for power efficient designs.

Prateek et al., (2008) have done an evaluation of the FinFET Circuits using different supply voltages and different threshold voltages. A technique for FinFET-based low-power circuit synthesis has been proposed in this paper. To increase the power performance of FinFET-based global interconnections, a method named TCMS (Threshold Control by Multiple Supply Voltages) has been proposed. This scheme represents a significant divergence from the conventional multiple-supply voltage schemes considered in the past. On an average, around 65% power savings and area savings are obtained using this technique.

Nirmal et al., (2010) have proposed a NAND gate using FinFET technology. Leakage power savings are analyzed for the various logic design styles through the astute use of FinFET. Bindi et al., (2011) have designed and done the implementation of a Full Adder cell for ALU using FinFET. For four different cell models of FinFET-based Full Adder in terms of average dissipated power, delays & energy-delay-product (EDP) have been examined and they have achieved 94 % reduction in delay, 97 % reduction in power dissipation and 99 % reduction for both PDP and EDP.

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Dhulipalla et al., (2011) have proposed the realization of 4-bit ALU with FINFETS, using addition & subtraction as the arithmetic functions and AND & OR as the logical functions.

Islam et al., (2011) have proposed the use of sub-threshold voltage FinFET transistors to improve the energy/switching of the 1-bit static full adder. Saraswat et al., (2013) have also proposed a 1-Bit full adder cell using Double Gate FINFET. They have used only 10 transistors while maintaining the performance. They have investigated the use of Double Gate FinFET technology by using high speed-low threshold voltage transistors to provide low leakage. Ajay et al., (2013) have proposed the implementation of Logic Gates & Flip-Flops using FinFET Technology. In this paper, an evaluation of the symmetric (Symm-*0G*) and asymmetric (Asymm-*0G*) gate work function of FinFET in a high performance process has been investigated using Computer aided design stimulations. The design of FinFET logic gates, latches and flip-flops is also explored using mixed-mode 2-D system simulations for optimum leakage. They found that using a single IG mode system at the top of a series stack is sufficient to significantly reduce leakage.

The main design objective for VLSI designers is to attain performance necessities within a power budget. This paper has explored how circuits based on FinFETs can be made power-efficient.

III. PERFORMANCE EFFICIENT ALU USING FINFET

Power consumption is a serious issue in processor design. ALU is one of the significant parts of the processor. ALUs are designed with a combination logic circuit that contains a number of functional components for various arithmetic & logic operations where their output changes asynchronously in accordance with input changes. This circuit performs operations depending upon the select line given to the Multiplexer. Block diagram of ALU is shown in the Figure 1.

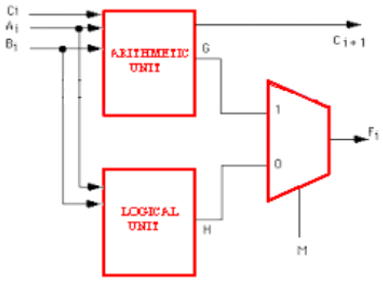

Figure 1 Block diagram of the ALU

Mathematician John von Neumann proposed the ALU model in 1945 for a computer called the EDVAC. ALU is a digital circuit that performs arithmetic and logical operations on integer binary numbers. It is an indispensable component of the central processing unit (CPU) found in many computers. Operands are provided as inputs to the ALU along with a code to select the operation. The result of the completed operation is the output of the ALU.

In this paper, it is proposed to design a performance efficient ALU with optimum power and high speed.

A. ALU using CMOS

An ALU is designed with the following functions:

Arithmetic unit consists of

- ➢ Adder
- ➢ Multiplier

Logical Unit is comprised of

- ✓ XOR gate
- ✓ AND gate

Table 1 shows the operation of ALU. Here each unit consists of an individual select line based on which the intended operation is performed. For an Arithmetic Unit if the Select line is 1, the inputs are multiplied else the output contains the added inputs. The Logical Unit will perform the AND operation when the Select line is 0, otherwise the output is the XOR of inputs.

In this paper ALU is developed using FinFET technology with a Carry Look Ahead Adder which accelerates the speed by decreasing the quantity of time needed to calculate carry bits. The Output Carry and Sum is obtained without waiting for the propagation of the carry signal through the intermediate stages. The conventional ALU is simulated using 180nm CMOS Technology with the supply voltage of 1.8V. Figure 2 shows the schematic of ALU using CMOS technology.

TABLE 1 Operation Of Alu

FUNCTION	SELECT LINE	
	0	1
ALU	LOGICAL	ARITHMETIC
ARITHMETIC	MULTIPLIER	ADDER
LOGICAL	XOR	AND

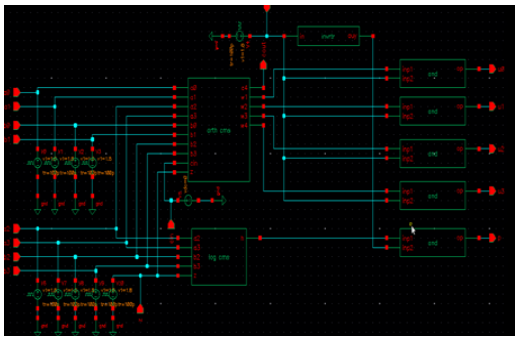

Figure 2 Schematic of ALU using CMOS

ARITHMETIC UNIT OF ALU

Arithmetic Unit performs mathematical operations like Addition and Multiplication on the given number of inputs. The designed Arithmetic unit comprises of Fast adder which is a 4 bit CLA adder & a 2 bit Multiplier. It operates when a low signal i.e binary 0 is given as input to the select line of the multiplexer.

ARITHMETIC UNIT OPERATION

The Adder or Multiplier operation will be selected based on the select line in the Arithmetic unit. Figure 3 represents the schematic of Arithmetic Unit of ALU. If the select line (z) goes low the output of the arithmetic unit has multiplied inputs, else it contains the added inputs.

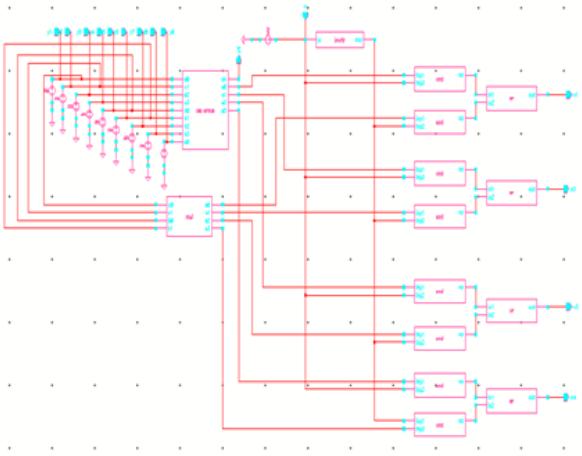

Figure 3 Schematic of Arithmetic Unit using CMOS CLA Adder

A Carry-Look-Ahead adder (CLA) is a type of adder used in digital logic. A CLA enhances speed by decreasing the quantity of time needed to calculate carry bits. It can be distinguished with the ripple carry adder for which each full adder must wait to receive its carry in to calculate its output carry bit. The carry-look-ahead adder calculates carry bits directly from the given inputs.

The speed of addition is greatly enhanced using the CLA.

OPERATION OF CLA

To speed up addition two signals P-propagate carry and G-Generate carry are created using the direct inputs, addends & augends'. The block diagram of 4-bit CLA Adder is shown in Figure 4 and Figure 5 shows the schematic of CLA.

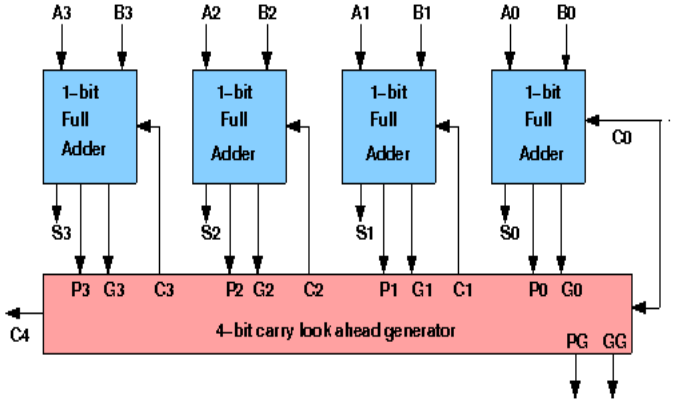

Figure 4 Block diagram of CLA

The signal from input carry c0 to the final carry c4 requires an AND gate & an OR gate, which constitutes two gate levels. If the parallel adder has 4 full adders, to generate the output carry c4, it would require 2*4=8 gate levels from c0 to c4. For an n-bit parallel adder, 2n gate levels are required.

To build a CLA Adder, the two signals that are to be generated are Carry Propagator (P) and Carry Generator (G):

$$P_i = A_i \oplus B_i$$
$$G_i = A_i \& B_i$$

The output sum and carry can be expressed as

$$S_i = Pi \oplus Ci$$
$$C_{i+1} = G_i + P_i C_i$$

The Boolean expressions for the carry output of each state can be written from the previous equations.

$C_0 =$ input carry

$C_1 = G_0 + P_0C_0$

$C_2 = G_1+P_1C_1 = G_1+P_1G_0+ P_1P_0C_0$

$C_3 = G_2+P_2C_2 = G_2+P_2G_1+P_2P_1G_0+P_2P_1P_0C_0$

$C_4=G_3+P_3C_3=G_3+G_2P_3+P_3P_2G_1+P_3P_2P_1G_0+P_3P_2P_1P_0C_0$

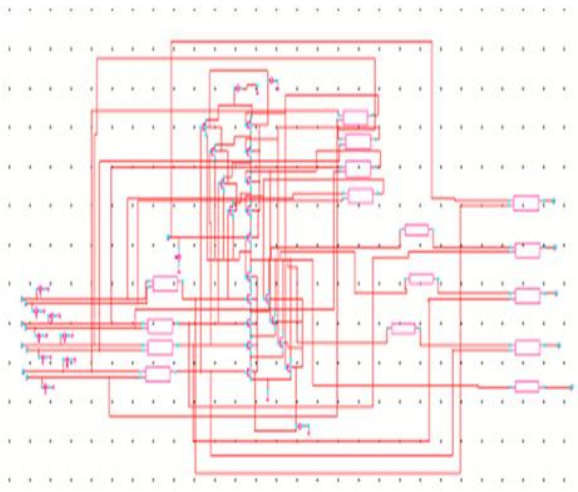

Figure 5 Schematic of 4 bit CLA adder using CMOS

MULTIPLIER

Here the operation is performed by multiplying multiplicand and multiplier bit by bit. A_0 and A_1 are the multipliers, B_0 and B_1 are the multiplicands and C_1, C_2, C_3, C_4 are the products. The first partial product is calculated by multiplying B_1B_0 by A_0. Multiplication of these two bits results in a 1 if both the bits are 1 otherwise the output is 0. This is similar to AND operation. The multiplier operation is explained in the Figure 6.

Therefore first partial product is directly obtained from the AND gate. The second partial product is calculated by multiplying B_1B_0 byA_1 and shifting one position to the left. To calculate the sum of the partial products, half adders and full adders are used.

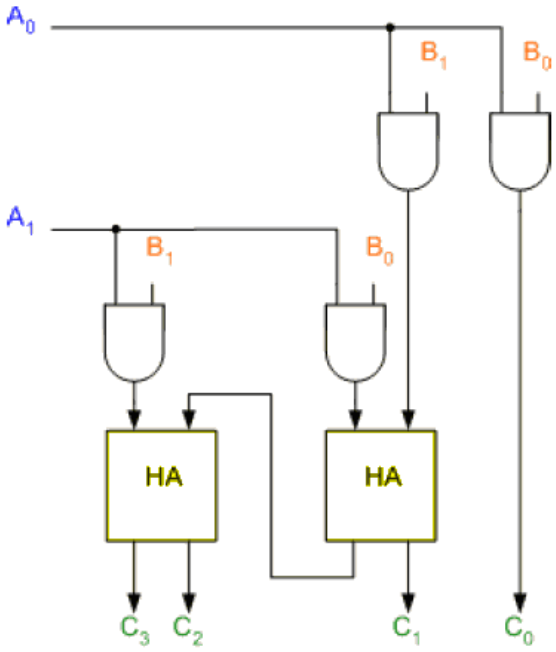

Figure 6 Block diagram of 2 bit Multiplier

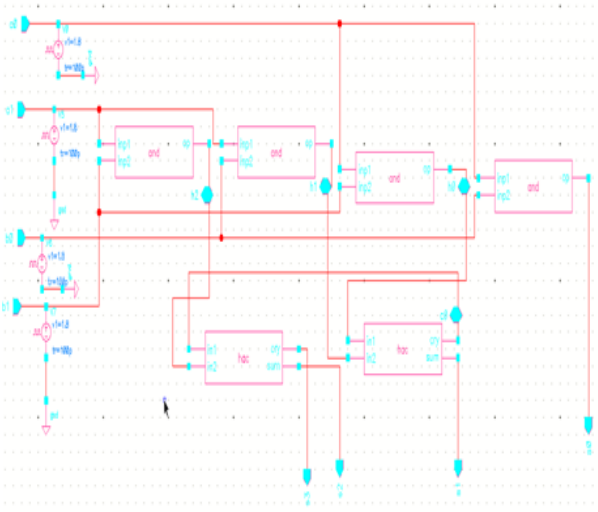

Figure 7 Schematic of Multiplier using CMOS

Figure 6 and 7 shows the block diagram of 2-bit Multiplier and schematic of 2-bit Multiplier using CMOS technology.

LOGICAL UNIT OF ALU

The designed logical unit of ALU comprises of AND and XOR gates**.**

AND GATE

The logical AND operation is performed when the Select line (z) is 1. The AND operation can be represented as

$$C = A.B$$

Its truth table is shown in table 2. In an AND operation only if all the inputs are 1, its output will become 1, else its output will be 0. Figure 8 depicts the symbol of AND gate.

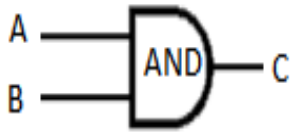

Figure 8 Symbol of AND gate

Table 2 Truth table of AND gate

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

EXCLUSIVE-OR

The two input Ex-OR gate is basically modulo two adders, since it gives modulo addition of two binary numbers. Figure 9 represents the symbol of XOR gate.

$$OUT = (A \oplus B)$$

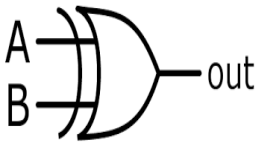

Figure 9 Symbol of XOR gate

Table 3 Truth table of Ex-OR gate

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Table 3 shows that the output of Ex-OR will be activated only for different input levels. For similar inputs, its output will become zero.

B. ALU using FinFET

Short channel effects & leakage current become a serious limitation in scaled down devices fabricated using CMOS technology. These effects become more predominant when the size of the transistor shrinks. Thus FinFET technology overcomes these limitations without compromising the performance. To reduce the short channel effect separate control voltage can be given to each gate which allows dynamic control of threshold voltage Vt.

The design of Arithmetic and Logical Unit using the FinFET structure is proposed in this paper, with the supply voltage of 1.0V. This reduction in supply voltage can also reduce dynamic power consumption significantly. The operation of this circuit is similar to the Conventional ALU. Here FinFET requires Pull Up Voltage of 1.18V and Pull Down Voltage of -0.02V. Fig 10 represents the schematic of the ALU using Double gate transistors.

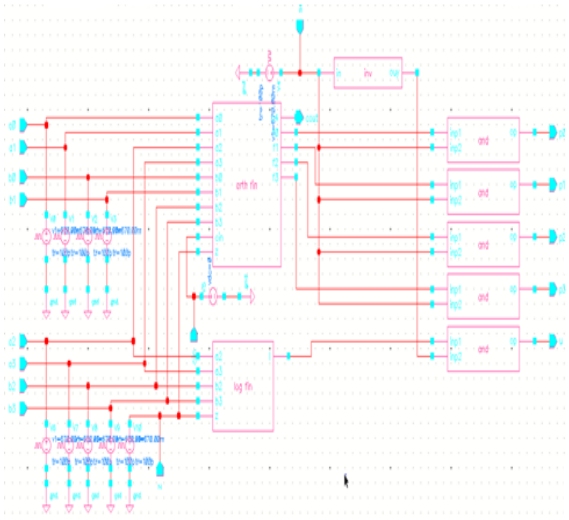

Figure 10 Schematic of ALU using FINFET

ARITHMETIC UNIT OF FinFET

Arithmetic Unit performs mathematical operations like Summation, Subtraction, Multiplication & Division on the given number of inputs. The designed Arithmetic unit comprises of Fast adder which is a 4 bit CLA adder & a 2 bit Multiplier. These circuits are designed with the FinFET transistor with the supply voltage of 1V. It operates when a high signal i.e binary 1 is given as input to the select line of the multiplexer.

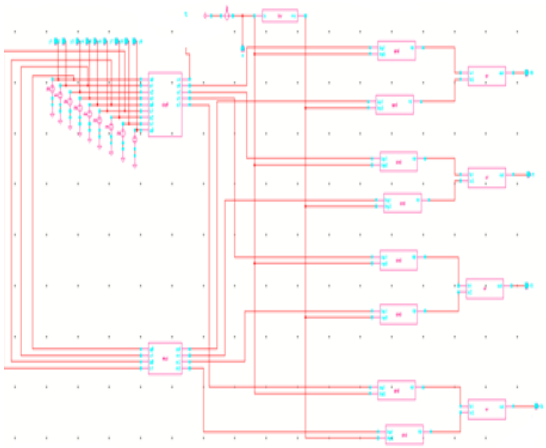

Figure 11 Schematic of the Arithmetic Unit Using FinFET

LOGICAL UNIT OF FinFET

Logical Unit of the ALU using FinFET structure consists of AND and XOR gates. The operation of Logical Unit is similar to that of the Conventional CMOS Logical Unit but with the supply voltage of 1.0V. Figure 11 represents the schematic of the logical unit.

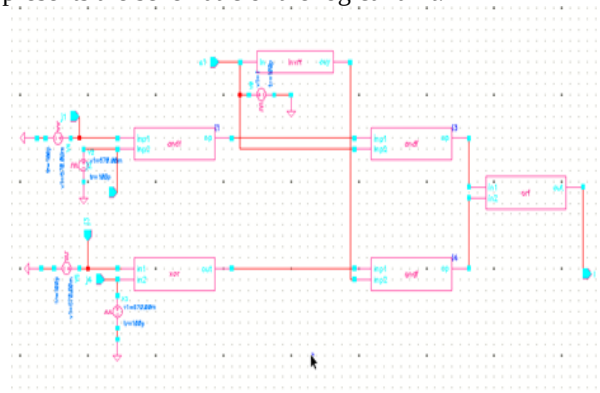

Figure 11 Schematic of Logical Unit

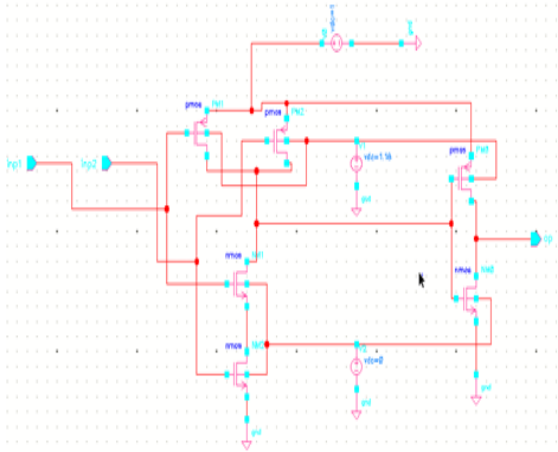

Figure 12 Schematic of AND gate

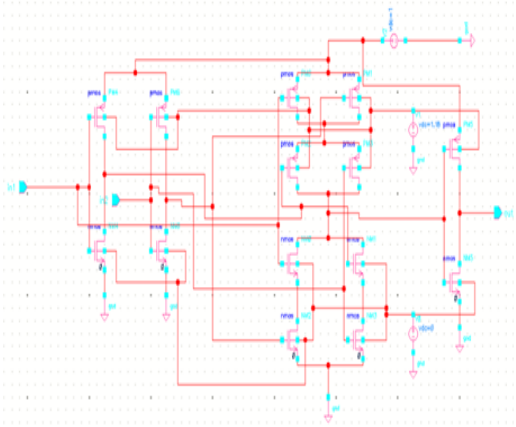

Figure 13 Schematic diagram of XOR gate

Figure 12 and Figure 13 depicts the Schematic diagram of AND Gate and XOR Gate respectively.

IV. SIMULATION RESULTS

SIMULATION RESULTS OF ALU

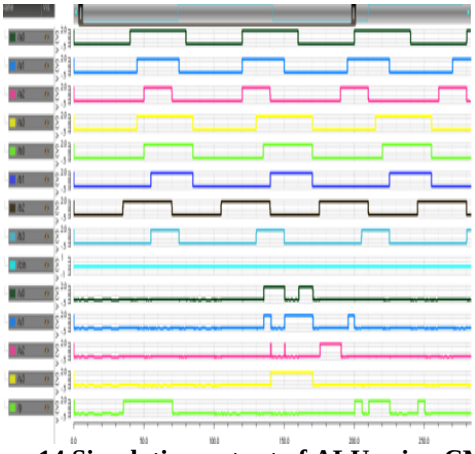

Figure 14 Simulation output of ALU using CMOS

Figure 14 depicts the simulated output of ALU designed using CMOS technology. Based on the select line 'sel' either different operations can be selected.

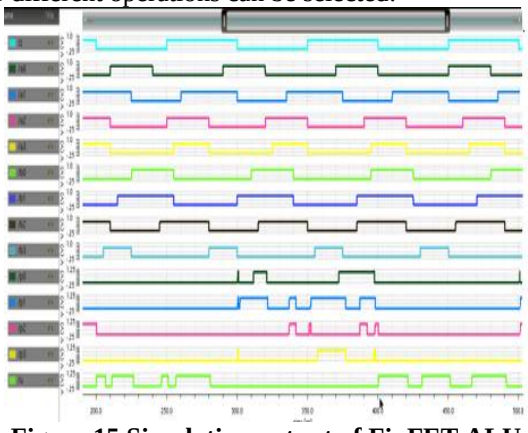

Figure 15 Simulation output of FinFET ALU

Figure 15 represents the output waveform of the ALU realized using FinFET technology. It exhibits the same operation as performed by CMOS ALU. It can be seen that the simulated output of FinFET ALU is similar to that of CMOS ALU.

ARITHMETIC UNIT

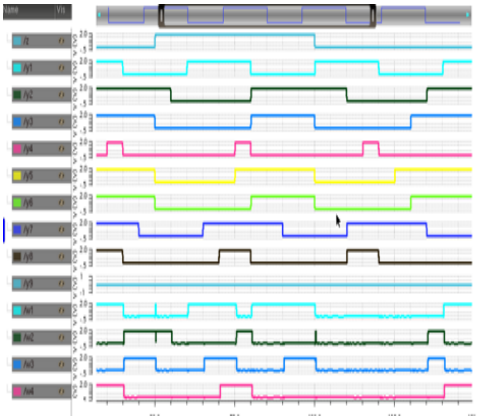

Figure 16 Simulation output of Arithmetic unit using CMOS

Figure 16 gives the simulated result of Arithmetic unit of CMOS ALU. Selection line selects the operation to be performed, based on which adder or multiplier will be executed.

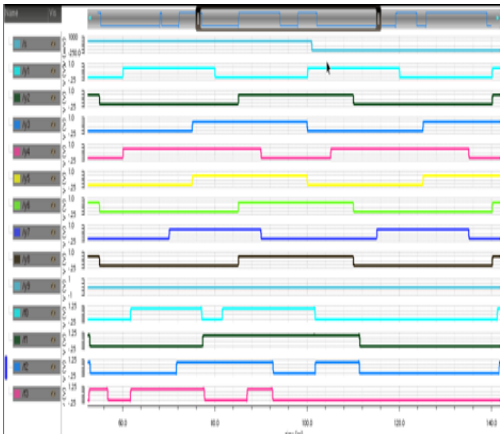

Figure 17 Simulation output of Arithmetic Unit using FinFET

Fig 17 shows the output of Arithmetic Unit of FinFET ALU. It shows that a low value of z enables multiplier to multiply y1y2 with y5y6. A high value of z enables adder to add y1y2y3y4 with y5y6y7y8.

LOGICAL UNIT

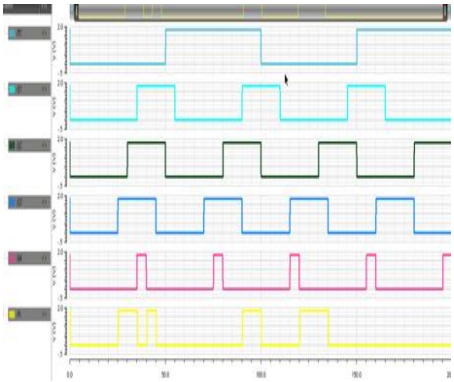

Figure 18 Simulation output of Logical unit using CMOS

Figure 18 shows the output waveform of logical unit in CMOS ALU. Here based on the value of select line XOR operation or AND operation is executed.

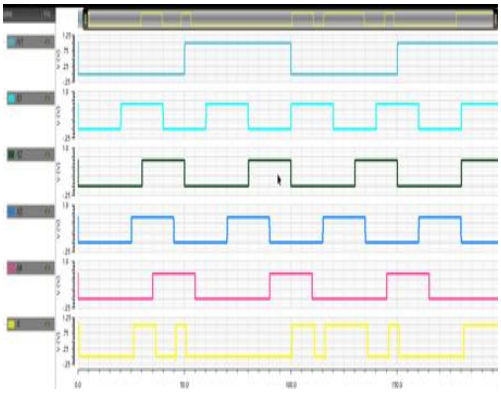

Figure 19 Simulation output of Logical unit using FinFET

Figure 19 gives the stimulated output of logical unit of FinFET ALU. When z is at low level y3 & y4 are XORed else AND operation is performed with y1 and y2.

POWER ESTIMATION RESULTS

The main aim of the project is to prove that there is reduction in power when FinFET technology is used as an alternative for CMOS technology. The power estimation result clearly reveals that the power efficiency of FinFET ALU is more than the CMOS ALU.

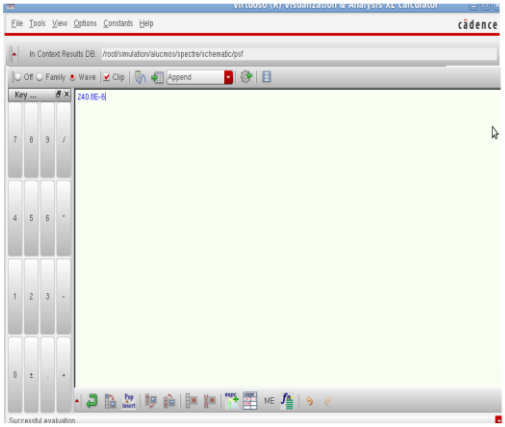

Figure 20 Average Power of CMOS ALU

Figure 20 show the power consumed by CMOS ALU is 240.8uW.

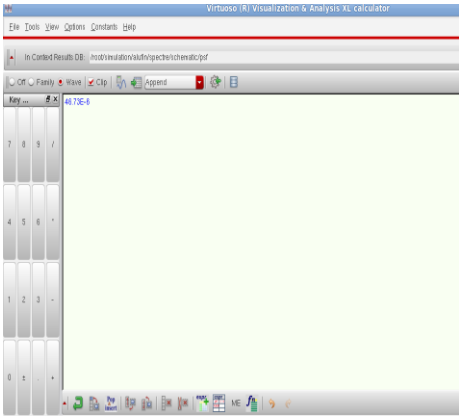

Figure 21 Average Power of FinFET ALU

Figure 21 shows the power consumption of FinFET ALU as 46.73uW.

POWER COMPARISON TABLE

Table 4 Power values of different circuits used in ALU

Function	Average Power	
	CMOS	FinFET
INVERTER	4.98uW	0.82uW

AND	1.25uW	0.35uW
OR	1.46uW	0.41uW
XOR	3.48uW	1.12uW
FAST CLA	289.4uW	64.82uW
MULTIPLIER	27.28uW	8.57uW

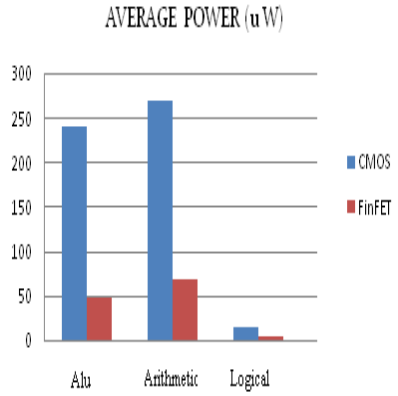

Figure 22 Comparison of Average power consumption

Table 4 represents the Average Power values of various CMOS and FinFET Circuits. Figure 22 gives the comparison of the power consumption of ALU using CMOS & FinFET which shows that circuit has lesser power when FinFET technology is used.

V. CONCLUSION

A Performance Efficient FinFET ALU has been designed using Fast Carry Look Ahead Adder. In the simulation results, functionality of FinFET and conventional CMOS ALU are found to be the same, whereas the power consumption shows a large reduction in FinFET than using CMOS. The average power reduction is 80.5%, hence making the FinFET ALU power efficient along with an enhanced speed of addition, which makes it performance efficient.

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