International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8 Issue-4, November 2019

Digitalized Synchronization of Multi level STATCOM with Switch Fault Elimination

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Abstract: ***With much advancement in the FACTS technologies STATCOM with multi-level inverter provides reactive compensation with less harmonics injection in the grid system. The voltage stress on each power electronic switch is also reduced as the voltage across each switch is low, in turn reduces the switching losses. In this paper a cascaded multi-level inverter with STATCOM application of 2m+1 levels controlling through Space Vector PWM was considered. Switch fault analysis is carried out by detecting and mitigating the fault with a bypass power electronic switch. Design method and parametric analysis is carried out in MATLAB simulation and results arevalidated.***

Keywords—STATCOM- Static Synchronous Compensator,Switch Fault Analysis, SVPWM- Space Vector Pulse Width Modulation, Harmonic Reduction .

I. INTRODUCTION

Among all the FACTS devices in the power systems the STATCOM is the most accepted compensating device to ensure power quality in the grid system. With several advancements in the technology of the control system the efficiency and also the Reliability has been increased for these devices. Modification of simple VSI (Voltage Source Inverter) with a three level PWM operation to a multi-levelPWM (Pulse Width Modulation) output from a Cascaded H-bridge inverter may decrease the harmonic content injected by the STATCOMin the grid and also reduces the stress on the power electronic switches during the operation at higher voltages which in turn reduces switching losses in the device.

In the proposed methodology, we consider a thirteen level Voltage source inverter with six cascaded H-bridges [1] and space vector PWM technique to control the IGBTs (Insulated Gate Bipolar Transistors). Three phase pulses are produced to operate the bridge with an angle difference of 120 degrees to each other. High voltage operations with larger levels increase the number of switches connected to the system which also create vulnerability of the switches to open circuit and short circuit faults during the operation.

Manuscript published on November 30, 2019.
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The number of switches used in a 13 level cascaded H-bridge are 4x6 = 24 IGBTs in each phase. So, it is very important to make sure the detection and mitigation of these faults in the switches with a sophisticated control system and ensure the protection of the grid connected devices from these disruptive failures of switches in the STATCOM.

A model of 13-level cascaded H-bridge with all cells connected in series shown in Fig.1.

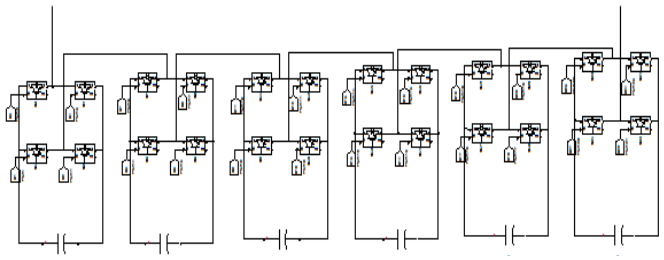


Fig. 1: 13-level cascaded H-bridge

Each cell consisting of four IGBT switches with anti-parallel diode to avoid circulating current in the system during the operation. Each cell has a high rating capacitor on the DC side, to which the charge and discharge conditions are controlled by the SVPWM (Space Vector Pulse Width Modulation) technique applied to the switches.

II. MULTILEVEL SPACE VECTOR PULSE WIDTH MODULATION TECHNIQUE

Among several PWM techniques [2] the SVPWM technique is the most advanced and reliable method for the inverting operations. The digitalized control of the switches makes the system accurate with precise switching state conditions. However the basic sinusoidal PWM technique is simpler than the SVPWM, but the peak output voltage of the inverter is limited to half of the input DC voltage. In the SVPWM technique the sampling control signals are generated at regular intervals of time with better harmonic performance and converter output voltage of the inverter is 15% more than the SPWM technique [3]. The SVPWM has a complicated control where the required sector (1 to 6) has to be identified and selected for the required output voltage andthe AC side.The SVPWM control signals are formed by the sinusoidal signals with the offset voltage generation with the given relation.

$$V_{offset} = -(V_{max}+V_{min})/2 \quad (1)$$

The space vector control [7] diagram in MATLAB Simulink modelling is shown in figure 2. The output signals are passed through a gain of $2/\sqrt{3}$ to increase the output reference value from 0.866 to 1 and maintain the modulation index as 1.

In the input, the MUX gain 'K' is the modulation index in terms of 6*K (where 6 is the number of cascaded H-bridges).

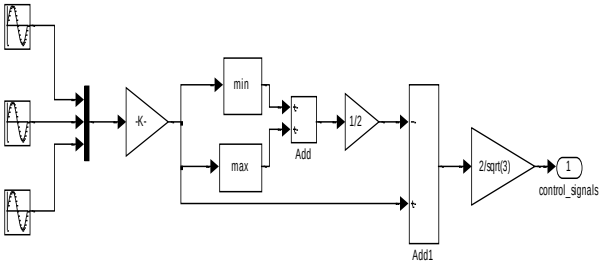


Fig 2: Space vector control signals generation

Where, the V_{max} is the maximum voltage of the three sinusoidal input signals and V_{min} is the minimum of three phase sampled sinusoidal signals. The offset voltage is the sector selection of the controller to control the switching pattern. The control signals with fundamental frequency (50Hz) are compared withtwelve carrier waveforms (triangular waveforms) which gives the PWM [3] signals to the IGBTs connected in the cascaded H-bridge. Figure 3 shows the comparison of fundamental waveform with the carrier waveforms.

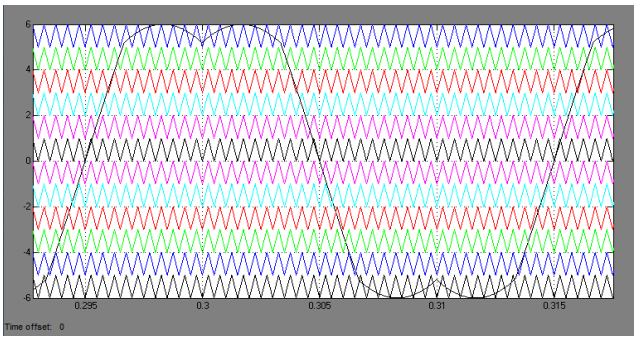


Fig. 3: Fundamental space vector control signal with 12 carrier waveforms

Among several phase shifted PWM techniques, PD(Phase Disposition) is utilized for the generation of twelve triangular waveforms .Each triangular and fundamental comparison generates a signal which is given to two diagonal IGBTs in a cascaded H-bridge. The output voltage of a 13-level waveform with DC input voltage can be seen in figure 4.

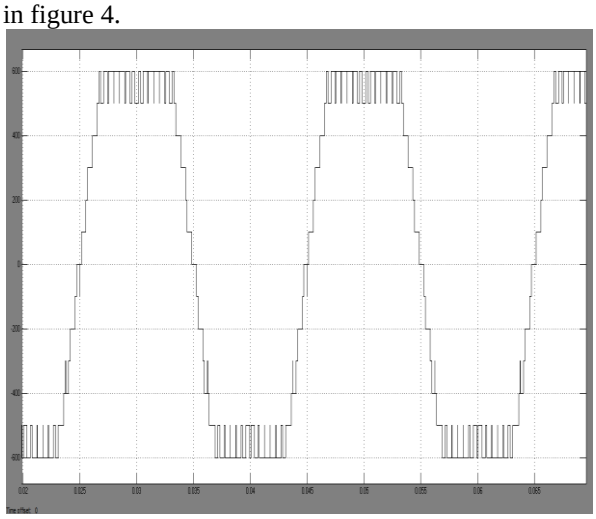
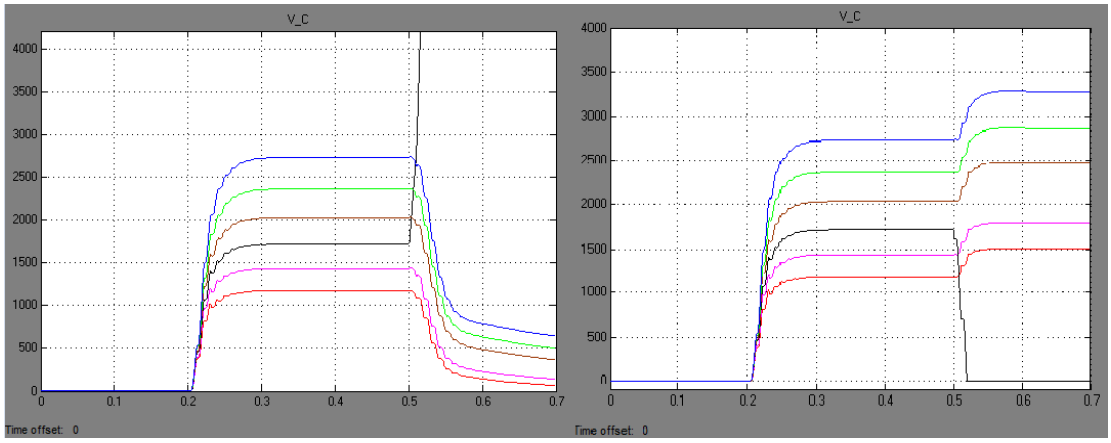


Fig. 4: 13-level output of the multi-level SVPWM inverter

III. PROPOSED FAULT DETECTION AND MITIGATION TECHNIQUE

Fault analysis is carried out on the STATCOM [4] with introduction of open circuit and short circuit faults in any of the switches (IGBT) in a random cell causing voltage drop in the grid during compensation. In practical applications the short circuit condition is more severe than the open circuit condition, however in MATLAB modelling the open circuit has more effect on grid voltagesas compared to short circuit.

At the DC side high value of capacitances are connected, the voltages of the six capacitors changes with the faults in the switches of the cascaded cells. The voltages of the capacitors on the DC side with open and closed faults are shown in the figure '5a' and '5b' below.



(a) **(b)**

Fig. 5a: Open circuit capacitor voltage, 5b: short circuit capacitor voltage

The possible faults in the 24 switches of the cascaded H-bridge are

$C_1 = Vdc0(S_{21}–S_{22} +S_{31}–S_{32}+S_{41} –S_{42} +S_{51} –S_{52} + S_{61} -S_{62})$ (cell 1 faulted)

$C_2 = Vdc0(S_{11} – S_{12}+S_{31} – S_{32}+ S_{41}– S_{42}+S_{51} – S_{52}+S_{61} - S_{62})$(cell 2 faulted)

….

$C_6 = V_{dc0}(S_{11} – S_{12}+S_{21} – S_{22}+S_{31} – S_{32}+S_{41} – S_{42}+ S_{51} – S_{52})$ (cell 6 faulted) (2)

It can be simply written as$C_i=V_{dc0}\sum(sj1-sj2\ )$(3)

j=1 to n,i=1…n, n is the number of blocks

$X_i=\left|\ Eout–C_i\ \right|$ (4)

Where $X_i\rightarrow$ Faulted block.

The ideal output voltage

$\hat{E}_{out},0 = nV_{dc0}/\sqrt{2}$ (5)

$E_{out},fault=(n\ -1)V_{dc0}/\sqrt{2} = (n-1)/n*\hat{E}out.$ (6)

Among the voltages of six capacitors the faulty capacitor voltage is varies rapidly after the fault. In open switch fault the capacitor voltage is charged to top voltage tending to infinity whereas in closed switch fault the voltage of the capacitor drops down to zero. The above given capacitor voltages are taken as a feedback to the detection circuit where the six relays for six bypass switches are provided in a certain operating region.The detection control model is shown in figure 6.

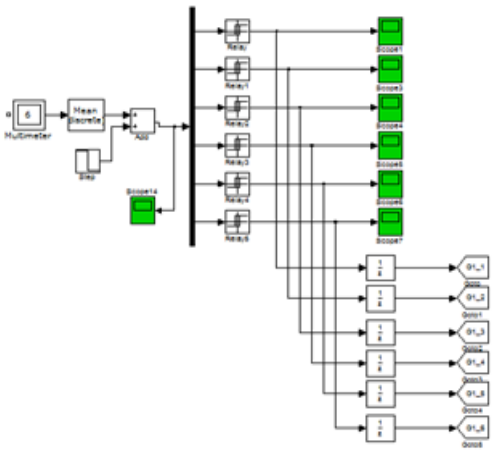


Fig. 6: Fault detection and mitigation relay model

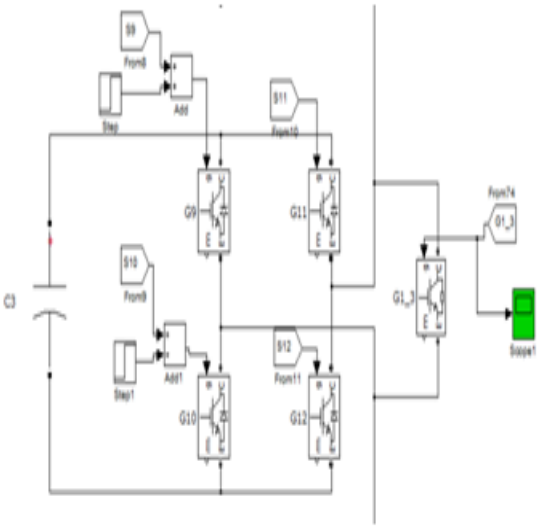


Fig. 7: Bypass switch (G1_3) placement with switch fault in G9 and G10 switches

G1_1 to G1_6 are the gate signals of the six bypass IGBTs provided at each cell which can be seen in figure 7.

The time interval from 0sec to 0.1sec is less load condition without STACOM [5], the time interval from 0.1 to 0.2sec is heavy load condition without STATCOM. The STATCOM is connected to grid through circuit breaker which operates at 0.2sec compensating the reactive power and eliminating the voltage sags in the load side. The complete system diagram is shownin figure 8 with STATCOM connection.

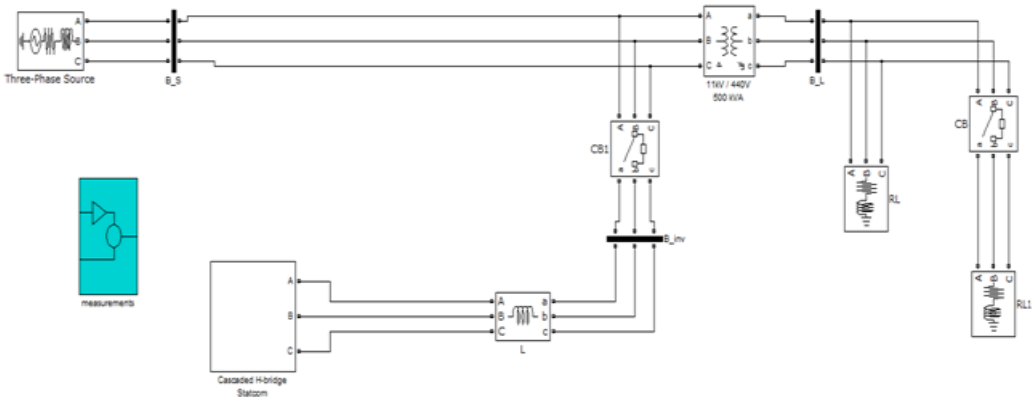


Fig. 8: Grid connected 13-level SVPWM controlled STATCOM

With relay switch ON signal, the bypass switch in any of the cell (faulty cell) is turned ON skipping the faulty cell of the cascaded H-bridge and bypassthe fault in the STATCOM. This elimination of the cell in a phase protects the grid connected devices during the fault in the STATCOM.

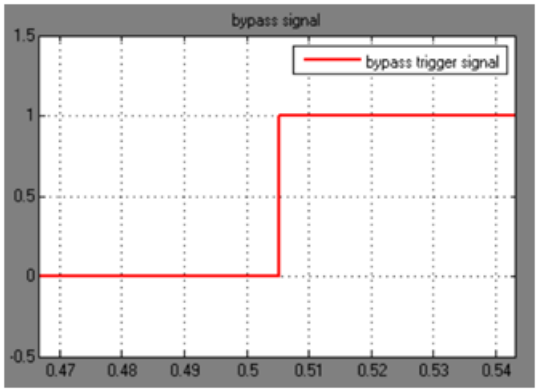


Fig.9: Relay Operational signal during open circuit fault

In Fig.10 graphical representation, the load voltage phase A in closed circuit has no much effect with and without the detection and mitigation control [6], but in the open circuit condition the load voltage profile is much better with the control bypass operation compared to without controller.

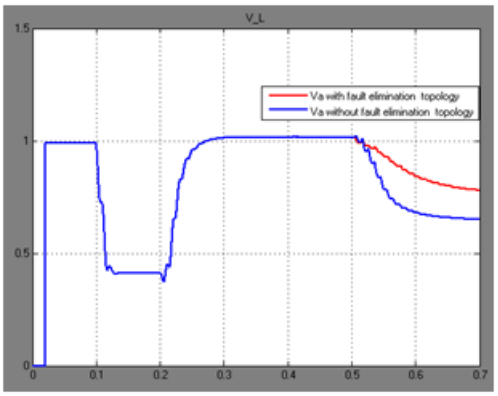


Fig. 10: magnitudes of phase A load voltage

The THD comparison of the proposed topology with and without the controller is shown in figure 11. The pu load voltage of A phase is improved to 0.82 from 0.66 during the switch fault and the THD is improvised to 17.06% from 19.6%. The voltage drop has been reduced as well as the harmonic distortion is reduced.

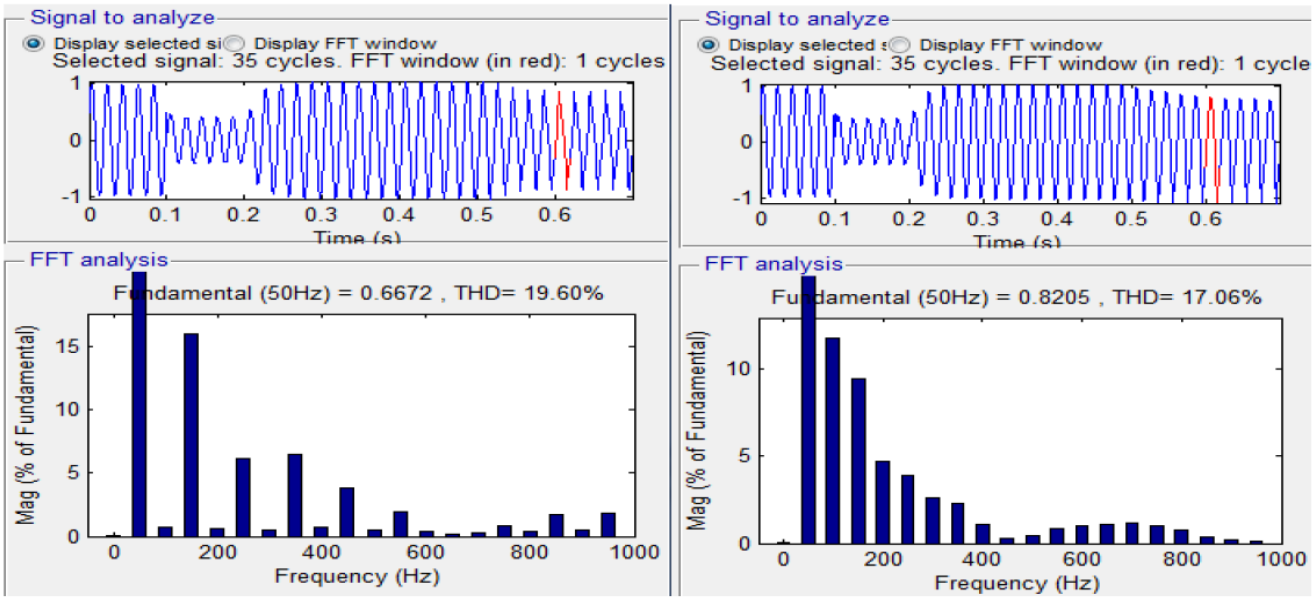


Fig. 11: THD comparison during open switch fault with and without detection and mitigation controller

IV. CONCLUSION

With the above analysis and implementation of 13-level STATCOM controlled with SVPWM during open and closed switch fault conditions, it is clear that the load voltage profile is maintained with low voltage sag and reduced THD (total harmonic distortion) during the fault time. The bypass switch operates with relay signal generated just 3.5sec after the fault, making the controller efficient and reliable.

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