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Design of Bootstrap Sample and Hold Circuit

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Abstract: ***This paper describes the design and implementation of open loop sample and hold circuit using bootstrap technique, which can be used as front end sampling circuit for high speed analog-to-digital converters. Different design criteria viz. speed, power, resolution, linearity, noise and harmonic analysis have been dealt with. Both theoretical analysis and simulation results are carried out. The bootstrap circuit is designed and then compared in a 0.18µm and 0.35µm CMOS process. It is observed that signal to noise and distortion ratio (SNDR) and effective number of bits (ENOB) are higher for 0.35µm technology. But these advantages are at the cost of higher power dissipation. Hence there exists a trade-off between these performance metrics.***

Keywords : sample and hold, bootstrap.

I. INTRODUCTION

Most analog-to-digital converters (ADC) typically employ a sample-and-hold circuit at the front end that must achieve high speed, high linearity and high precision with low-power dissipation. S/H circuit architectures can roughly be divided into open-loop and closed-loop architectures. The main difference between them is that in closed-loop architectures the capacitor, on which the voltage is sampled, is enclosed in a feedback loop, at least in hold mode. For high-speed sampling, open-loop schemes are fundamentally better suited than closed loop schemes because closed-loop sampling techniques require quality amplifiers (Op-Amps) that are stable and fast. Hence, the maximum sampling rate is limited by the gain-bandwidth product of the amplifier [1]. Conversely, open-loop sampling does not require an amplifier with stability restrictions, resulting in sampling networks with greatly reduced time constants compared to their closed-loop counterparts.

Open-loop architectures such as source-follower-based T/H (track-and-hold) have been reported in high-speed ADCs [2,3] in which the need for high bandwidth precludes the use of closed-loop designs. Furthermore, these architectures tend to consume lower power than closed-loop ones. State of art open loop 103MHz S/H circuit has been designed in [4]. Miller capacitance technique has been used in open loop configuration S/H circuit [5]. Some of the references are used in studying the behavior of S/H circuits. Analysis of open loop track and hold circuits has been referred in [6]. Dynamic Power dissipation of sampled circuits has been estimated in [7]. Several attempts have been made to reduce non-linearity issues in these circuits including clock boosting [2] and using dummy switches [3].The work done in here deals linearity issues and is intended for the realization of S/H circuit presented in [8].

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II. S/H ARCHITECTURE

Architecture of the S/H circuit is shown in Fig.1 [8]. Operation of the S/H is as follow, in sampling mode S1, S2 and S3 are closed and buffers track differential input as sampling capacitors are charged. At sampling moment, first S1 opens and after that S1 opened completely then S2 and S3 open, this cause true differential sampling. This means that sampling moment determined by one switch (S1), then S4 and S5 was closed and S/H goes in hold mode. The fully differential structure and the single sampling switch, eliminate any timing mismatch.

Using NMOS switch as S2 and S3 will cause the input-dependent on-resistance and input-dependent charge injection. As input changes, Vgs of NMOS switch changes too. These variations in Vgs of NMOS switch cause the input-dependency of on-resistance and charge injection. To avoid these problems instead of S2 and S3 switches we have used bootstrapped switch that is shown in Fig. 2.

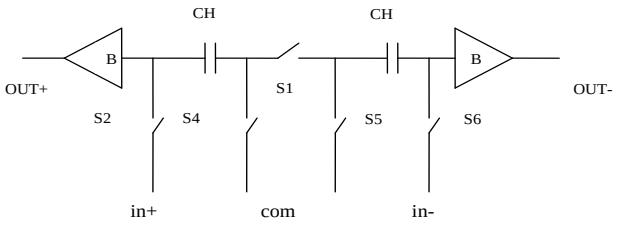


Figure 1 Open loop S/H architecture.

III. SAMPLING NETWORK

The sampling network consists of a sampling switch Ms and a hold capacitor *Cs* to store the value of sampled signal during the hold mode. During the tracking phase, the combination of the switch and the capacitor forms a first order RC network, the time-constant of which sets the maximum achievable sampling frequency. The speed of sampling network appears not to be a serious limitation in this work because as will be seen the chosen operating frequency is far less than the time-constant of the switch network and is basically limited by other parts of the circuit. The noise contribution due to the sampling network is dependent on the sampling capacitance

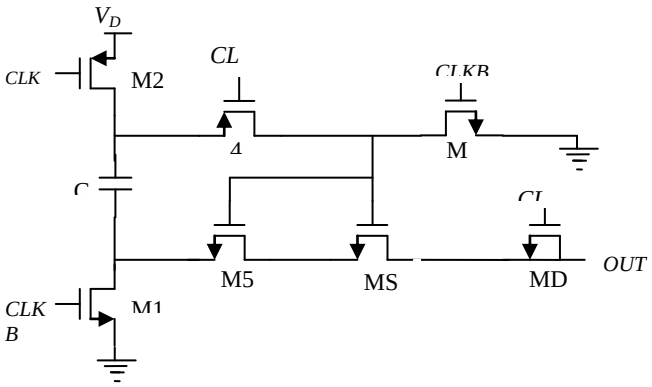


Figure 2 Bootstrap switch circuit.

value and the width of the switching transistor. The total noise during the track mode is given by:

$$\overline{V_{on,t}^2} = \frac{KT\gamma}{C_L + C_{gs} + R_{sw,on} g_m C_s} + \frac{KT R_{sw,on}}{C_s R_{sw,on} + \frac{C_L}{g_m}}$$

where Rsw,on is the resistance of the switch during the track mode, is the excess noise factor for the given technology and Cgs and CL are the gate-source capacitance of the source follower and the load capacitance of the circuit, respectively. From this equation it is apparent that a larger value of CS would lower down the noise. In addition to the noise added by the switch, the nonlinearity due to the signal-dependent behavior of the switch can degrade the overall linearity of the T/H circuit. The on resistance of a long-channel MOS device operating in the linear (triode) region is given by:

$$R_{sw,on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})}$$

where V_{th} is the threshold voltage, V_{GS} is the gate-source voltage of the transistor during the track phase and *W* and *L* its width and length, respectively. If no precaution is taken to keep V_{gs} independent of the input signal, the resulting on resistance would lead to substantial non-linearity while the circuit is in track mode. Another consequence of varying V_{GS} *is* that the charge injection at the onset of the hold mode would be a function of the input signal, which in turn can cause additional non-linearity.

IV. BOOTSTRAPPED SWITCH CIRCUIT

In this switch, V_{GS} stays constant and does not have input-dependency problems[9,10]. Operation of the circuit is as follow; when *CLK* is low, M1 and M2 are on and C charges to V_{DD}. Also M4 is on and connects the gate of Ms to *GND* that cause, Ms to be off. When *CLK* is high M3 is on and through M5, V_{IN} applies to C. So the overall voltage on C is V_{DD} + V_{IN}. This voltage is also the gate voltage of MS that causes V_{GS} of Ms Stays constant and be independent of input

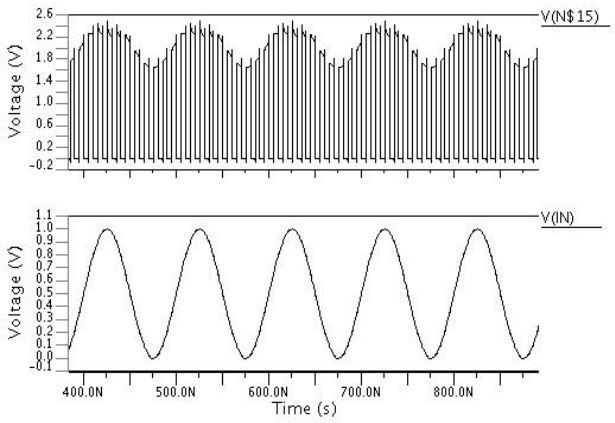


Figure 3 Simulated gate voltage and input voltage of switch.

voltage. Dummy transistor MD is used to eliminate the constant charge injection of Ms.

V. SAMPLING SWITCH CLOCK-BOOSTING

A clock-boosting circuit was implemented in this design to avoid the variations due to non-constant V_{gs} in the resistance of the switch during the track mode. During the hold phase, transistors M1, M2 & M4 conduct while M3, M5 & Ms are off. The gate of Ms is also shorted to ground by M4 to ensure that the sampling capacitor is disconnected from the input. It is clear from this equivalent circuit that the boosting capacitor would be charged to the potential of the source of M2 in this phase of operation. During track phase, *CLK* is high, thereby turning M1−2 and M4 off and M3, M5 on. As a result C will be connected across gate-source terminal of the switch. The overdrive voltage of the switch in track mode is thus independent (approximately) of the input signal. The value of the clock-boosting capacitance should be chosen with care. In high speed applications, the capacitor should be small enough to be able to charge to V_{DD} within a half-cycle of clock. The minimum value of this capacitor is determined by the parasitic capacitances in the circuit. C along with the parasitic capacitances of the gate of the switch will form a capacitive divider. The fraction of V_{DD} which appears across the switch is thus [9]

$$V_{gs} = \frac{C}{C + C_p} V_{DD} - \frac{C_p}{C + C_p} V_{in}$$

Therefore, if the clock-boosting capacitor is chosen to be small the effect of parasitic capacitors in the design would be more pronounced. Equation further shows that parasitic capacitances can create input-dependent variations in the gate source voltage; therefore, a larger value of C would improve the linearity, as well.

Figure 4 depicts a single-ended schematic of the T/H circuit designed in this work. The circuit consists of a sampling network, its associated clock-boosting circuit, and a PMOS source-follower.

The T/H is implemented in a differential fashion to suppress even-order nonlinearities as well as offset and common-mode noise. The biasing branch of the source-followers is, .

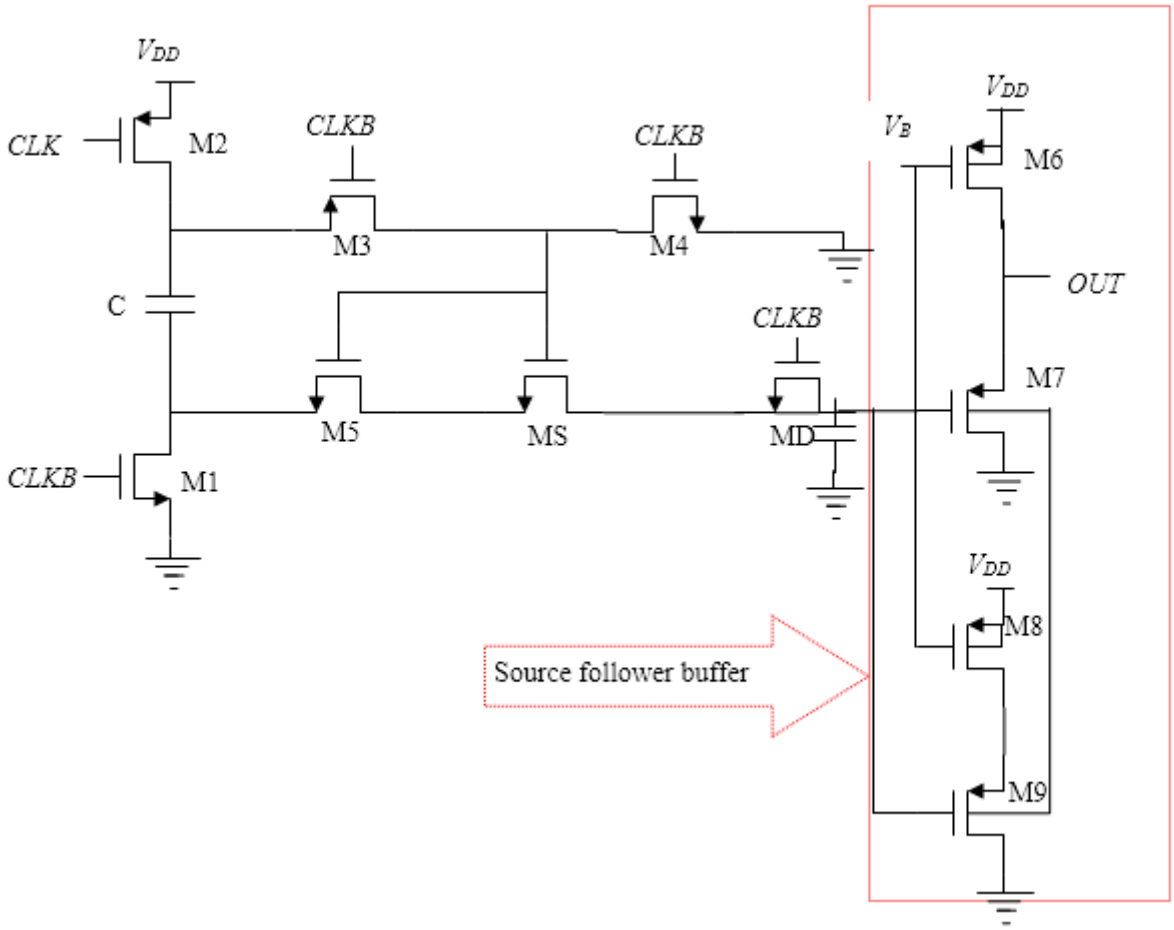


Figure 4 Schematic of single ended open loop bootstrap circuit.

however, shared between the two half circuits to cancel the noise contribution of biasing devices.

VI. TRANSISTOR SIZING

The sampling switch Ms transistor size is most critical from channel charge injection and low point of view. If the size of the sampling transistor is large then it will result in an increased charge-injection at the output. On the other hand in order to have lower value of the size of the sampling transistor should be larger.

The next most important transistor in the design is M3 from sizing point of view. This transistor allows appearing as gate voltage for the sampling transistor. So the propagation delay of this transistor should be as small as possible. Secondly it is a *PMOS* device so its width should naturally be larger as compared to *NMOS* devices to compensate for lower charge mobility and hence speed of the transistor. On the other hand by increasing the size of the transistor, parasitic capacitances associated with the upper plate of the boosting capacitor will reduce the gate voltage of sampling switch as described by Eq. above.

The sizes of *Cs* and C_L have been kept to 1pF to have low KT/C noise. The sizing strategy of has already been discussed above which is also quite critical from performance point of view.

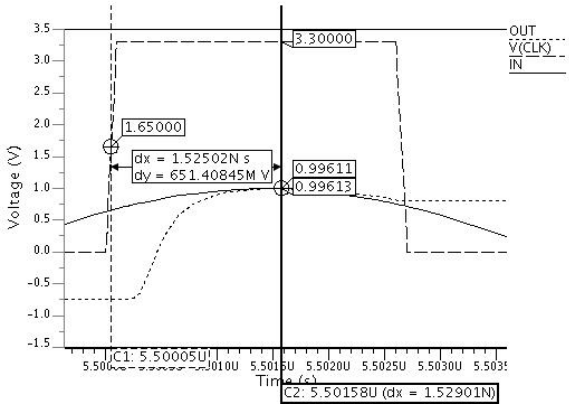
Table 1 Width of transistors used in the circuit.

TRANSISTORS	W/0.35µm	W/0.18µm
M1	1 µm	0.5µm
M2	3µm	1.5µm
M3	3µm	1.5µm
M4	1µm	0.5µm
M5	1µm	0.5µm
M6	40µm	47µm
M7	40µm	47µm
M8	4µm	4.7µm
M9	4µm	4.7µm
Ms	12.57µm	6.65µm
MD	6.47µm	3.35µm

VII. SIMULATION RESULTS

The designed T/H circuit was simulated in CMOS 0.18µm and 0.35µm BSIM3v3 model technology. The values of load capacitor CL and capacitor Cs are chosen as 1pF and 1pF, respectively. The performance metrics are simulated and compared for both the technologies.

The charge injection is corrected to the first order by introducing differential topology as it appears as a common-mode disturbance. The charges introduced by two switches in a differential topology do not exactly cancel each other. The overall error is however suppressed for differential signals because this technique removes constant offset and



lowers the non-linearity component.

Figure 5 Waveform for acquisition time measurement of bootstrap S/H circuit.

Acquisition time is the delay in time when a track-and-hold circuit enters the tracking mode and tracks an input signal with certain accuracy. Ideally speaking the sample-and hold circuit should immediately start tracking the input signal as the clock phase goes high or to value as in this case of the bootstrapped switch. Acquisition time can be used as a measure of on resistance and hold capacitance for maximum allowable sampling frequency. The acquisition time increases with reduced technology for the same capacitive load. Fig 5 shows the acquisition time measurement of bootstrap circuit at 0.35µm technology on Mentor Graphics ELDO.

The circuit achieves a SNDR of greater than 10-bit resolution at sampling rate of 200MHz, while consuming less than 4mW of total power with both the circuits implemented with 2Vp-p differential input. Figures 6 and 7 show the frequency spectrum at 40MHz input frequency for 0.35µm and 0.18µm technology of bootstrap circuit.

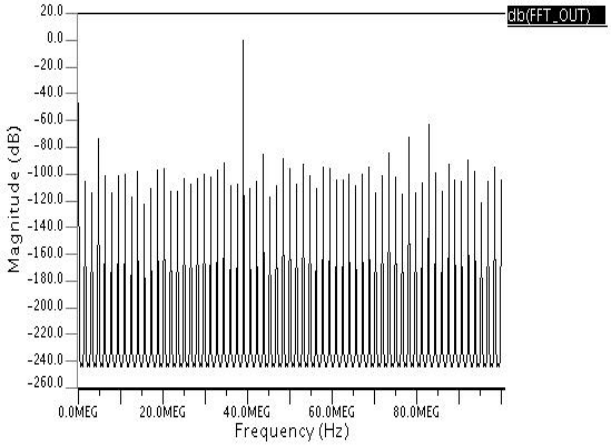


Figure 6. FFT spectrum at 40MHz input frequency at 0.35µm technology of bootstrap S/H

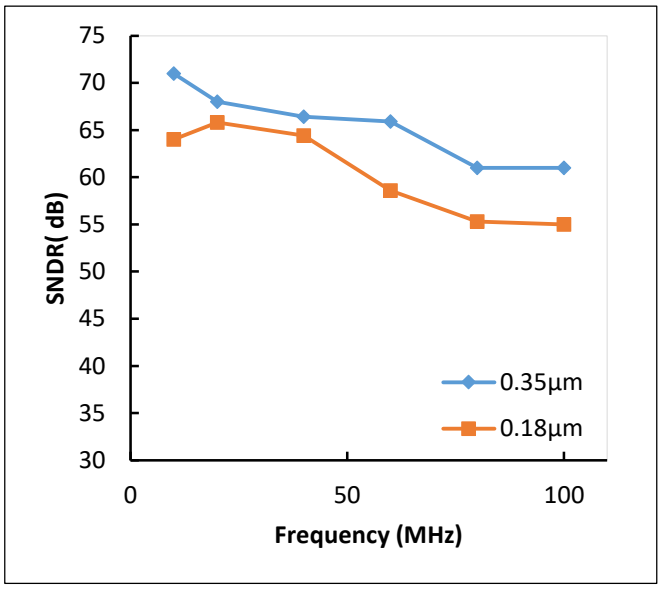


Figure 7 SNDR performance of bootstrap S/H circuit.

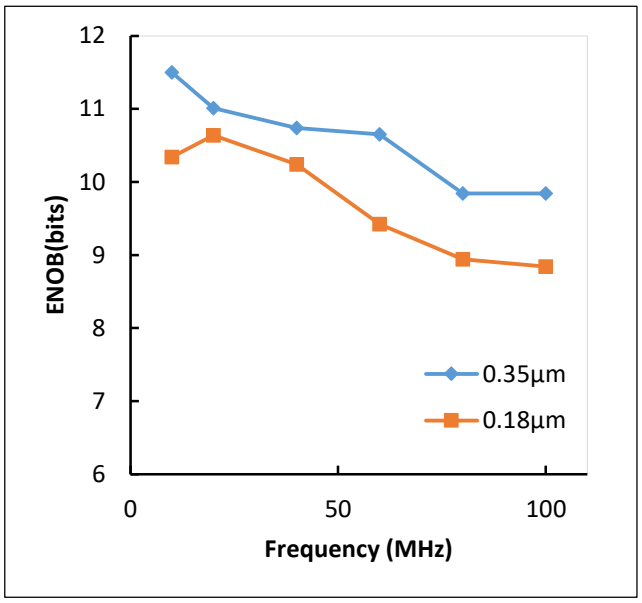


Figure 8 Effective number of bits variation with frequency of bootstrap S/H circuit.

The above FFT graph shows the spurs 0.35µm technology which are greater than are in 0.18µm technology. Harmonics are greatly suppressed because of differential topology. The variations in threshold due to bulk biasing in buffers cause increase in distortion. The signal dependent threshold voltage of the MOS device would still introduce non-linearity into the system. Furthermore, it should be noted that in addition to the variations in V_{GS}, other factors exist which cause variations in the switch resistance such as the dependence of onresistance on the drain-source voltage of the device thereby increasing the distorion. Simulation results demonstrate the variation of SNDR over the Nyquist frequency range.

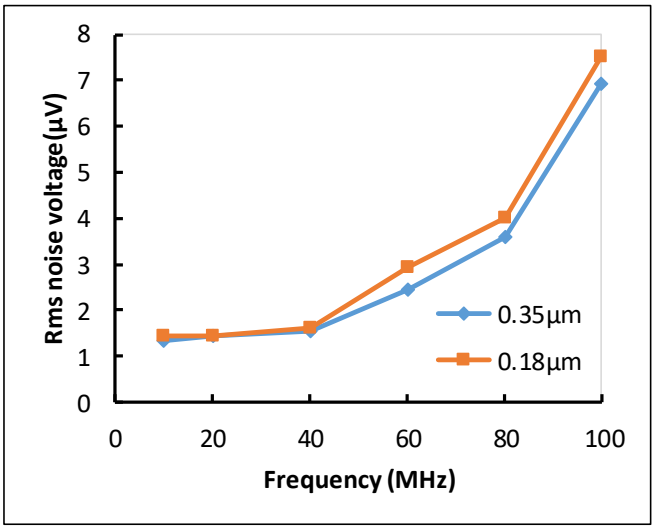


Figure 9 Rms noise voltage variation with frequency of bootstrap S/H circuit.

Figures 7 and 8 shows the SNDR, effective number of bits (ENOB) variation with the varying frequency (f), rms noise voltage variation with frequency (f). Table 2 gives the various performance metric for the bootstrap S/H circuit.

Table 2 Performance metrics of bootstrap S/H circuit.

Simulated parameters	0.35μm	0.18μm
Supply voltage	3.3V	1.8V
Power dissipation	4.68mW	2.34mW
Acquisition time	1.52ns	1.72ns
SNDR	61dB	55dB
Effective Resolution	9.84 bits	8.94 bits

It is observed that SNDR and ENOB are higher for 0.35μm technology. Maximum SNDR is 61dB and maximum ENOB is 9.84 bits for 0.35μm technology. Figure 6.6 shows that rms noise is nominally lesser for 0.35μm technology. But these advantages are at the cost of higher power dissipation as the supply voltage is higher in case of 0.35μm technology. Hence there exists a tradeoff between these performance metrics.

VIII. CONCLUSION

A highly-linear high-speed CMOS S/H circuit has been implemented for 0.35μm and 0.18μm and discussed. A comparison at two technologies has been done. This design uses clock boosting and linear operation to achieve a SNDR of greater than 10 bit resolution at 200MS/s with a 2V FSR since most of the dynamic figures are met the bootstrap sample-and-hold circuit is suitable for the single-chip integration with low-voltage application. Also, this architecture with some modifications can be used for low-voltage pipelined A/D converter.

REFERENCES

1. P.R.Gray and R. G. Meyer, “Analysis and design of analog integrated circuits”, 4th ed, John Wiley & Sons Inc., 2005.
2. M. Waltari, K. Halonen, “1.0-Volt, 9-bit Pipelined CMOS ADC,” in proc 26th European Solid-State Circuits Conference, pp. 360–363, Sep. 2000.
3. L. Sumanen, M. Waltari, K. Halonen, “A 10-bit 200 MS/s CMOS Parallel Pipeline A/D Converter,” IEEE J. Solid-State Circuits, vol. 36, pp. 1048–1055, Jul. 2001.
4. Kh. Hadidi, “Open loop 103MHz -61 dB THD S/H circuit “1998 IEEE.
5. Peter J. Lim, “A High-speed Sample-and-Hold Technique Using a Miller Hold Capacitance,” IEEE journal of solid-state circuits, vol.26, no.4,pp. 169-172, April 1991.
6. Peter Harpe, “Analysis of Open Loop Track-and-Hold Circuits” 2007 IEEE.
7. Hiroyuki Sato, “Dynamic power dissipation of track/hold circuit ” 2000 IEEE.
8. Mahmoud Sadollahy, “A High-Speed Highly-Linear CMOS S/H Circuit ” Proceedings of the ICCCE, pp. 550-554, May 13-15, 2008.
9. Renyuan Huang and Chin-Long Wey,“A High-Accuracy CMOS Oversampling Switched-Current Sample/Hold (S/H) Circuit Using Feedforward Approach,” IEEE transactions on circuits and systems—ii:analog and digital signal processing, vol.45, no 3, March 1998 .
10. Kenji Ohno, “A Switched-Voltage High-Accuracy Sample/Hold Circuit,” The 47th IEEE International Midwest Symposium on Circuits and Systems .1994