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Design and Simulation of Error Amplifier used in Power Management chips

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Abstract:This paper discusses the design procedure of error amplifier, which is used in the power factor correction circuit built with dc-dc Boost converter. The error amplifier is the heart of the power management IC's which indicates the accuracy of the entire circuitry. The specifications are considered which is suitable for power management applications. The gain of the amplifier is chosen to be 60db, UGB of 75MHz, slew rate of 50V/uS, PM greater than 60', technology 180nm. The design is simulated using tsmc 180nm technology with Analog Device's LT-SPICE simulator.

Keywords: CMOS opamp, error amplifier

I. INTRODUCTION TO ERROR AMPLIFIERS

In all power management ICs, there will be a negative feedback system that will perform the desirable control actions using operational amplifiers. The control ICs for power factor corrections make use of error amplifiers for the generation of the necessary template for shaping the input current. The functional block diagram is shown in Figure 3.1 where in, an error amplifier [1] compares the output voltage with a reference generating the required magnitude of the error signal. The error signal, being the function of variation in output voltage, is multiplied with the sinusoidal current template thereby the magnitude of the current template is set. The current template so generated is compared with a ramp signal in an op-amp to generate the necessary gate signals for the converter. From the above discussion it is very clear that operation amplifiers are essential components in any power management ICs. The ability of the controller to shape the input current in the form of a sine function is governed by the specifications of op-amps such as DC gain, UGB, slew rate, PSRR, CMRR. The error amplifiers used in commercial chips are not optimized and the design guidelines are often proprietary in nature. The present scope of the research is to design a power factor controller with all the necessary control features. In this paper, guidelines [2] to design an error amplifier with the desirable specifications is presented.

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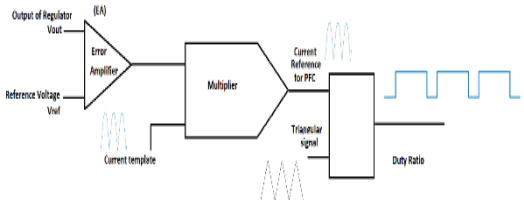

Figure 1 Block diagram for usage of op-amp as error amplifier in gate signal generation

An operational amplifier (Opamp) is a DC coupled high gain electronic voltage amplifier with a differential input and usually, a single-ended output. They are employed from dc bias applications to high speed amplifiers and filters. General purpose Opamps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications.

Opamps are characterized by a large number of mutually conflicting performance specifications with variable priorities which depend on the Op-Amp functionality within the analog system. For example, Opamps used as comparators in ADC are primarily required to have high slew rates, small input offsets, and restricted area and power dissipation [3]. In contrast, Op-amps (error amplifiers) used negative feedback configurations have to be compensated to achieve high gain, and good phase margins with better cross over frequency.

The analog circuit designer need to follow several steps/phases in designing an Op-Amp[4]. In the first phase, the designer considers the intended application of the Op-Amp, sets the performance specifications, and decides upon an appropriate circuit topology. In the second phase, the topology[5] is sized and biased using analytical first order design equations. In the third phase, the design is evaluated and optimized by adjustments of the design parameters and repeated circuit simulation.

II. BASIC STRUCTURE OF TWO STAGE OPAMP

Figure 3.2 shows the block diagram for a two stage opamp. The first stage consists of differential amplifier [6] [7], followed by the second stage which is a common source amplifier. A differential amplifier being a single stage opamp with single pole role off, has insufficient gain for any practical applications in power management IC's. Hence two stage operational amplifiers are needed to boost the gain so as to meet the requirement. The basics of two stage opamps are discussed in further paragraphs, highlighting the design aspect.

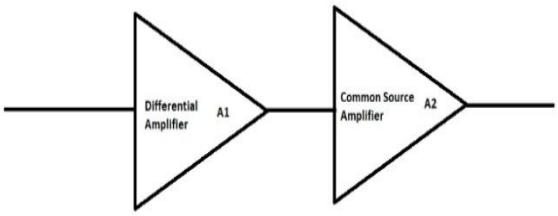

Figure 2: Block diagram of two-stage CMOS opamp

III. BIASING OF THE MOS AMPLIFIERS

In order to ensure proper/faithful amplification of signals, all the transistors in an amplifier are required to operate in the saturation region over the range of the input voltage swings. Otherwise, the output will suffer from clippings leading to distortion. The transistor should not enter into linear or cutoff region. To achieve this, the designer should bias the all the transistors in the saturation region irrespective of the input voltage swings [8]. Biasing is a technique to satisfy all the above conditions. There are many methods of biasing the MOSFETs out of which biasing using current mirror is to be used for on chip amplifiers. Current mirrors [9] are also used in comparators, regulated current sources, in addition with amplifiers. In very complex circuits, simple current mirrors are also used to minimize transistors count. Its function is to replicate accurately an input current. Most of the time, a current mirror is designed to give high output impedance and an output relatively free from noise. The following few paragraphs explain the basics of current mirrors starting from drain current equations.

A. The Basic Current Mirror

The ideal "two-transistor" current mirror shown in Figure 3.3 consists of matched transistors M1 and M2. M1 is diode-connected transistor and it is used to define the gate-to-source voltage of M2 [4] .This produces an output current Iout identical to the input current Iref. Normally, M1 and M2 operate in saturation and the gate-to-source voltage Vgs of M1 and M2 are same.

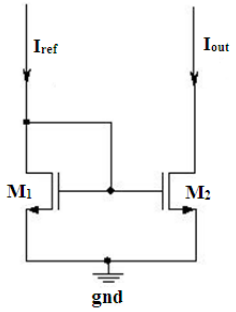

Figure 3: Basic Current mirror circuit

The drain current expression for the transistor M1 operating in saturation is given by equation 1

$$Iref = \frac{Kn'}{2}\ (\frac{W1}{L1})(Vgs - Vth)^2 \qquad (1)$$

Similarly, $Iout$ is related to VGS as:

$$Iout = \frac{Kn'}{2}\ (\frac{W2}{L2})(Vgs - Vth)^2 \qquad (2)$$

where Kn' is the process related parameter approximately given by $\mu nCox$.

By taking the ratio of Iout and Iref, the following equation is obtained.

$$\frac{Iref}{Iout} = \frac{\frac{W1}{L1}}{\frac{W2}{L2}} \qquad (3)$$

From the above equation, it can be claimed that the electrical ratio is expressed in terms of the device dimension ratio [7]. By setting the (W/L) ratio of both the transistors equal Iout is made to track the Iref. Hence the name current mirror. In the circuit of opamp, such current mirrors are used with nmos and pmos pairs.

B Design Procedure for the opamp

After understanding the current mirror biasing concepts, the design procedure of opamp may be started. The design procedure begins by choosing the (W/L) ratio for each transistors so that to keep all of them in saturation region for proper amplifier operation. As it is the primary requirement in most of the analog circuit design, [10] in contrast to digital circuit, the transistor should be switched between cutoff and linear mode, hence no problem of channel length modulation. The different characteristics of the Op-Amp are defined by different stages transistors, which are to be satisfied using the design equations. The step by step design procedure for opamp is discussed in following paragraphs. The circuit of opamp is as shown in figure 3.4, same names of the transistors is continued for their respective width length ratio.

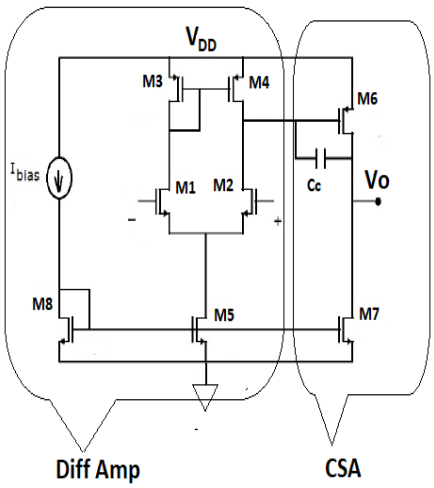

Figure 4 Two stage opamp circuit [ref]

The design starts with the specifications which are listed below, for typical gain of 120 db specifications are shown.

DC gain=80 db
UGB= 75 MHz
Phase Margin >= 60'
Slew rate = 50 V/u Sec
CL = 2 pF
Process = 180nm
VDD = 5 V
Lmin = 180 nm

First step is to write the small signal model [11] for the circuit, where a transistor is represented as voltage controlled current source, applying the small signal conditions (all dc voltages, currents is taken as zero for the purpose of building the small signal model). Figure 3.5 shows the small signal model [11] for two stage opamp.

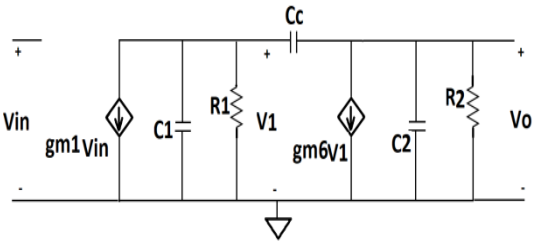

Figure 5 small signal model for two stage opamp

The transfer function of the two stage is opamp is given by 4.

$$\frac{Vo}{Vin} = \left(\frac{V_1}{V_{in}}\right)\left(\frac{V_o}{V_1}\right) \qquad (4)$$

$$\frac{Vo}{Vin} = \frac{gm1R1gm2R2\left(1-\frac{sCc}{gm2}\right)}{s2[R1R2(C1C2+C1Cc+C2Cc)]+S[R2(Cc+C2)R1(Cc+C1)+Ccgm2R1R2]+1} \qquad (5)$$

By setting jω=0 at s=0, the DC gain can be obtained. The numerator and denominator of the transfer function equation represents the zeros and poles of the system respectively [6].

$$\frac{Vo}{Vin} = \frac{Adc\left(1-\frac{s}{z}\right)}{\left(1+\frac{s}{p1}\right)\left(1+\frac{s}{p2}\right)} \qquad (6)$$

By comparing with the transfer function represented by 6 with 5, the following equations are obtained.

The dc gain is given by the expression Adc shown in.7

$$A_{dc} = (g_{m1}R_2)(g_{m2}R_1) \qquad (7)$$

Where g_{m1} and g_{m2} are the transconductances of the MOSFET M1 and M2 respectively.

The position of the first pole frequency or 3db frequency is given the equation 3.8

$$p_1 = \frac{1}{g_{m2}R_2R_1C_c} \qquad (8)$$

The second pole frequency is given expression p2.

$$p_2 = \frac{g_{m2}}{C_2} \qquad (9)$$

The zero frequency is given by 10

$$z = \frac{g_{m2}}{Cc} \qquad (10)$$

where Cc is the Miller capacitance.

The unity gain bandwidth of the opamp is given by 11

$$UGB = \frac{g_{m1}}{Cc} \qquad (11)$$

Slew rate is the ratio of tail current and Miller capacitance, which is given by 12

$$Slew\ Rate = \frac{I_5}{Cc} \qquad (12)$$

To have phase margin of 45', the value of Miller cap [10] to be chosen as 0.11CL, for the value of Miller cap is to be 0.22CL. This condition derived by considering phase angle of the transfer function $\frac{V_0}{V_{in}}$. Now by considering the specifications of the opamp the W/L ratios of the transistors can be designed. The sentences need to be revised to suit technical presentation

Assumptions: g_{m1}=g_{m2} (Transconductance of first stage),

g_{m6} (Transconductance of second stage)

$$Slew\ Rate = \frac{I_5}{Cc} \qquad (13)$$

First stage gain,

$$Av1 = -\frac{g_{m1}}{g_{ds2}+g_{ds4}} = -\frac{2g_{m1}}{I_5(\lambda_2+\lambda_4)} \qquad (14)$$

Where gds2 is the inverse of ro2

Where gds4 is the inverse of ro4

Second Stage gain,

$$Av2 = -\frac{g_{m6}}{g_{ds6}+g_{ds7}} = -\frac{g_{m6}}{I_6(\lambda_6+\lambda_4)} \qquad (15)$$

where gds6 is the inverse of ro6

where gds7 is the inverse of ro7

Unity Gain bandwidth, UGB $= \frac{g_{m1}}{C_C}$ (16)

Output Pole, $P_2 = \frac{-g_{m6}}{C_L}$ (17)

RHP Zero, $Z_1 = \frac{g_{m6}}{C_C}$ (18)

Positive CMR,

$$ICMR+ = V_{DD} - \sqrt{\frac{I_5}{\beta 3}} - |V_{T03}|(\max) + V_{T1}(\min) \qquad (19)$$

Negative CMR,

$$ICMR- = V_{ss} - \sqrt{\frac{I_5}{\beta 1}} - |V_{T1}|(\max) + V_{DS(sat)} \qquad (20)$$

Saturation Voltag $V_{DS(sat)} = \sqrt{\frac{2I_{DS}}{\beta}}$ (21)

C Miller compensation:

Prediction and control of the response of the opamp discussed is difficult due to the presence of many poles contributed by various RC networks[12] .

It is observed that the system's response is principally governed by two dominant poles contributed by the differential pair and the common source stage. The system design involves compensation in such a way that the opamp is governed by a single pole within the required UGB [13].The most widely used compensation technique is undoubtedly the pole splitting method where a Miller capacitor is used to split the poles, pushing the dominant pole to a much lower frequency thereby reducing the bandwidth and providing ample stability [14].

According to Miller Theory [4], a capacitor is connected between differential stage and inverting stage results in huge input capacitance which is governed by $C_{in} = C_c(1 + |Av_2|)$ and also gives an output capacitance given by $C_{out} = C_c(1 + \frac{1}{|Av_2|})$ which is almost equal to Miller capacitance. (Cc which is shown in figure 3.4 & 3.5). This leads 1st stage pole moving towards origin, and 2nd stage pole moving outwards results in a single pole system. The Miller capacitor which is connected between an input and output of inverting stage results in RHP zero (equation 15). The effect of RHP zero is nullified using a resistor in series with the Miller capacitance, which is equal to inverse of transconductance of inverting stage . (gm of M6)

Table below shows the W/L ratios of all the transistors designed using the design equations 10 to 21.

Table 1 Designed (W/L) ratios of the error amplifier

Transistor	W	L
M1	5µm	1 µm
M2	5 µm	1 µm
M3	14 µm	1 µm
M4	14 µm	1 µm
M5	12 µm	1 µm
M6	173 µm	1 µm
M7	75 µm	1 µm
M8	12 µm	1 µm

IV. RESULTS AND DISCUSSIONS

The simulation results have been obtained for the circuit in 180 nm CMOS technology using Analog Device developed LT-SPICE[15]. Figure 6 shows the circuit implemented using LT-SPICE. The design is simulated for various characteristics, which are plotted in following figures.

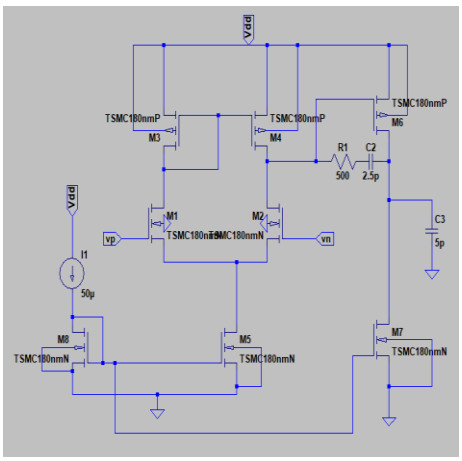

Figure 6 op-amp simulated using LT-SPICE

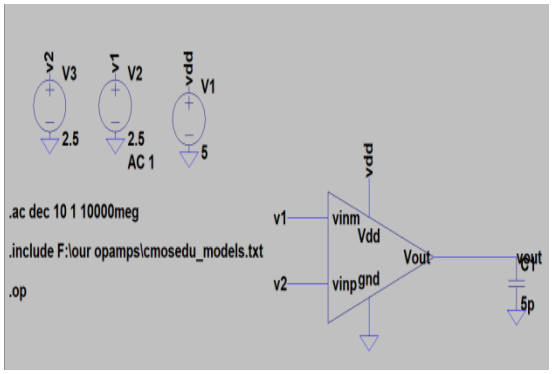

Figure 7 Set up to find gain & UGB

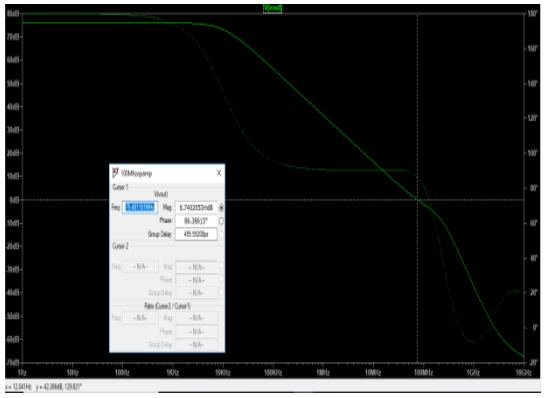

Figure 8 Simulated results Gain=78db and UGB=75MHz

Figure 7 shows the set up required to calculate the DC gain and the gain bandwidth. The simulated results is shown in figure 8, the gain is found to be 78db at zero frequency and unity gain bandwidth is 75MHz

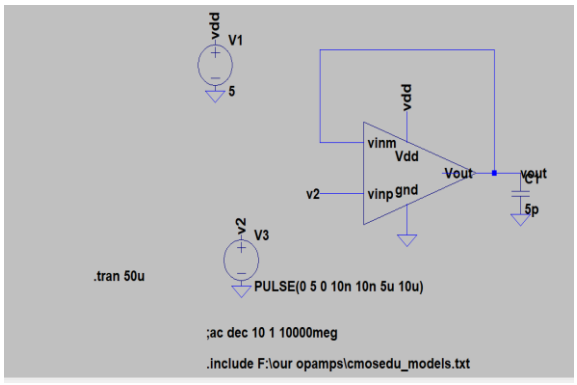

Figure 9 Set up find slew rate

Figure 10 Simulated result of slew rate = 54V/uS

Figure 9 shows the set up required to calculate slew rate of the opamp. [10] The slew rate indicates how better the opamp can track the changes in the input signal. The simulated results is shown in figure 10, the slew rate is found to be 54 V/µS.

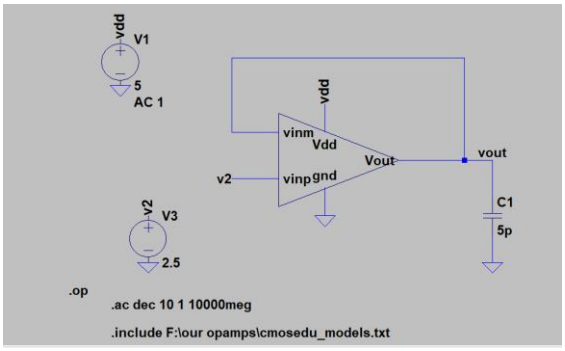

Figure 11 Set-up to obtain PSRR

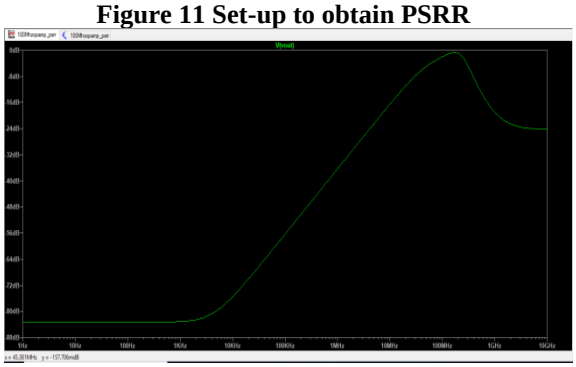

Figure 12 Simulated results of PSRR = -83db

Figure 11 shows the set up required to find the PSRR of the opamp. The PSRR indicates ability of the opamp to reject the supply noises. The simulated results is shown in figure 12, the PSRR [16] rate is found to be -83db.

V. CONCLUSION

As discussed in the paper, the error amplifier is the major analog building block which is used in the Boost power factor controller [2]. The op-amp used is a high DC gain amplifier, with typical gain values more than 60db, UGB of 75MHz, PSRR of -83db, slew rate of 54V/uS which is sufficient to make the system errors low. The paper also highlights the stability issues of the controller which is summarized in by taking Miller compensation.

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