International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-4, November 2019

Artificial Intelligence Algorithmic Based Fault Tolerance with OLC Codes for Parallel Fault Detection and Correction FFT Soc Design

Raju Katru, M.Chandrasekher

Abstract: ***Different errors are attacks the VLSI SoC designs these are harm to Mathematical operations and obstacles to results because of this soft core errors are trending to screen. With the increase of information communication, sources of noise (SON) and interference and parallel processing, increases the fault tolerances so designers have been striving to achieve with the require for extra competent and consistent techniques for detecting and correcting faults in parallel "transmission_(TX)" and "reception_(RX)" of data. even if some methods and advances have been projected and apply in past years but information dependability in TX and TX is at rest a trouble. In this research we recommend a more efficient mutual "error_detection" & "correction_technique" stand on the Artificial intelligent algorithmic based fault tolerance (AIABFT) with parallel Orthogonal Codes, and vertical parity. With the help of proposed method designing a parallel processing faults detection and correction FFT. This AIABFT method has been experimentally executed and replicated using Xilinx_vivadoResults of the simulation indicate that the suggested method detects 97% of the mistakes and corrections as expected in the received impaired n-bit code up to (n/2-1) bits of mistakes***

Keywords: ***Artificial intelligent algorithmic based fault tolerance (AIABFT), OLS codes, parallel fault detecting FFTs, Xilinx.***

I. INTRODUCTION

When input is transferred via a pipeline (wired or wireless), the reliability of data may be affected by some noises due to this official information being changed this is called an fault. The recipient thus requires error detection and adjustment methods. One of scheduling methods that detects and corrects defective information is orthogonal code. Each k-bit set of information is transformed to n-bit "orthogonal code" in this technique. An OLC n-bit code includes n/2 1's andn/2 0's which implies this code's parity was always zero. We introduce a fresh methodology in this article to improve the orthogonal code's encryption capacity. This procedure is executing with VHDL and field programmable gate array (FPGA). With the rise in data transfer and thus noise and disturbance sources, technicians have really been fighting with the requirement for more effective and reliable methods to detect and correct mistakes in the information obtained. While several methods and methods have been suggested and implemented over the past century, there is still a issue with data reliability in communication. Thus, ED & EC methods are necessary. Most of these methods could only identify mistakes, like "Cyclic Redundancy Check"(CRC)[1-3]; others are intended to identify and right the mistakes, including Solomon Codes[4, 5], Hamming Codes[6], and Normal Orthogonal Codes (NoC)[7, 8]. Furthermore, current methods are not capable of achieving high effectiveness in error detection and correction as well as meeting bandwidth demands, particularly with an rise in the amount of transferred data. A method (NoC) combining the OCC and a method, Closest Match utilizing FPGA), has resulted in the enhancement of the NOC's detection capacities from 71.88 percent to 93.57 percent[9] in a prior job. We introduce an extended method (AIABFT) in this document which connects parity of Orthogonal Codes vertical to parallel FFT fault. The outcomes illustrate that the planned method augment both ED and EC capability of parallel processing fault detection with Orthogonal Codes.

Parallel keys are rated binarily and are equivalent to ones and zeros. An "orthogonal n bit" matrix has 'n/2' 1's and 'n/'2 0's. That implies there are "n/2" locations differing between ones & zero's. All OL codes will also produce 0 bits of parity. The primary motivation meant for orthogonal system is because they be not susceptible to next to_far impacts & since the "cross correlation" of every produced orthogonal code is 0, it is easy to detect corrupted code sequence[1]. The idea is demonstrated as shown in table-1 by an 8/bit orthogonal symbols. It includes orthogonal 8-bit codes and antipodal 8-bit codes. Because the orthogonal codes show in table-1, antipodal instructions were the opposite of orthogonal codes, each of them produces zero parity bit. In orthogonal coding techniques, a transmitter sends no parity bit as a "parity bit" is assumed to be zero.

Receiver, k-bit knowledge set is map into distinctive n/bit/orthogonal code. Wherever' n=2^(k-1)'. As an eg, a 4-bit knowledge place is delineated by a novel 8-bit/orthogonal code[d]. Orthogonality of every produced code is chequered by judgment the cross correlation by the antecedents generated codes. if the correlation is 0 then solely code is accepted otherwise repeat request is generated. This correlation method is ruled by the following eq[4],

Manuscript published on November 30, 2019.
* Correspondence Author
Raju Katru*, Ph D scholar in Rayalaseema University, Kurnool, Andhra Pradesh, India.
M.Chandrasekher, Manager(D&E), Bharath Dynamite Ltd, ,Khanchnbagh,Ministry of Defence,Hyderabad,India

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license http://creativecommons.org/licenses/by-nc-nd/4.0/

where a combination of n-bit frame X1,X2.... Xn and Y1,Y2... Yn ar evaluate to make eq(1)

$$R(x,y) = \sum_{i=1}^{n} Xi \cdot Yi < \frac{n}{4} - 1$$ -------EQ(1)

R(x, y) is the component of similarity. N/4 is the cutoff point of two orthogonal rules. This is provided by both the calculation below

$$d_{th} = \frac{n}{4}$$ ---EQ(2)

In which n is the duration of the system and dth is the roughly halfway limit of 2 orthogonal codes [1]. For 8/bit/orthogonal code, "dth=8/4=2".We add additional 1-bit compensate to equation for dependable identification. (1).

$$t = n - R(x,y) = \frac{n}{4} - 1$$ ---------- (3)

Table: 2 OLCODES and antipodal code

Orthogonal code									p	Antipodal code									p
0	0	0	0	0	0	0	0		0	1	1	1	1	1	1	1	1		0
0	1	0	1	0	1	0	1		0	1	0	1	0	1	0	1	0		0
0	0	1	1	0	0	1	1		0	1	1	0	0	1	1	0	0		0
0	1	1	0	0	1	1	0		0	1	0	0	1	1	0	0	1		0
0	0	0	0	1	1	1	1		0	1	1	1	1	0	0	0	0		0
0	1	0	1	1	0	1	0		0	1	0	1	0	0	1	0	1		0
0	0	1	1	1	1	0	0		0	1	1	0	0	0	0	1	1		0
0	1	1	0	1	0	0	1		0	1	0	0	1	0	1	1	0		0
0	0	0	0	0	0	0	0		p	0	0	0	0	0	0	0	0		p

In which 't' is the group of errors which could be rectified with an orthogonal n\bit_code, For eg, a single OLC code correction errors can be built with an 8/bit orthogonal_code (n= 8). Likewise, using a 16/bit/orthogonal code (n= 16) etc, a 3e error correction of orthogonal code could be developed. The following table-2 shows some orthogonal codes as well as the correlating ability to correct mistakes.

II. LITERATURE REVIEW

[1]When information is transmitted through a channel (wired or remote), a few clamors may influence the unwavering quality of information Because of this genuine data get changed. This alluded as mistake. In this manner blunder location and revision schemes are necessary at the beneficiary. Symmetrical digit is 1 of the coding systems which recognize just as right the defiled information. In this strategy eachk-bit informational collection is changed over into n-bit symmetrical code. A n-bit symmetrical code contains n/2 1's and n/2 0's, that implies equality of this code is constantly zero.

[2] Different pseudo-irregular or pseudo-commotion (PN) just as symmetrical arrangements that could be utilized as distribution codes for code division various access (CDVA) cell organizes or would be utilized for encoding discourse sign to diminish the leftover knowledge are researched. We quickly audit the hypothetical foundation for direct arrangement CDMA frameworks and depict the primary attributes of the maximum length, "Gold", Barker, and Kasami successions. We likewise talk about factor and fixed-length symmetrical codes like Walsh Hadamard codes. The equality of PN and symmetrical codes are additionally inferred. At long last, another PN grouping is proposed which is appeared to have certain preferable properties over the current codes.

[3] In this workl, he propose another procedure for building better more-rate space-time codes. The created code development depends on a connection of a symmetrical liberty time square code and an external M-TCM encoder. Be that as it may, dissimilar to the current STB-MTCM plans which are rate-lossy, the proposed development yields higher-rate space-time codes by extending the cardinality of the symmetrical space-time square code before linking with an external M-TCM encoder. A bit of leeway of the proposed development is that the standard methods for structuring a decent TCM code, for example, the great set parceling idea, can be received to understand the STB-MTCM plans with enormous coding gains. We introduce several schedule cases of enhanced real-time full-rate instructions for a structure to 2 receiving devices. Outcomes from leisure show that the commercial space-time models considerably outstrip the existing ST-TCM buildings. For example, the current QPSK room-time4-state 2-bit / picture code conducts scandalously stronger than the last 32-state plan, when executing the new QPSK 32-state protocol is only 1.5 dB away from either the power outage probability threshold. Furthermore, by symmetric abussing its signal, interpreting the multidimensional nature of the suggested M-TCM growth is rendered intelligently low.

[4] with regards to UWB (ultra-wideband) drive radio, one of the difficulties, for both high and low information rate applications, is the structure of an effective coding/balance plan fusing forward mistake rectification (FEC) and spreading abilities. In this paper, we present encoding procedures misusing the trellis structure of symmetrical convolutional codes for producing time-bouncing successions appropriate for UWB drive radio and, simultaneously, for mapping the data bits onto the transmitted waveforms.

[5] In computerized correspondence framework, complexity coding is favored for the means coding as it encourages a superior mistake redress as correlation with square symbols which doesn't need recollection. Among different strategies, for example, CR and SC; symmetrical coding is one of the digits that can identify mistakes and right debased information in a productive manner.

[6The purpose of packet forwarding and virtualization is to allow assistants to understand the basics of data exchange and organization and the norms used specifically on the Web through the use of the Online convention blending and the TCP / IP conference lounge area. The most rapid development in the current culture could be developments recognized with data communication and scheme establishment. A statement to this situation is the existence of some fresh long-range casual messaging apps. Officials must be ready in this computer-arranged community to operate and cope with the Interludes, many part of the intertubes, or the scheme of an connection connected with both the Intertubes. Because both the number as well as kinds of performers are extending,

it is essential to have a literature that includes the latest advances, when showing the material in a way that is available to field-based debutants with virtually no basis.

[7] The issue of blunder control and disguise in video correspondence is ending up progressively significant on account of the developing enthusiasm for video conveyance over inconsistent channels, for example, remote systems and the Internet. This paper surveys the strategies that have been produced for mistake control and camouflage in the previous 10–15 years. These methods are portrayed in three classes as indicated by the jobs that the encoder and decoder play in the basic approaches. Forward blunder camouflage incorporates techniques that include excess at the source end to upgrade mistake flexibility of the coded bit streams. Mistake covering by post preparing alludes to tasks at the decoder to recoup the harmed regions dependent on attributes of picture and video signals. Last, intuitive blunder disguise covers systems that are reliant on a discourse between the source and goal. Both ebb and flow inquire about exercises and practice in universal principles are secured.

[8] This paper depicts continuous investigate at National Laboratory keen on the issue & potential issues of calculation adaptability to 100,000_ pc frameworks. Such enormously || PCs are anticipated to be expected to arrive at a pet lemon computational speed before 2010. What's more, to make such theoretical machines a reality, IBM Research has started building up a PC named "Blue Gene" that could have up to 65,536 processor contributes the 2005 time span. A input issue is the manner by which to adequately use a engine with 100,000 processors. Logical calculations have demonstrated poor versatility on 10,000 processor frameworks that survive these days.

[9] Despite broad innovative work endeavors, existing offbeat/separation learning frameworks remain restrictively costly, essentially due to the utilization of computerized/simple video to record and play back course addresses. Therefore, full-scale organization of advanced learning innovation has been constrained to just an extremely modest number of establishments. The Lectern undertaking plans to take out the costly hardware and activity cost related with video-based course talk recording while at the same time conveying a similar degree of guidance adequacy. Platform utilizes the computerized pen and contact delicate screen advancements to fabricate an advanced work area, which is demonstrated to have the option to adequately bolster customary addressing exercises and to straightforwardly catch educators' homeroom introductions with negligible interruption.

[10] This study covers rollback-recuperation strategies That does not involve the development of a distinctive speech. We describe reset recovery conferences in the original section of the research onto bank-based and log-based events. Checkpoint-setting conferences are completely dependent on checking referring for removal of the template state. You can promote check-pointing, be uncomfortable, or provoke communications. Plug-based conventions join checking pointing with recording of non-deterministic events, masked as factors in iterators. The post-based systems may be positive, idealistic, or causal depending about how factors are recorded. Throughout the summary, we describe the assessment problems at the rollback-recovery center as well as the agreements that are currently addressing them. We also look at the showcase of multiple conferences on rollback-recovery regarding a development of alluring characteristics and evaluate the problems that arise in the use of these exchanges personable.

[11] Recently, a calculation based methodology utilizing diskless check indicating has been created give adaptation to non-critical failure to elite grid tasks. With this methodology, adaptation to non-critical failure is consolidated into the network tasks, making them versatile to any single procedure disappointment with low overhead. In this research, we execute a model called various check pointing that empowers the grid tasks to endure a specific arrangement of numerous processor disappointments by including different check pointing processors. Aftereffects of executing this procedure on a system of workstations show improvement in both the unwavering quality of the calculation and the exhibition of check pointing.

[12] Diskless Check pointing is a strategy for make sure direct the condition of a long-running calculation on a conveyed framework without depending on stable stockpiling. All things considered, it takes out the presentation bottleneck of customary check pointing on circulated frameworks. In this paper, we inspire diskless check pointing and present the essential diskless check pointing plan alongside a few variations for improved execution. The presentation of the essential plan and its variations is assessed on an elite system of workstations and contrasted with conventional circle based check pointing. We reason that diskless check indicating is an attractive elective circle based check pointing that can improve the presentation of conveyed applications even with disappointments.

[13] As the quantity of processors in the present elite PCs keeps on developing, the interim to-disappointment of these PCs are winding up significantly shorter than the execution time of numerous present superior registering applications. Albeit the present models are normally ro-bust enough to endure hub disappointments without prodding total framework disappointment, most the present elite registering applications can't endure hub disappointments and, accordingly, at whatever point a hub comes up short, need to prematurely end themselves and resume as of the earliest starting point or a steady stockpiling based check_point.

[15] This work tends to the issue of deficiency recuperation in value-based memory, and proposes a technique for issue recuperation dependent on parallel recomputing in value-based memory framework. This technique uses the information forming component of value-based memory framework to stay away from the additional expense of state sparing, moves back a solitary exchange to abstain from burning through the processing time of the deficiency free exchanges, and embraces the || re_computing strategy to decrease the expense of flaw recuperation.

[16] Independence of extraordinary components, straightforwardness and adaptability are extremely noteworthy highlights required from the adaptation to non-critical failure plans for present day bunches of PCs. So as to go to such prerequisites we built up the RADIC design (Redundant Array of Distributed Independent Checkpoints). RADIC is an engineering dependent on a completely disseminated exhibit of procedures that team up so as to make a dispersed adaptation to non-critical failure controller.

Without rare, focal or robust parts, this device operates. RADIC uses a post-log rollback-recovery protocol to adapt to inner error exercises, directly to the customer implementation. Using the RADIC thoughts we performed a system, RADICMPI, that includes some normal MPI instructions and all RADIC functionality. We attempted RADICMPI in a real realm by mixing the bunch's hubs with letdowns and inspecting the app's behavior. Our studies confirmed RADICMPI's proper operation and RADIC part adequacy.

[17] Measure-based outline presents interruption in program implementation. Interruption impacts can be relieved by making up for estimation overhead. Methods for remuneration investigation in execution profiling are displayed and their usage in the TAU execution framework portrayed. Test grades on the NAS‖ standards exhibit that transparency pay could be successful in getting better the exactness of execution profiling.

[18] Soft blunders represent an unwavering quality danger to present day digital crks. This create insurance against delicate mistakes a necessity for some apps. Correspondences and sign handling frameworks are no exemptions to this pattern. For certain apps, an intriguing alternative is to utilize optimization-based adaptation to non-critical failure (ABFT) procedures that attempt to abuse the algorithmic properties to recognize and address mistakes. Sign preparing and correspondence applications are appropriate for ABFT. One model is quick Fourier changes (FFTs) that are a key structure obstruct in numerous frameworks. A few insurance plans had planned to distinguish and address blunders in F/F/Ts. amongst folks, presumably the utilization of the Parseval or aggregate of cube check is the mainly generally recognized.

[19] With the expansion of information transmission and subsequently wellsprings of clamor and obstruction, engineers have been battling with the interest for increasingly effective and dependable strategies for distinguishing and adjusting mistakes in got information. Albeit a few systems and methodologies had projected and ap_plied in the most recent decade, information unwavering quality in transmission is as yet an issue In this research we propose a high effective joined blunder identification and adjustment procedure dependent on the OLC, Closest Match, and vertical equality.

III. PROPOSED METHODS

Advances in SoC fabrication Innovation is quickly surpassing the capacities of IC architecture. The first SoCs featured embedded small-scale (SSI) features that were design-friendly. As the number of devices increased, techniques of early design rapidly became outdated. Computerized tools are commonly used today to design integrated circuits of very big scale (VLSI). These software instruments are very complicated on their own. However, with improvements in SoC manufacturing technology, the pressure continues to raise to fix more challenging issues with design automation. Current hardware development in the modern generation of VLSI design data processing has also been pushed to the useful threshold. Completely fresh solutions to the issue of VLSI design such as parallel processing and detection of error resistance. The key to fixing this issue may be the artificial intelligence (AI) technique. This article discusses AI digital technology prospective contributors to VLSI design and tries to consider the following. Is AI going to give truly helpful alternatives, or is it going to go the way of the previous 20 years? What major changes can be expected in the design of VLSI over the next three, five or ten years due to AI? The extent in which VLSI architecture effects AI will impact the future computer community considerably. Advances in VLSI support advances in computing hardware and together they feed advances in AI research. Before describing how AI technology will be used to advance VLSI design capabilities, VLSI design requirements are reviewed, followed by an overview of existing AI based VLSI design tools. Then the salient features of AI technology are examined to draw some conclusions on their impact on VLSI design tools and methodology. Approaching AI from the VLSI design perspective, one would like to extract concepts from AI technology which can be put to practical use. Some concepts are actually not new but rephrased and with the rephrasing often come new ideas about how to use or implement the concepts.Fig.3 explains that flow parameters consideration of block here in 1st step primary input parameters are collected and assign in a manner such that useful for 4 or 8 or 16 or 32 FFT butterfly structure purpose. In the 2nd step signal processing FFT module is reconfigurable to fault tolerance detection using AI controller. Coming to 3rd step OLC block is collecting information from above FFT block detecting and correcting the errors. In section 2 existed methods have this scheme but,single error detection and correction only done but using this OLS codes multiple error correction and detections are possible. In 4th step artificial intelligence block is collection information and re_verifies the errors and fault tolerances.

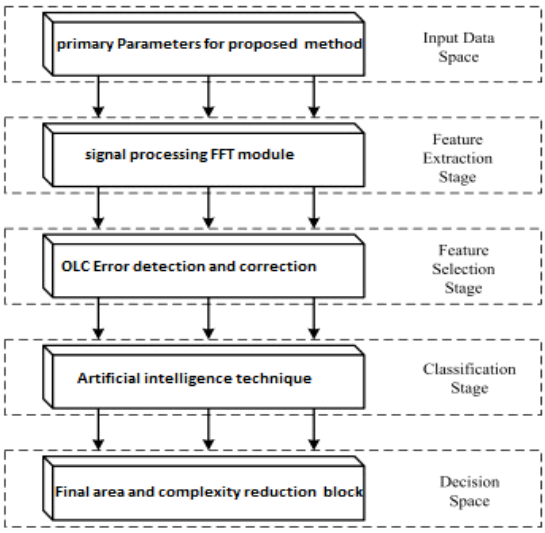

Figure: 3 flow diagrams for proposed scheme

If filtered data have any one of fault or error then send it back to FFT / OLC and re filter the data sent it to final results blocks. In the 5th step we conclude that area and complexity is analyzed.

4.1 Signal processing FFT module:

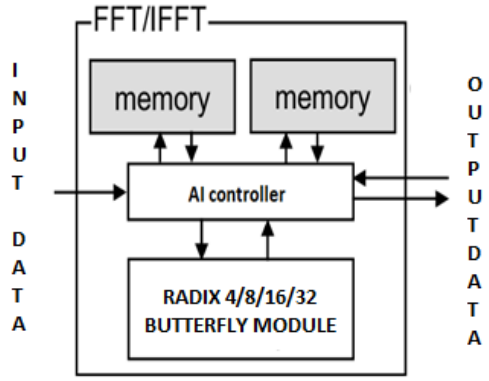

Figure: 4 FFT/IFF Modules

Fig.4 explains that FFT module with AI controller's Numeric figures is filled variables and inputs for complicated FFT routines. This discusses complicated data combined-radix FFT protocols. For FFTs of every duration, the infused-radix processes operate. They are really a re-implementation of the Fortran FFTPACK database of Paul Swarztrauber. The hypothesis is described in Clive Temperton's research article "Auto-sorting Mix-radix FFTs." Here, the modules are using the same indexation system as FFTPACK or fundamental formulas.

The blended radix calculation depends on sub-change modules—profoundly streamlined little length FFTs which are joined to make bigger FFTs. There are proficient modules for elements of 2, 3, 4, 5, 6 and 7. The modules for the composite variables of 4 and 6 are quicker than consolidating the modules for and.

For components which are not executed as modules, there is a fall-back to a general length-module which uses Singleton's technique for productively registering a DFT. This module is , and more slow than a committed module would be nevertheless works for any length. Obviously, lengths which utilize the general length-module will at present be factorized however much as could be expected. For instance, a length of 143 will be factorized into. Enormous prime components are the most dire outcome imaginable, for example as found in, and ought to be kept away from in light of the fact that their scaling will overwhelm the run-time (counsel the record "simulated intelligence FFT Algorithms" incorporated into the AI conveyance on the off chance that you experience this issue).

The blended radix instatement work AI_fft_complex_wave restores the rundown of components picked by the records for a known extent. It tends to be utilized Search the factorization of the duration and the operated-time. The drop-time scales as, where are the parts of, to the first think. For client-controlled projects, you might want to issue a note that if the duration is factorized poorly, the shift will be mild. In the event that you as often as possible experience information lengths which can't be factorized utilizing the current little prime modules counsel "artificial intelligence FFT Algorithms" for subtleties on including support for different variables Shown in fig.4

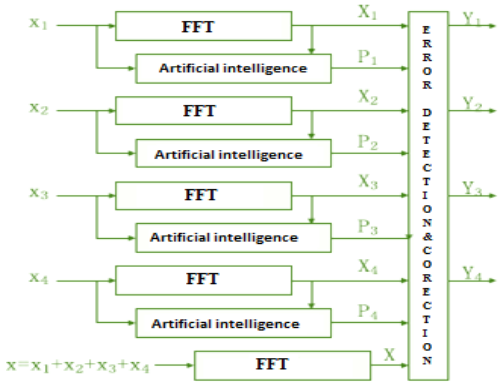

Figure: 5 AI based ECD using OLC codes

3.1 Artificial intelligence RBFN

The Radial Basis Function Network (RBFN) relying on Artificial intelligence is a version of the three-layer neural nets move foreward. They produce a carry-through feedback surface, a secret surface as well as an throughput layer named a radial base function (RBF) in the hidden layer. Its RBF systems split the feedback storage in to neurotic spheres and use a particular type of feature in the sort of receptor transition. $h(\mathbf{x}) = g\left(\|\mathbf{x}-\mathbf{c}\|^2\right)$ ---------- EQ(3)

Where ‖d‖2 is the separation work from an endorsed focus (squared Euclidean standard) Radial premise capacities originate from the field of estimation hypothesis [66]. The most straightforward are the multi-quadratic RBFs characterized by the connection

$$h(x) = \sqrt{(d^2 + c^2)}$$ ---------- EQ(4)

And the emaciated cover spline_function

$$h(x) = d^2 \ln(d)$$ ---------- EQ(5)

The accepted Gaussian RBF have the shape

$$h(x) = \exp\left(-d^2/2\right)$$ ---------- EQ(6)

A characteristic Gaussian RBF for the *j*th neuron (node) in the" univariate case "(one input) has the form"

$$h_j(x) = \exp\left(-\frac{(x_j - c_j)^2}{r_j^2}\right)$$ ---------- EQ(7)

Where cj is the middle and rj is the sweep. The middle, the separation scale and the exact state of outspread capacities are flexible parameters. Spiral premise capacities are much of the time used to make neural systems for relapse type issues. Their trademark highlight is that their reaction diminishes (or increments) monotonically with good ways from a main issue. A conventional single-layer coordinate with k neurons can be communicated by the model.

$$f(x) = \sum_{j=1}^{k} w_j h_j(x)$$ ---------- EQ(8)

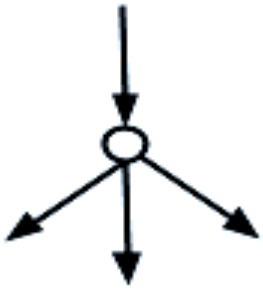

Figure: 6 3 layered model

Using this model 3 way fault detection and detection is performed find the steps in a fast manner and area and complexity is reduced. Efficiency is also more using this layer method.

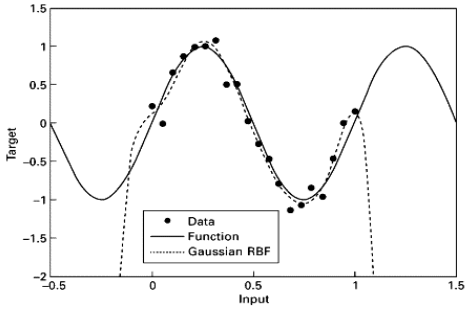

Figure: 7 target vs input comparison

Fig.7 input comparison Vs target Gaussian RBF function solves the complexity and typical-ness of parallel processing

IV. RESULTS:

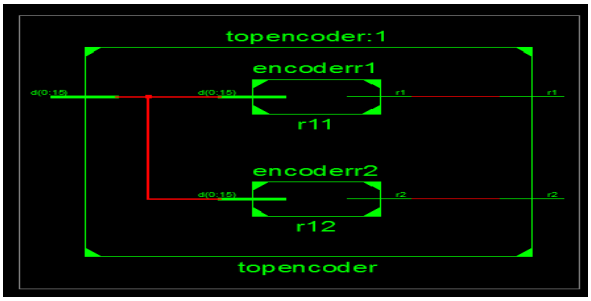

Figure: 8 top encoder block

Fig.8 explains that Here we design a encoder block with the help of AI controller such that fault tolerance can be easily identified and reduced the fault rate by Artificial intelligence RBFN

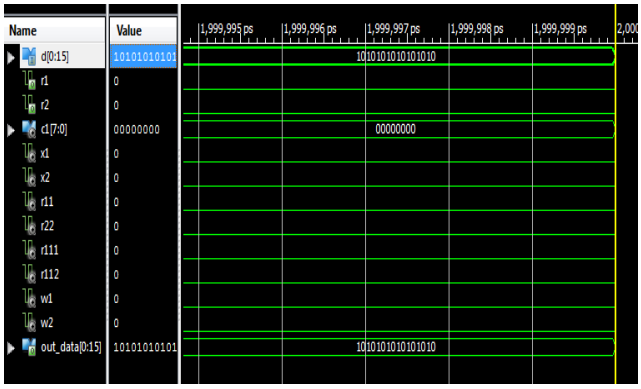

Figure: 9 top encoder block simulation

Fig.9 explains that data input can be automatically send to transmitter with the help of transmitter at the receiver end these are received with the help of OLC codes so more then one error also rectified in previous only one error can be identified and modified but using this we can more than two errors also detected and corrected.

Fig.15 explains that simulation results of proposed final model here more than one error can be corrected and detected

	UN protected FFTs	ECC protected	Parity SOS protected	Parity SOS-ECC protected	ATCPF, AIABFT	AI_OLC_PFFT PROPOSED
slices	15037	21811	23378	20156	5472	5472
Flip Flops	11407	16533	14727	13648	10944	10944
LUT-4	27830	40805	44273	38528	10944	10944

V. CONCLUSION

The privacy of parallel application of FFTs against soft mistakes was explored in this research. Two methods were suggested and assessed. The methods suggested are based on mixing an current EC approach to OLC codes with the conventional xor inspection. To detect and identify mistakes, the XOR controls are used and a straightforward parity AI FFT is used to correct them. A Proposed technique can be used to detect and locate mistakes, as well as region is the same as the existing method[20] but more than one error can be recognized and fixed and 97 percent effectiveness can be attained.

REFERENCES

1. N. Kaabouch, A. Dhirde, and S. Faruque, “Improvement of the orthogonal Code Convolution capabilities using FPGA implementation”,IEEE Electro/Information Technology Proceedings, pp. 380-384, 2007.
2. A.Mitra, “On Pseudo-Random and Orthogonal Binary Spreading Sequences”, International Journal of Information and Communication Engineering ,pp.447-454, 2008
3. Siwaruk Siwamogsatham and Michael P. Fitz, “Improved HighRate Space-Time Codes via Orthogonality and Set Partitioning” , IEEE Proceeding,264-270, 2002.
4. Luca Reggiani, Annalisa Tomasetta, Gian Mario Maggio, “Orthogonal Convolutional Modulation for UWB Impulse Radio Communications”, IEEE conference ISCAS . pp2441-2444, 2006
5. S. Faruque, “Error Control Coding based on Orthogonal Codes”, Wireless Proceedings, Vol. 2, pp. 608- 615, 2004.
6. B.Forouzon, “Data Communication and Networking”,Tata McGraw-Hill publication,4th edition,2008
7. Yao Wang, “Error Control And Concealment For Video Communication: A Review”, Proceedings Of The IEEE, Vol. 86, No. 5, May 1998
8. A. Geist and C. Engelmann, ”Development of Naturally Fault Tolerant Algorithms for Computing on 100,000 Processors”. http://www.csm.ornl.gov/ geist/ .
9. T. Chiueh and P. Deng. ”Evaluation of checkpoint mechanisms for massively parallel machines”. FTCS ’96: Proceedings of the The Twenty-Sixth Annual International Symposium on Fault- Tolerant Computing, page 370-379, 1996.
10. E. N. Elnozahy, L. Alvisi, Y. Wang, and D. B. Johnson. ”A survey of rollback-recovery protocols in message-passing systems”. ACM Computing Surveys. 34(3):375-408, 2002.

11. J. S. Plank, and K. Li. ”Faster checkpointing with n + 1 parity”. 24th Int. Symp. on Fault-Tolerant Computing, pages 288-297, Austin, Tex., June 1994.
12. J. S. Plank, K. Li, and M. A. Puening. ”Diskless checkpointing”. IEEE Trans. Parallel Distrib. Syst., 9(10):972-986, 1998.
13. Z. Chen, G. Fagg, E. Gabriel, J. Langou, T. Angskun, G. Bosilca, and J. Dongarra. ”Fault tolerant high performance computing by a coding approach”. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2005), pages 213-223, Chicago, Illinois, June 2005.
14. G. Bronevetsky, D. Marques, K. Pingali, and P. Stodghill. ”Automated application-level checkpointing of mpi programs”. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2003), pages 84-94, San Diego, CA., June 2003.
15. X. Yang, Y. Du, P. Wang, H. Fu, J. Jia, Z. Wang, and G. Suo. ”The fault tolerant parallel algorithm: the parallel recomputing based failure recovery”. In The Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT 2007), Brasov, Romania, 2007
16. G. Fagg and J. Dongarra. ”FT-MPI: Fault Tolerant MPI, Supporting Dynamic Applications in a Dynamic World”. in Lecture Notes in Computer Science: Proceedings of EuroPVMMPI 2000. Hungary: Springer Verlag.
17. D. Bailey, T. Harris, W. Saphir, R. Wijngaart, A. Woo, and M. Yarrow. ”The NAS parallel benchmarks 2.0”. In NASA Ames Research Center Report, NAS-05-020, 1995.
18. P. Reviriego, C. J. Bleakley, and J. A. Maestro, “A novel concurrent error detection technique for the fast Fourier transform,” in Proc. ISSC, Maynooth, Ireland, Jun. 2012, pp. 1–5.
19. Anlei Wang, & Kaabouch, N. (2008). FPGA based design of a novel enhanced error detection and correction technique. 2019 IEEE International Conference on Electro/Information Technology. doi:10.1109/eit.2008.4554262.
20. “Parallel failure and mean-time-between-failure recovery using aiabft with the help of automated traditional check-plancherelfunction (atcpf)” 2019

AUTHOR PROFILE

Mr.RAJUKATRU, pursed Bachelor of Technology from University of Kakatiya University in 2003 and Master of Technology from JNTU Hyderabad University in year 2009. He is currently pursuing Ph.D in Rayalaseema University,Kurnool,Andhrapradesh and currently working as Assistant Professor in Department of Electronics and Communication Engineering in Ashoka Institute of Engineering & Technology. He has published more than 13 research papers in reputed international journals. He has 10 years of teaching experience and 5 years of Research Experience.

Dr.M.Chandrasekhar, BDL Manager, Ministry of defence, Hyderabad, Telangana. He has published more than 90 research papers in reputed international journals. He has 30 years of Industrial experience and 20 years of Research Experience