Design of Low Power and High Speed Decoder and Priority Encoder using Carbon Nanotube Field Effect Transistor for Binary Content Addressable Memory Array

A. Gangadhar, K. Babulu

Abstract*: In this paper, design of Positive Feedback Adiabatic Logic (PFAL) based decoder and priority encoder using Carbon Nanotube Field Effect Transistor (CNTFET) for Binary Content Addressable Memory (BCAM) array is presented. The optimum set of CNTFET parameters such as number of tubes, chirality vector, pitch, dielectric constant and dielectric materials for low power and high speed encoder and decoder is used. The performance of proposed decoder and priority encoder is analyzed for average power, peak power and delay. Simulation results show that the proposed circuits outperforms compared to that of CMOS technology based circuits. The average power and peak power of the proposed decoder and priority encoder are in the range of µW while the range of values for CMOS based decoder are mW. The average delay of the proposed decoder is improved by 35.96% compared to that of CMOS based decoder. The average delay of the proposed priority encoder is improved by 30.77% compared to that of CMOS based priority encoder. All simulations are conducted for both CMOS and CNTFET based decoder and Priority encoder in HSPICE at 32 nm technology.

Keywords: Carbon Nanotube Field Effect Transistor, Decoder, optimum parameter set, Positive Feedback Adiabatic Logic, Priority Encoder.

I. INTRODUCTION

Content Addressable Memories (CAM) have become more popular in applications like parallel search and fast look up tables. The main functions of CAM are to store the data and to locate the address where it has been stored in the memory in less time. The CAM has the ability to search the data in one clock cycle. The simplest form of CAM is Binary CAM (BCAM). The applications of CAMs include packet classifiers, look-up table, network routers and cache controllers. CAM cell has similar structure to that of (Static Random Access Memory) SRAM except additional circuitry for comparison of data. Usually the CAM cells are arranged in an array form for storing the data and to search the data. The stored information is structured as rows and columns in the form of CAM cells. The depth and width of the CAM array is represented by number of rows and columns respectively. The main components of CAM array are encoder, decoder, data drivers and individual BCAM cells arranged in row and column pattern [1]. In CAM array the search operation takes place in parallel. This would make the search operation incredibly quick. Post-processing of CAM inputs is extremely application-specific, which is either a match or a mismatch. [2- 4]. The problem with parallel search is high power consumption. Numerous efforts have been made to improve CAM's energy efficiency.

Several attempts were made to decrease consumption of power in CAM cells/ array CAM cells/ array and its associated circuits are presented. At nanoscale CMOS faces challenges like short-channel effects, leakage current and source-to drain tunneling. Because of the high mobility of electrons movement near ballistic transport and high driving capacity and smaller area, the CNTFETs are become promising alternate for CMOS technology especially when the device scaled at nanometers range. The authors [21-26] revealed that CNTFET outperforms compared to CMOS for both circuits and transmission lines. The positive feedback logic shown superior performance in the design of BCAM cells and other circuits needed to realize the BCAM array such as priority encoder, decoder and other logic gates [27, 28].

In this paper, we proposed the design of power efficient decoder and priority encoder with optimized CNTFET and adiabatic logic. The performance of proposed optimized CNTFET based decoder and priority encoder is compared to that of CMOS based decoder and priority encoder. The rest of the document is arranged as follows. Section II presents the proposed CNTFET based decoder and priority encoder circuits. Section III presents the result analysis and performance analysis of the proposed CNTFET based decoder and priority encoder. Section IV concludes the paper.

II. PROPOSED CNTFET –PFAL LOGIC BASED PRIORITY ENCODER AND DECODER

Positive feedback adiabatic logic has basic unit of latch element comprises of back to back connected inverters. Between the output and power clock, the n channel CNTFET devices are arranged. This type of logic gates maintains the both logic 1 and logic 0 levels as outputs.

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***** Correspondence Author
A.Gangadhar*, Research Scholar, ECE Department, JNTUK, Kakinda, India. Email: gangadhar.ece@jntukucev.ac.in
K.Babulu, Professor, ECE department, JNTUK, Kakinda, India. Email: kapbbl@gmail.com

The CNTFET based PFAL logic gates NOT, AND, NOR, are shown in Fig.1, Fig.2, and Fig.3 respectively. The decoder and priority encoder circuits are designed using optimised CNTFET based PFAL logic gates. The output of the priority encoders corresponds to the active input with highest priority. Therefore, all other inputs with a reduced priority will be ignored when an input with a greater priority is present. The functional tables for priority encoder and decoder are shown in Table I and Table II respectively.

The schematic diagram of PFAL inverter gate is shown in Fig.1. The operation of PFAL inverter is explained as follows. The input is applied as A and output is taken at the junction of drains of MP_1 and MN_1. The compliment of output is taken at the junction of drains of MP_2 and MN_2. Initially, input 'A' is high and input '$\bar{A}$ is low. The output (out) stays at ground level when power clock (PC) increases from ground to V_{DD}. Output ($\overline{out}$) is same as the PC. The outputs 'out' and '$\overline{out}$' are set to values of zero and V_{DD}, respectively if PC is equal to V_{DD}. When PC value drops to zero from V_{DD}, the output $\overline{out}$ returns its energy to PC. The supplied charge is therefore retrieved. PFAL utilizes the four-phase clocking rule to effectively recover the energy. These basic gates are used to design the PFA logic based proposed priority encoder and decoder circuits. The search operation in CNTFET based IPFAL is as follows. Input A acts search data. The power and delay analysis for the both circuits are presented in Table III. It is clear from the table the CNTFET based circuits shown superior performance compared to that of the CMOS based circuits/ gates.

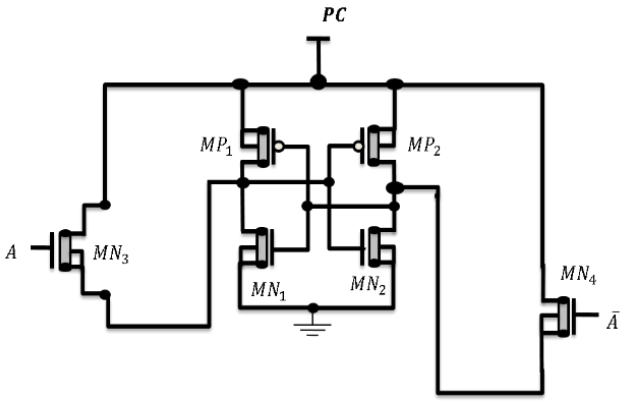

Fig1. CNTET based PFA Logic Inverter

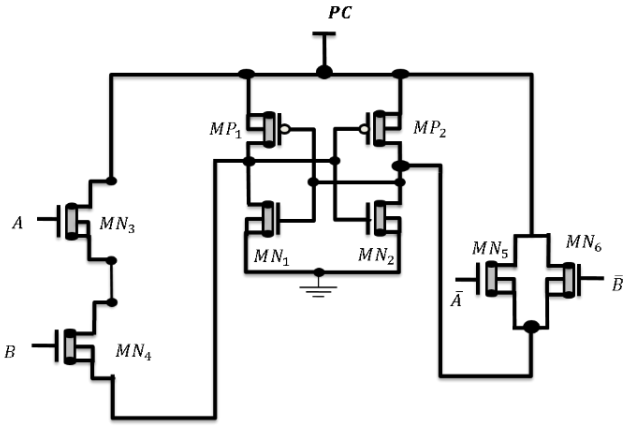

Fig2. CNTET based PFA Logic AND Gate

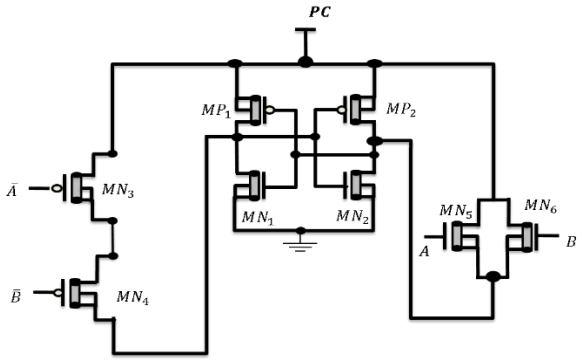

Fig3. CNTET based PFA Logic NOR Gate

Table I: Truth table of Priority Encoder:

Input of the Encoder				Output of the Encoder	
X_3	X_2	X_1	X_0	Y_1	Y_0
1	X	X	X	1	1
0	1	X	X	1	0
0	0	1	X	0	1
0	0	0	1	0	0
0	0	0	0	0	0

Table II: Truth table of Decoder

Input of the Decoder		Output of the Decoder			
X_1	X_0	d_3	d_2	d_1	d_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Table III: Delay and Average Power Values of PFA logic based basic gates

PFA based Logic Gate/ Circuit	CMOS			CNTFET		
	Delay	*Avg. Power*	*Peak power*	*Delay*	*Avg. Power*	*Peak power*
Inverter	3.053nS	0.533µW	5.63 µW	1.951nS	60.5pW	4.985nW
AND	3.341nS	0.78 µW	8.33 µW	2.285nS	0.10nW	15.41nW
OR	3.298nS	0.78 µW	8.33 µW	2.283nS	0.36nW	82.44nW

The power and delay analysis of CNTFET with various CNTFET parameters such as tube count, chirality vector, pitch value, oxide thickness and type of oxide material is performed. The analysis yielded optimal parameter set for CNTFET to achieve low power consumption.

This parameter set is used for simulation of all the CNTFET based circuits such as logic gates, encoder, decoder and the optimal CNTFET parameter set is given in Table IV.

Table IV: CNTFET parameters for Low power applications

S.No.	CNTFET Parameter	Value
1	Tube count	3
2	Chirality Vector	(10,0)
3	Pitch Value	5
4	Oxide Thickness	9
5	Oxide Material	$Si_3N_4(K_{ox} = 7)$

III. RESULT ANALYSIS

This section presents the output waveforms and performance of the proposed CNTFET based basic logic gates, encoder, decoder is presented. The performance of BCAM array in terms of average power, peak power and search delay is presented. The simulations are performed using HSPICE. The Power clock is considered as a sinusoidal of amplitude 0.7 V and frequency 125 MHz. The logic 1 is considered as 0.7 V and logic 0 is considered as 0V. All the circuits are simulated at 32nm technology. The values of average power, peak power and search delay of priority encoder are listed in Table V. The values of average power, peak power and delay of decoder is listed in Table IV. The output waveforms of PFAL logic gates, decoder and priority encoder are shown through Fig.4 to Fig.8. The output of CNTFET based IPFAL-AND gate is shown in Fig. 4. For all circuits the PC signal is sinusoidal. The inputs are square waves. It is clear that the output follows PC when two inputs are high. Otherwise, the output remains at low value. The output of CNTFET based IPFAL-OR gate is shown in Fig. 5. It is clear that the output follows PC when any one inputs is high. Otherwise, the output remains at low value. The output of CNTFET based IPFAL-NOT gate is shown in Fig. 6. It is clear that the output follows PC when input is low. Otherwise, the output remains at low value. The output of CNTFET based IPFAL- Priority encoder is shown in Fig. 7. If the input is 1XXX then the output is 10. For an input 01XX the output is 10. For an input 001X the output is 01. For an input 0001 the output is 00. The output bit 1 refers to signal which follow PC. The output bit 0 refers to logic low. The output of CNTFET based IPFAL- decoder is shown in Fig. 8. One of the four output line follow the PC while other output lines at low value.

Table V: The power and delay analysis of proposed priority encoder

S.No.	Type of the Binary CAM cell Array	Output Lines	Power and Delay values of the proposed priority encoder		
			Average Power	*Peak Power*	*Delay*
1	CNTFET	y_0	28.71 nW	4.16 µW	2.283 ns
		y_1			2.283 ns
2	CMOS	y_0	2.197 µW	79.65 µW	3.298 ns
		y_1			3.298 ns

Table VI: The power and delay analysis of proposed decoder

S.No.	Type of the Binary CAM cell Array	Output Lines	Power and Delay values of the proposed decoder		
			Average Power	*Peak Power*	*Delay*
1	CNTFET	d_0	0.6226 nW	84.65 nW	67.29 ns
		d_1			27.29 ns
		d_2			43.29ns
		d_3			3.28 ns
2	CMOS	d_0	4.155 µW	44 .41 µW	47.34 ns
		d_1			17.34 ns
		d_2			23.34 ns
		d_3			2.34 ns

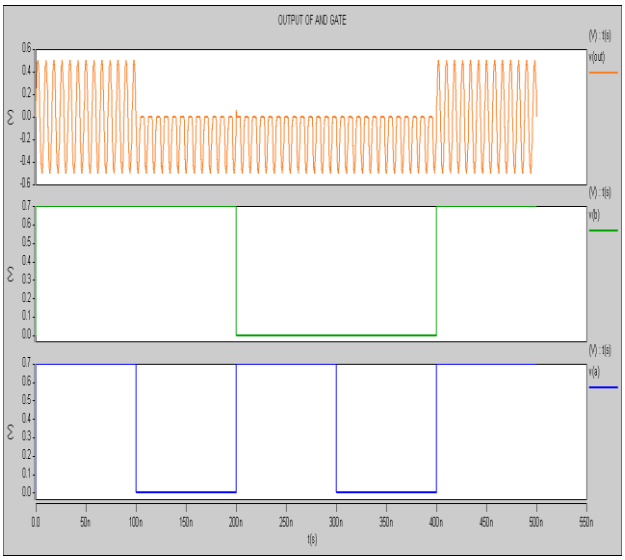

Fig.4 CNTFET –PFAL AND gate output

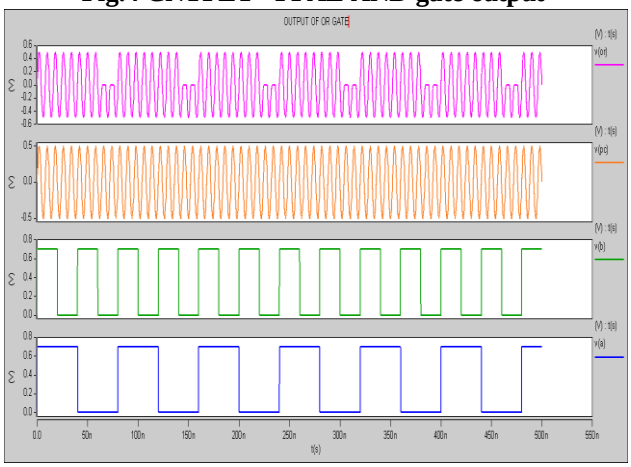

Fig.5 CNTFET –PFAL OR gate ouput

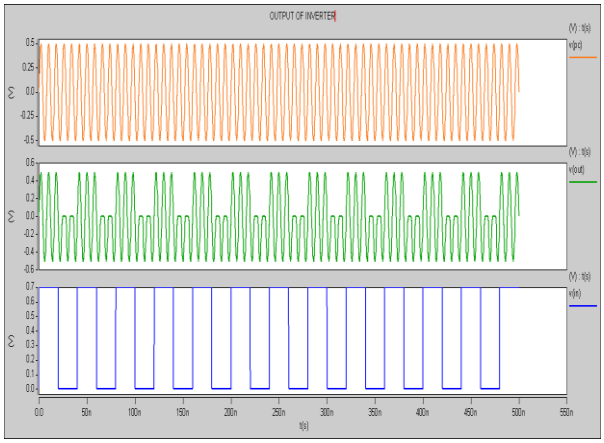

Fig.6. CNTFET-PFAL - NOT output

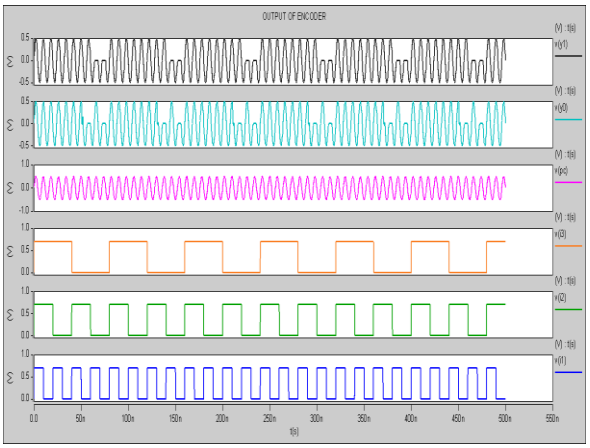

Fig.7. CNTFET-PFAL – Priority encoder output

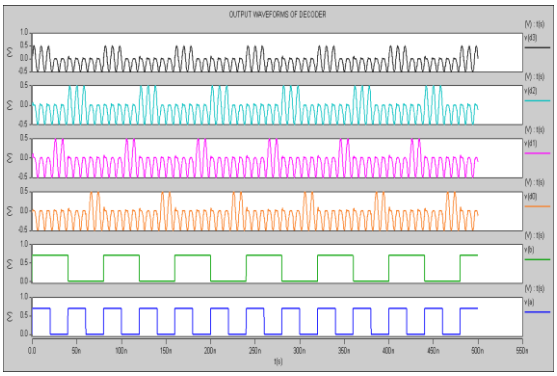

Fig.8. CNTFET-PFAL – decoder output.

IV. CONCLUSIONS

In this paper, we proposed carbon nanotube field effect transistor based basic logic gates, decoder and priority encoder circuits. The proposed circuits are based on the positive feedback adiabatic logic. The simulation results show an improvement in average power, peak power and average delay of proposed circuits compared to that of CMOS-based circuits. The average power and peak power of the proposed decoder and priority encoder are in the range of µW while the range of values for CMOS based decoder and priority encoder are mW. The average delay of the proposed decoder is improved by 35.96% compared to that of CMOS based decoder. The average delay of the proposed priority encoder is improved by 30.77% compared to that of CMOS based priority encoder. All simulations are performed in HSPICE at 32 nm technology for both CMOS and CNTFET.

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AUTHORS PROFILE

A.Gangadhar completed his B.Tech and M.Tech in 2005 and 2010 respectively. Presently, he is working as an Assistant Professor in ECE in UCEV, JNTUK Vizianagaram, India. He is a research scholar at JNTU Kakinada. His research interests include VLSI Design and Embedded System Design.

Dr.K.Babulu has received Ph.D in VLSI from JNTUA, India. Presently, he is working as Professor in the department of ECE, UCEK, JNTU College of Engineering, Kakinada. His research interests include VLSI Design, Embedded System Design, ASIC Design and PLD design.