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Enhancement of Power Quality using Fast Acting Unified Power Quality Conditioner (UPQC)

Vipin Kumar Mishra, Ritula Thakur

Abstract: ***The Unified Power Quality Conditioner (UPQC) is the most flexible solution for all power quality problems. The UPQC is one of the APF family members where shunt and series APF functionalities are integrated together to achieve superior control over several power quality problems simultaneously. Reference signal extraction is the most important part of any control. Feedback control requires the minimum information about the process also the corrective action is taken when the control variable is changed but it has some drawbacks that it does not provide any predictive action for any known disturbance. The proposed control technique uses feed forward plus feedback control with synchronously rotating reference frame based reference signal extraction that not only measures the disturbances (voltage sag here) but also take corrective action to compensate for the same before they actually disturb the system. The applications of feed forward control along with the feedback control are able to compensate for the measured disturbance with the desired speed of response that enables faster restoration of voltage at load end. The suggested method is implemented by simulation in MATLAB/SIMULINK to demonstrate the improvement in response time.***

Keywords**:** ***Power Quality, Active Power Filters, UPQC, Harmonics, DSTATCOM, DVR, d-q Theory.***

I. INTRODUCTION

It has been always difficult to maintain the quality of electric power within the acceptable limits. Some of the consequences of poor power quality may result into increased losses, abnormal and undesirable behaviour of equipment's, interference with nearby communication lines etc. The widespread use of power electronic based systems has further put the burden on power system by generating harmonics in voltages and currents along with increased reactive current. Unified Power Quality Conditioner is among the most comprehensive solutions to the power quality related problems.

The two active power filters of UPQC, the shunt active power filter or DSTATCOM (Distribution Static Compensator) and the series active power filter or DVR (Dynamic Voltage Restorer) are basically voltage source inverters controlled to ensure sinusoidal voltage to its normal value at load terminals and sinusoidal current in phase with source voltage at source terminals [1]-[3].

The present work deals with UPQC-P where the DVR injects the voltage in phase with respect to source voltage. The proposed control technique uses feed forward plus feedback control with synchronously rotating reference frame based reference signal extraction. The suggested method is advantageous over normal methods implemented by feedback control as it provides a predictive control by measuring the upcoming disturbances and providing the suitable remedies. This implementation of feed forward plus feedback control enables faster restoration of voltage at load end.

II. OPERATIONAL STRATERGY OF UPQC

The UPQC encompasses of two voltage source inverters (VSI) connected through a common dc bus consisting a capacitor. One inverter, connected in shunt through inductor coupling is known as Shunt Active Pass Filter (APF) or DSTATCOM that compensates for the harmonic and reactive current taken by the load and hence making the source current to be in phase with the source voltage and sinusoidal. Other inverter is connected in series through series transformer known as Series Active Pass Filter or DVR that injects a voltage in case of sag or swell for maintaining the load end voltage at its normal value. The integration of both series active filters and shunt active filters helps in optimizing the performance whereas independent functioning is neither optimal nor cost effective [5].

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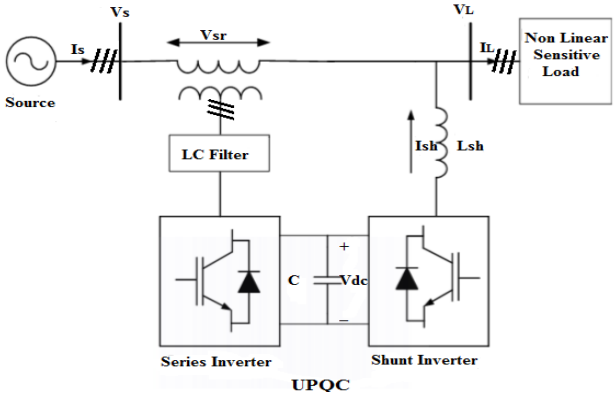
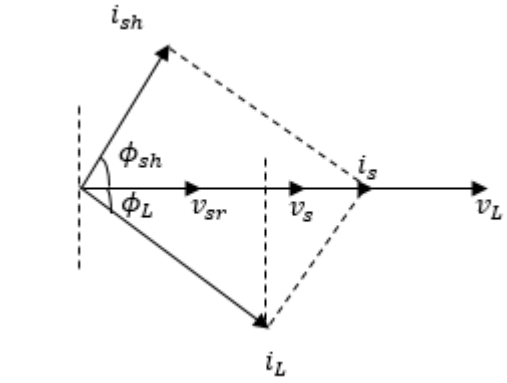
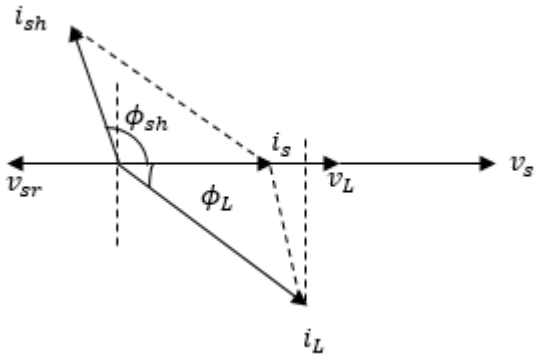


Fig. 1: Block diagram of UPQC system

In case of a non-linear load polluting the system with a great deal of harmonics, DSTATCOM injects an equal and opposite current and thus neglecting the effect of harmonics. During this operation it does not absorb any active power from source [7]. This phase relationship of the shunt compensating current with load voltage gets affected during the sag or swell conditions which indicates that there is some active power flow via DSTATCOM. Fig. 2 (a) shows that the shunt APF of UPQC is taking some active power from the source during voltage sag condition. It also draws extra current from the source to meet this increased active power demand.



(a)



(b)

Fig. 2: UPQC during (a) voltage sag (b) voltage swell

Fig. 2(b) shows that the shunt APF of UPQC feedbacks active power from the source during voltage swell condition by taking reduced current from the source to meet this reduced active power demand. This analysis shows that the magnitude of compensating current depends upon the reactive power compensation [13].

The DC link capacitor of UPQC provides power to the series inverter in case of voltage sag but it draws enough amount of power via shunt inverter of DSTATCOM to maintain its own voltage levels. Whenever the power flow changes the DC link voltage also changes which can be controlled by having a control over the power exchange between the controllers and source [9].

III. OPERATIONAL STRATERGY OF DSTATCOM

The DSTATCOM has two encapsulated loops, one inner loop to control the currents injected by DSTATCOM and the other outer loop to control the dc bus voltage as shown in Fig.3. The inner loop should respond faster than the outer loop. The dc bus is shared by both the DSTATCOM and DVR, in case of voltage sag the DVR has to inject the voltage and this causes drop in dc bus voltage i.e. why the speed of outer loop is based on the expected speed of voltage restoration of dc bus in DSTATCOM. As far as the speed of inner loop is concerned it will be decided based on the highest order harmonics that needs to be compensated. In inner loop the load current and injected currents of all three phases are converted from abc frame to synchronously rotating reference frame or d-q frame via Park's transformation.

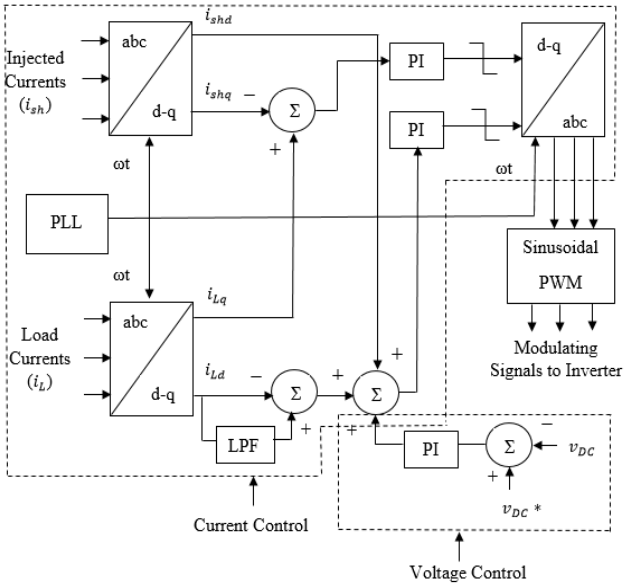


Fig. 3: Functional layout for DSTATCOM

The sinusoidal quantities are now converted into dc quantities d and q known as direct axis components or active power component of load current and as quadrature axis components or reactive power component of load current respectively. Apart from this load current also contains harmonic component which is still ac even after the transformation with different frequency.

The reference signal for DSTATCOM will be q-axis component as it has to compensate for the harmonics and reactive power but d-axis component cannot be neglected because it also contains harmonics that needs to be compensated through STATCOM and this enables filtration requirement for d-axis component.

The linear control technique (PI controller) is used to control these dc quantities which are converted back to ac using Inverse Park's Transform The peak of modulating signal may become more than the amplitude of triangular wave during sine-triangular pulse width modulation that leads to generation of lower order harmonics by inverter. This situation is called saturation and to avoid these limiters are used. These modulating signals are given to the shunt inverter that injects the compensating currents to the system.

IV. OPERATIONAL STRATERGY OF DVR

The control scheme of DVR involves feedforward and feedback controller in synchronously rotating reference frame as shown in the block diagram of Fig.4.

The three phase PCC (point of common coupling) voltages are given to the feedforward block in which they are converted from abc frame to synchronously rotating reference frame or d-q frame via Park's transformation which gives $\mathbf{v_{ffd}}$ (d-axis component) and $\mathbf{v_{ffq}}$ (q-axis component), since this transformation is in reference to the source voltage thus we get $\mathbf{v_{ffd}}$ component only and zero $\mathbf{v_{ffq}}$ component. The $\mathbf{v_{ffd}}$ component is subtracted from the pre-sag voltage which is assumed to be unity (expressed in per unit).

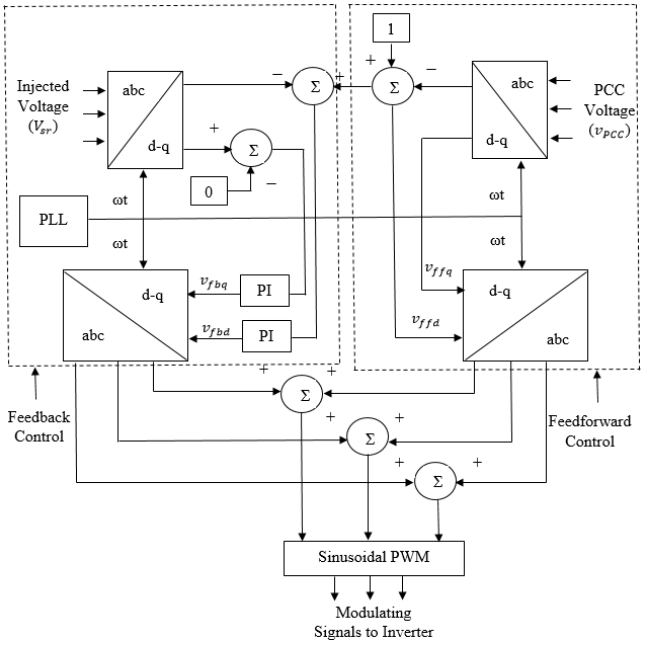


Fig. 4: Functional layout for DVR

In this way the feedforward controller computes the amount of voltage to be injected and this also serves as the reference signal to feedback controller. The feedforward voltages $\mathbf{v_{ffd}}$, $\mathbf{v_{ffq}}$ and feedback $\mathbf{v_{fbd}}$, $\mathbf{v_{fbq}}$ voltages after inverse Park's transformation gets added to give the final modulating signal and then switching signals are generated by comparison of modulating signals with switching signals.

The feedback signal to feedback controller is provided from secondary of series injection transformer of DVR. The injected voltage by DVR is in phase with the line and i.e. why it demands for some active power. The active power is provided by the DSTATCOM which draw it from the system to provide it to the DVR and to compensate for the losses in UPQC system. Since active power is used to mitigate for the voltage sag and hence it is termed as UPQC-P. The PLL (Phase Locked Loop) provides the phase angle information of source voltage and in that way helps to synchronize both DSTATCOM and DVR

V.MODELLING AND CONTROL

A. CONTROLLER DESIGN FOR DSTATCOM

The Shunt inverter of the STATCOM can be assumed to be of unity gain i.e. it is producing the voltage equal to the modulating signal at its output terminal. We need to adopt a carrier based modulation technique for generation of reference signal for shunt VSI. These reference signals are compared with high frequency carrier signals for generation of varying switching pulses. The sine triangle pulse width modulation (SPWM) associated with linear current control is adopted in the present work [23]. The output voltage of inverter has all the frequency components in modulating signal as well as components at and around multiples of switching frequency. Therefore, filters are needed at the inverter output side to filter out or minimized these components. A series R-L filter is the most common choice for filtering current output and for voltage output a complex R-L-C filter configuration is used.

The Shunt inverter is connected to the PCC through series Inductors (L) with nonzero internal resistance (R) and hence the injected current of the inverter may be written as in (1),

$$L\frac{d}{dt}\begin{bmatrix} i_{sha}(t) \\ i_{shb}(t) \\ i_{shc}(t) \end{bmatrix} = -R\begin{bmatrix} i_{sha}(t) \\ i_{shb}(t) \\ i_{shc}(t) \end{bmatrix} + \begin{bmatrix} v_{sha}(t) \\ v_{shb}(t) \\ v_{shc}(t) \end{bmatrix} - \begin{bmatrix} v_{La}(t) \\ v_{Lb}(t) \\ v_{Lc}(t) \end{bmatrix} \quad (1)$$

Where, i_{sha}, i_{shb} & i_{shc} are the currents injected by shunt inverter and v_{sha}, v_{shb} & v_{shc} are the inverter output phase voltages and v_{La}, v_{Lb} & v_{Lc} are the PCC or load end voltages. Since the system is assumed to be balanced, therefore, zero sequence component is zero and hence

$$i_{sha}(t) + i_{shb}(t) + i_{shc}(t) = 0 \quad (2)$$

The transformation of (2) in d-q reference will become

$$L\frac{d}{dt}\begin{bmatrix} i_{shd}(t) \\ i_{shq}(t) \end{bmatrix} = \begin{bmatrix} -R & -\omega L \\ \omega L & -R \end{bmatrix}\begin{bmatrix} i_{shd}(t) \\ i_{shq}(t) \end{bmatrix} + \begin{bmatrix} v_{shd}(t) \\ v_{shq}(t) \end{bmatrix} - \begin{bmatrix} v_{Ld}(t) \\ v_{Lq}(t) \end{bmatrix} \quad (3)$$

Equation (3) describes a Multi Input Multi Output (MIMO) system and therefore we need to decouple the d and q axes, so that the system reduces to Single Input Single Output(SISO) system. Let us define $\mathbf{v_d}$ and $\mathbf{v_q}$ independent variables such that

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$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \begin{bmatrix} i_{shd}(t) \\ i_{shq}(t) \end{bmatrix} + \begin{bmatrix} v_{shd}(t) \\ v_{shq}(t) \end{bmatrix} - \begin{bmatrix} v_{Ld}(t) \\ v_{Lq}(t) \end{bmatrix} \quad (4)$$

From (3) and (4), we can write

$$L\frac{d}{dt}\begin{bmatrix} i_{shd}(t) \\ i_{shq}(t) \end{bmatrix} = \begin{bmatrix} -R & 0 \\ 0 & -R \end{bmatrix} \begin{bmatrix} i_{shd}(t) \\ i_{shq}(t) \end{bmatrix} + \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (5)$$

Equation (5) represent two independent system having Single Input Single Output (SISO) approach. On taking Laplace transform of (5), we get

$$G_{shd}(s) = \frac{I_{shd}(s)}{V_d(s)} = \frac{1}{R + sL} \quad (6)$$

$$G_{shq}(s) = \frac{I_{shq}(s)}{V_q(s)} = \frac{1}{R + sL} \quad (7)$$

Equations (6) and (7) shows that both d and q axis controllers are identical. Hence the overall transfer function of the plant will be

$$G_{sh}(s) = \frac{I_{sh}(s)}{V(s)} = \frac{1}{R + sL} \quad (8)$$

It is evident from the above discussion that the controller should be designed to achieve a unity gain, first order closed-loop system for the interested frequency range i.e. the frequency of highest order harmonics we need to compensate. Let us choose a transfer function, Hsh (s) or controller such that the loop gain will become $G_{sh}H_{sh} = \frac{\omega_b}{s}$ (9)

Where, ω_b is the interested bandwidth of the closed-loop system. If we use P-I controller then in order to make the closed loop control of first order, unity gain the two gains

$$K_p = L\omega_b \text{ and } K_i = R\omega_b \quad (10)$$

So it is evident from the above discussion that proportional gain (Kp) and integral gain (Ki) depends on circuit parameters, L and R as well as on ω_b. Fig.5 shows the overall control block of closed loop current control.

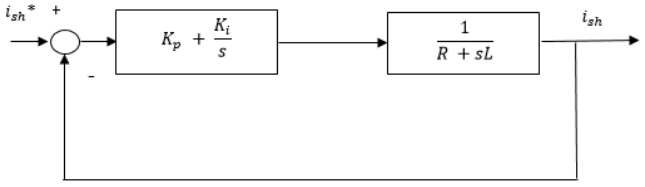

Fig. 5: Closed loop current control

Where, i_{sh}^* is the reference current to the controller. The range of bandwidth depends upon the highest order harmonics to be compensated with respect to fundamental frequency 50 Hz or 314 rad/sec. Here $\omega_b = 5966$ rad/sec. is selected to compensate up to 19th harmonics.

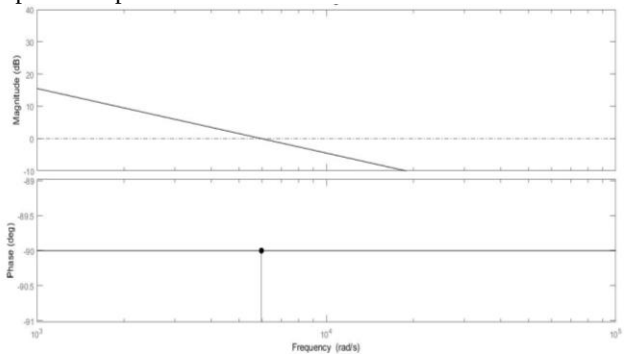

Fig. 6: Magnitude and Phase plot of inner loop gain

The controller design objectives for outer loop are basically the controller design for DC bus voltage. The regulation of DC link capacitor provides the peak reference source current. The d-q transformations are made with respect to source voltage and hence d component represents the active part while q components represent the reactive part of quantities under consideration. The real power demanded by the DSTATCOM is used to provide for the losses in shunt inverter and series inverter (in case of DVR) as well as the DC link capacitor. The controller constants of outer loop must be chosen in such a way that the required bandwidth is much smaller than the inner loop. The bandwidth ω_b for voltage control must be selected much smaller (8 to 9 times) than it is for current control as the DC bus acts as a source for DVR in case of voltage sag.

B. *CONTROL STRUCTURE FOR DVR*

The control establishment of the DVR is to compensate for the voltage sag/swell by injecting a voltage produced by inverter via a transformer connected in series with the source for maintaining the load end voltage at desired level. Feedback control is an important approach for taking out and compensating the distortion components [25]-[27]. This control requires the minimum information about the process also the corrective action is taken when the control variable is changed but it has some drawbacks that it does not provide any predictive action for any known disturbance. Therefore, a new feedforward and feedback control is adopted in the present work that not only measures the disturbances (voltage sag here) but also take corrective action to compensates for the same before they actually disturb the system [30].

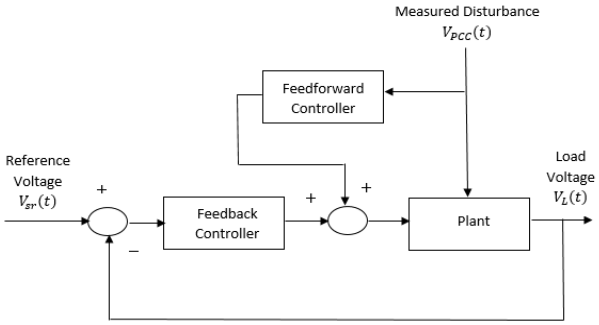

Fig. 7: Combined Feedforward and Feedback Controller

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The block diagram of combined feedforward and feedback controller is shown in Fig.7. The use of feedforward together with the feedback controller can measure the disturbances before it affects the process output as compared to the conventional feedback controller. This gives an improved performance with faster response. The knowledge of process model makes the feedforward controller more effective. A feedforward controller must always be used with the feedback controller as to observe the changes in disturbance and to avoid unmeasured disturbance. In UPQC-P, active power is used to mitigate the voltage sag as an in-phase voltage component is injected the series with line through a series inverter to compensate the voltage sag. This in-phase component is equal to reduced voltage magnitude from the desired load voltage value.

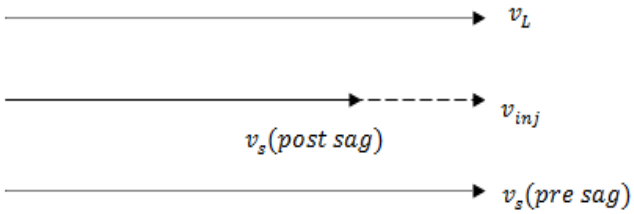

Fig. 8: Phasor diagram of In-phase compensation

To achieve the effective sag compensation, the shunt inverter of UPQC that is connected on DC side of DVR, draws the necessary active power required by the series inverter including the losses associated with UPQC. Fig.9 shows a typical series compensator connected to the system via series transformer and LC filter, where L_{se} is the filter inductance with internal resistance R_{se} and C_{se} is the filter capacitance.

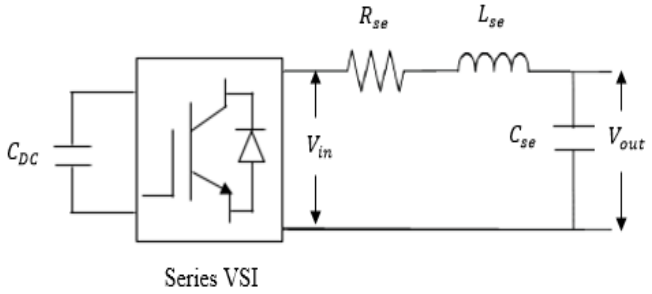

Fig. 9: System model of DVR

The Plant transfer function of DVR for a transformation ratio of 1:1 for series transformer can be written as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{s^2 L_{se} C_{se} + sR_{se} C_{se} + 1} \quad (11)$$

The bode magnitude and phase plot for transfer function of (11) is shown in Fig.10.

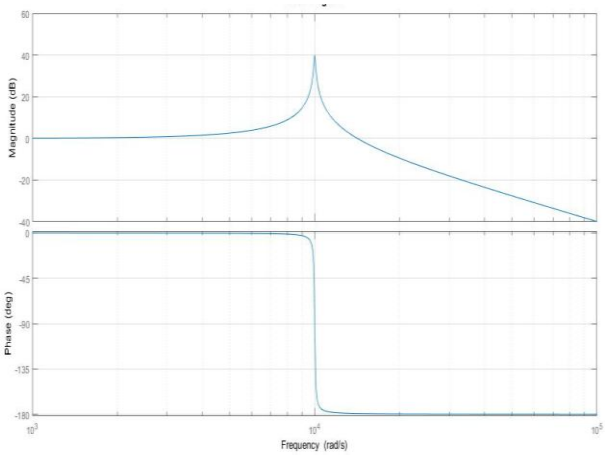

Fig. 10: Bode plot of plant transfer function of DVR

The controllers used for removing the modelling error is PI controllers, used in Feedback control to minimize the error. The improved magnitude and phase plot of DVR with closed loop control is shown in Fig.11. Consequently, the speed of operation is enhanced and in Power system speed does matter.

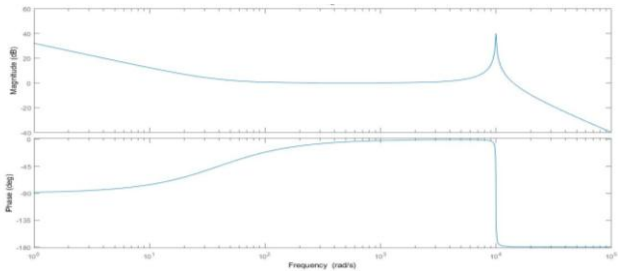

Fig. 11: Bode plot of plant transfer function of DVR

VI. RESULT AND DISCUSSION

The simulation model of the work is carried out in MATLAB/SIMULINK environment in which both DVR and DSTATCOM are modelled in to the power system. The load consists of a 3-ϕ linear network and 3-ϕ bridge rectifier as a nonlinear load. The linear network consists of resistances and inductances draws reactive power from the source which we are intended to compensate whereas the bridge rectifier inserts some non-linarites in the network and makes the associated voltage and current parts polluted with harmonics. The DVR takes care of the voltage part of the system whereas the DSTATCOM not only takes care of the current part of the system but also compensates for the reactive power. The physical parameters of the UPQC are encapsulated in Table-I

Table –I: Physical parameters for UPQC

Supply	440V, 50 Hz
Dc link Voltage	600V
DC link Capacitor	2500µF
Coupling Inductor(L_{sh})	5Mh
Resistor(R_{sh})	0.1Ω
Series Inductor(L_{se})	5Mh
Series Resistor(R_{se})	1Ω
Series Capacitance(C_{se})	5 µF

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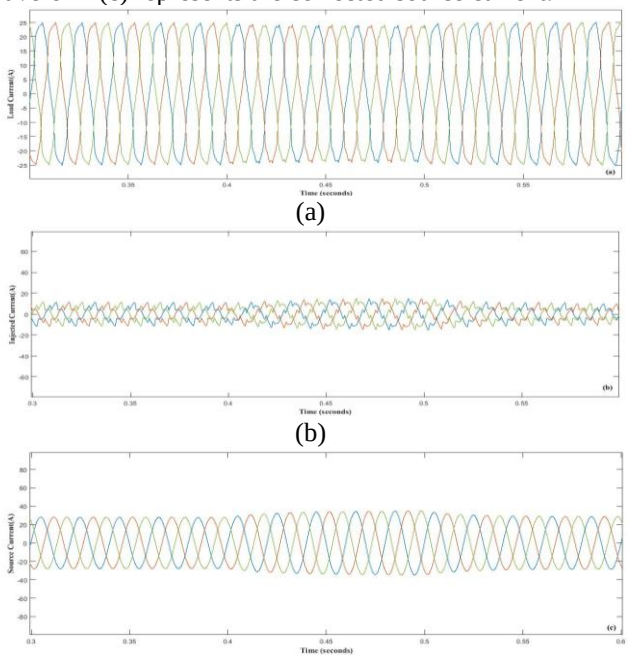
From Fig.12 to Fig.13 the results obtained from DSTACOM are shown during both the voltage sag /swell conditions. Fig.12 depicts the conditions during sag in which an increased source current is obtained due to active power being drawn from the system through shunt filter for series filter whereas the Fig.13 depicts the conditions during swell in which the source current demand is decreased due to active power being feedback to the system through shunt filter. In each of the figures the waveform (a) represents the distorted load current whereas waveform (b) represents the compensating current injected by DSTATCOM while waveform (c) represents the corrected source current.

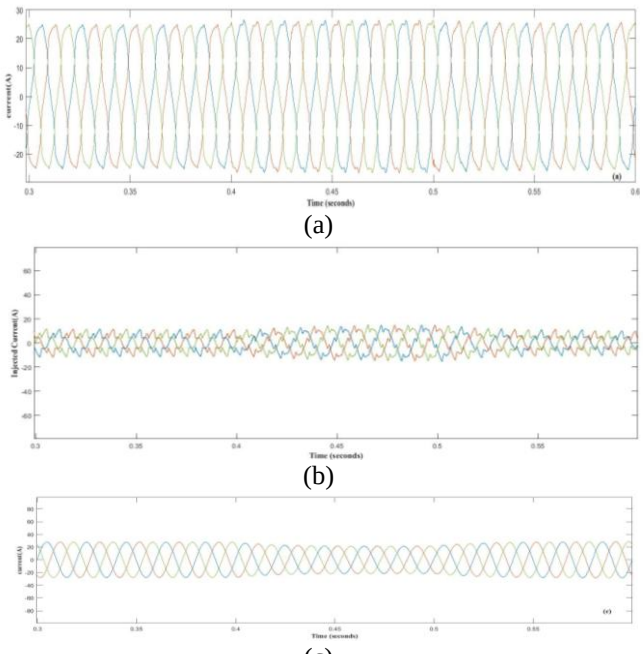


(a)

(b)

(c)

Fig.12:(a) Load Current(b) Injected current(c)Source Current for sag



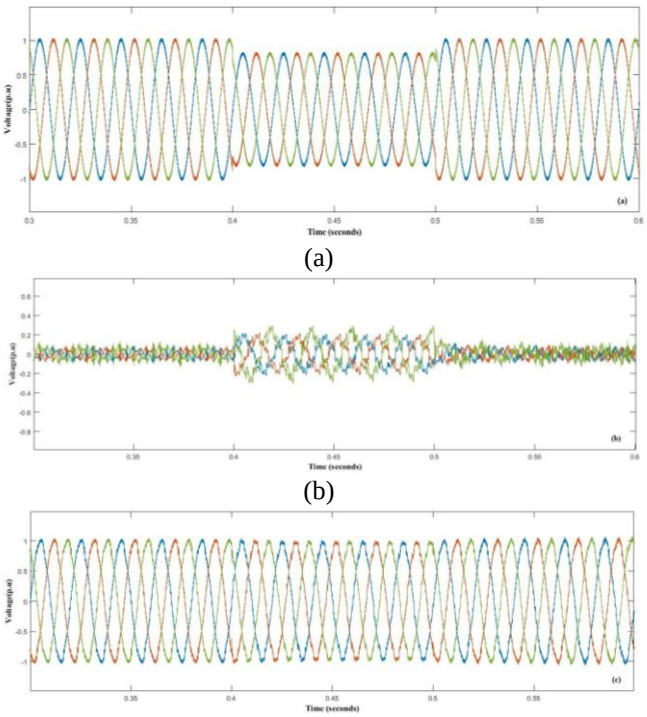
(a)

(b)

(c)

Fig.13:(a) Load Current (b)Injected current (c)Source Current for swell

From Fig.14 to Fig.15 the results obtained from DVR are shown for voltage sag/swell conditions. In each of the figures the waveform (a) represents the PCC voltage in which the sag/swell has taken place whereas waveform (b) represents the injected voltage by the DVR while waveform (c) represents the corrected load voltage

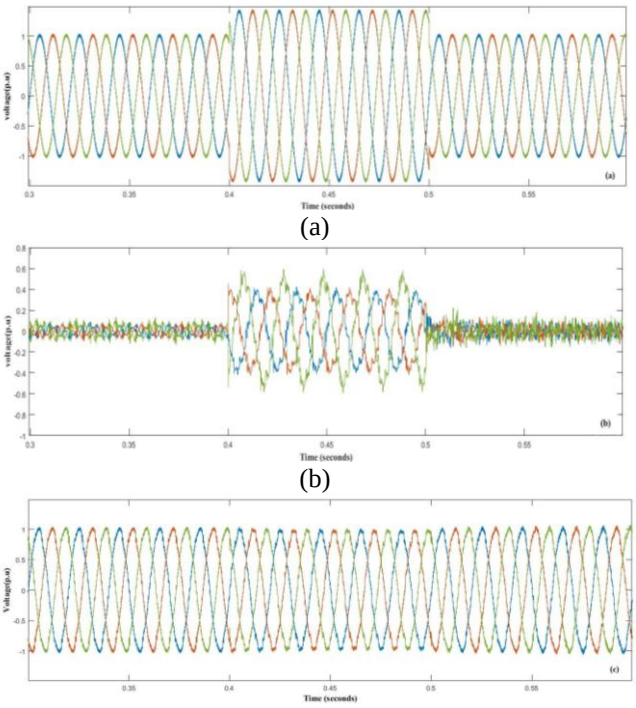


(a)

(b)

(c)

Fig.14:(a) PCC voltage reflecting the sag (b) Injected voltage by DVR (c) Improved Load voltage



(a)

(b)

(c)

Fig.15:(a) PCC voltage reflecting the swell (b) Injected voltage by DVR (c) Improved Load voltage

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As the DSTATCOM has to compensating for the reactive power demanded by the load as well and it is doing the same which is very much evident in Fig.16

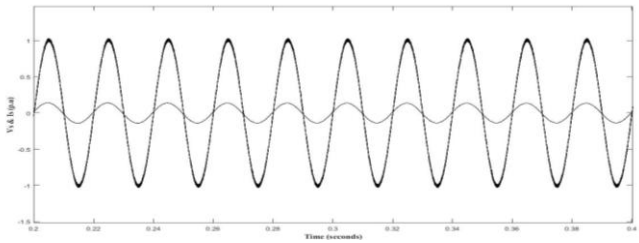
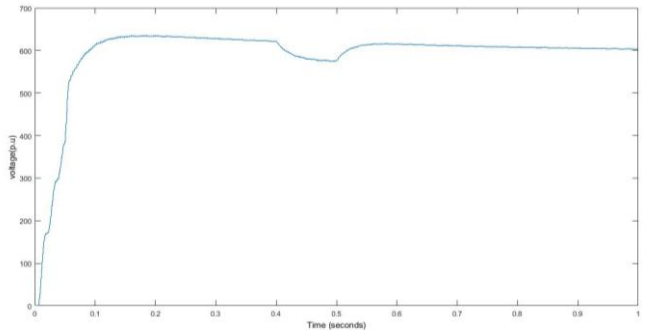
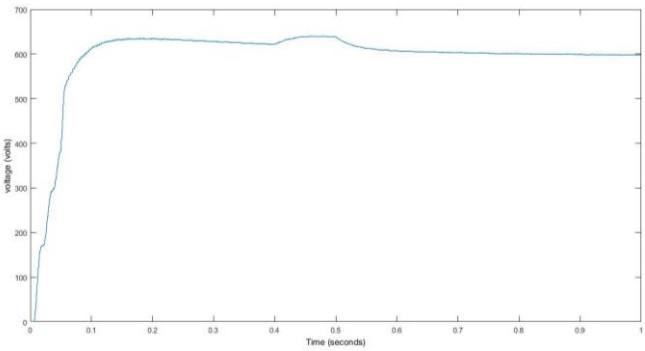


Fig.16: Phase relationship between source current (i_s) & source voltage (v_s)

The DC link capacitor voltage drop during sag conditions as series active filter requires some active power during the same while this voltage rises during swell conditions as active power is being feedback to the system via shunt filter considered as UPQC-P operation. Fig. shows the significant drop in DC link capacitor voltage during sag duration between t=0.4 to t=0.5 sec., while Fig. shows the significant rise in DC link capacitor voltage during swell duration between t=0.4 to t=0.5 sec.



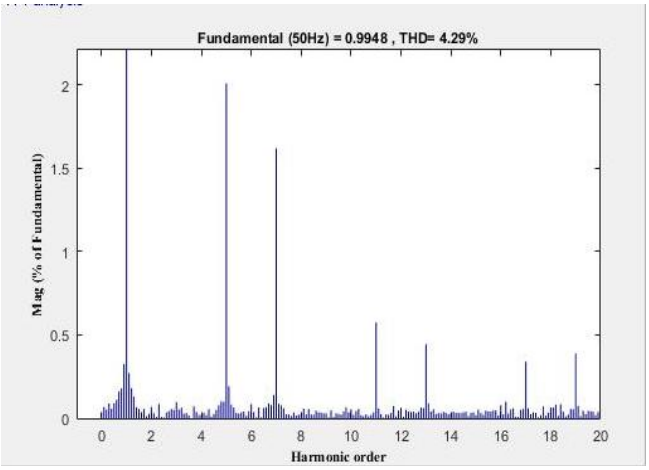
(a)



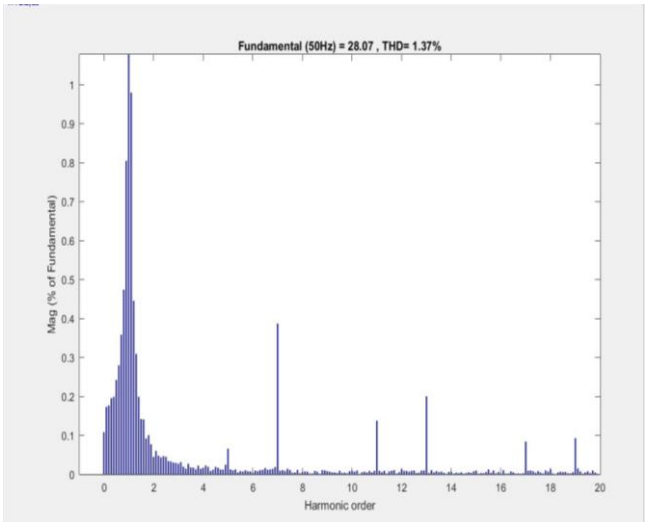
(b)

Fig.17: Variation in DC link voltage during (a) sag (b) swell

The THD of load current is reduced from 8.73% to 1.37% and THD in load voltage after compensation is found to be 4.29% as shown in Fig.18 which is well below as recommended by IEEE standards.



(a)



(b)

Fig.18: THD in (a) load voltage (b) source current

VII. CONCLUSION

The control structure proposed in the work uses feedforward along with feedback control implemented with d-q frame network. The applications of feed forward control along with the feedback control are able to compensate for the measured disturbance with the desired speed of response that enables faster restoration of voltage at load end. It has been observed that the shunt APF assists series APF in both sag/swell situations by maintaining the DC link voltage. The proposed technique is capable of improving both the voltage as well as current related problems and compensate the reactive power requirement of load and thus reducing the burden of source. The proposed method is studied using simulations in MATLAB/ SIMULINK and faster restoration of voltage profile is obtained with improved current profile which is also shown by improved THD profile.

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