# Differential CMOS Low Noise Amplifier Design for Wireless Receivers

**Mahesh Mudavath, K Hari Kishore, Srinivas Bhukya, Babu Gundlapally, Prashanth Chittireddy**

***Abstract- This article presents the differential CMOS-LNA design for wireless receiver at the frequency of 3.4GHz. This differential LNA provides less noise figure (NF), high gain and good reverse isolation as well as good stability. The designed LNA is simulated with a 180 nanometers CMOS process in cadence virtuoso tool and simulate the results by using SpectreRF simulator. This LNA exhibits a NF of 0.7dB, a high voltage gain of 28dB, and good reverse isolation ($S_{12}$) of -70dB. It produces an input and output reflection coefficient ($S_{11}$) of -6.5dB and ($S_{22}$) of -14dB, and it maintains good stability of Rollet factor $K_f > 1$, and also alternate stability factor $B_{1f} < 1$, respectively.***

***Keywords: - Differential; Low Noise Amplifier; Wireless Receivers; Noise Figure.***

## I. INTRODUCTION

The fast development of recent wireless communication technology as well as market has raised good quality by means of telecommunications and portable electronic devices [1]. The majority of the communication systems could be hand-held; hence device with compressed size is a challenging task for IC manufacturer. The key challenge for compact device size of such systems, directly that it affects power usage and portability. These are broadly used in homes and offices to offer multi-standard receivers [3]. CMOS technology for high frequency integrated circuits is an appropriate solution.

In an advanced CMOS process the challenging factors for design and development of the LNA building blocks are circuit linearity, decreasing supply voltage, low NF, and high gain. The receivers are broadly utilized in RF radio frequency systems. In reality, a receiver is capable to accept every signal from low to high frequency, and the received signals are typically very noisy and weak [1]. So, this *LNA* is desired to strengthen the received signals and transfer to the subsequent stages. For the design of LNA, noise figure is one of the important key parameter, as it shows the entire system noise presentation in a receiver, and also more power gain [1].

**Revised Manuscript Received on November 15, 2019.**

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Here, the easy way to design a differential LNA with cascode-stage to amplify weak and noisy signals for wireless receivers [4]. However, this approach requires increases the complication of the receiver, and bulky chip area [3]. The substitute technique employs the switched inductors, capacitors at the matching of input and output. This switching technique can't offer an appropriate match for all bands of frequency and it also restrictions to receive at a time one frequency band only [2,4,9]. But the cascode differential LNA design is able to offer an improved trade-off between power gain, & noise figure [3].

This paper is prearranged as follows. Section-2 covers the importance of low noise amplifier. Section-3 explains the cascode and differential amplifier techniques of LNA topologies and its fundamental theoretical calculations for design parameters. Section-4 is the description about the circuit design and analysis. The simulation plots are exposed in Section-5 and finally, Section-6 concludes this paper.

## II. LOW-NOISE AMPLIFIER

A low-noise amplifier is the foremost stage of the receiver front-end and it is used to amplify the signal which is coming from the antenna terminals whilst introducing a smaller amount of noise by the same LNA [5]. Actually the LNA consist of five different parts, which are appropriate topologies, input impedance matching network, inductive source degeneration circuit, biasing circuit, and output impedance matching network.

The universal topology of any LNA circuit can be consists of three stages. It has the input matching block, core amplifier and finally output matching block. To get better design performance the input/output matching network can try to maintain similarity. It is measured from s-parameters i.e. input/output reflection co-efficient. Generally, these values should be in the range of less than or equal to -10dBm.

The stability of the two-port network is analyzed using s-parameters. The essential and sufficient condition for stability is to taken from Rollet factor $K_f > 1$ and also alternate stability factor $B_{1f} < 1$, these are expressed in terms of s-parameters [1].

$$K_f = \frac{(1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2)}{(2\,|S_{12}*S_{21}|)} \quad (1)$$

$$|B_{1f}| = 1 + |S_{11}|^2 - |S_{22}|^2 - \Delta \quad (2)$$

Where

$$\Delta = (S_{11}.S_{22} - S_{12}.S_{21})$$

If $K_f > 1$ & $B_{1f} < 1$, the network would be unconditionally stable.

## III. CASCODE AND DIFFERENTIAL AMPLIFIER

The amplification block of the cascode circuit is revised during this analysis to attain an optimized performance in single-ended and differential topologies.

### 2.1. Cascode Transistor Amplifier

The signal flows through the gate of the first transistor $M_1$, to the second transistor $M_2$. The bias reference voltage $V_{ref}$ is fixed at gate of the second transistor $M_2$, such that both transistors operate in saturation mode. The lower transistor acts as a common source amplifier, whereas the upper transistor works in the common gate configuration and also it act as isolating output nodes from input.

To analyze the cascode stage and its circuit performance, we treat the two series connected transistors as a single compound transistor with the gate and source of $M_1$ and drain of $M_2$ acting as the corresponding terminals of the equivalent transistor.

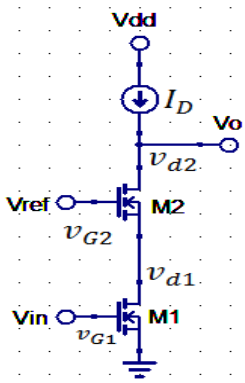


**Fig. 1. cascode amplifier**

To measure the drain current $I_D$ for cascode amplifier shown in Fig. 1 is a function of gate voltage $v_G$ which is applied at the gate terminal, and drain voltage $v_D$ which is taken from output of drain terminal.

$$I_D = f(v_G, v_D)$$

$$\partial I_D = g_{meq}\,\partial v_{G1} + g_{oeq}\,\partial v_{D2}$$

$$g_{meq} = \left.\frac{\partial I_D}{\partial v_{G1}}\right|_{\partial v_{D2}=0}$$

$$g_{oeq} = \left.\frac{\partial I_D}{\partial v_{D2}}\right|_{\partial v_{G1}=0}$$

$$\partial v_{Ds2} = \partial v_{D2} - \partial v_{S2} = 0 - \partial v_{S2} = -\partial v_{d1}$$

$$\partial v_{Gs2} = \partial v_{G2} - \partial v_{S2} = 0 - \partial v_{S2} = -\partial v_{d1}$$

We then evaluate its equivalent $g_{meq}$ and $g_{oeq}$. Since the two transistors are in series, then the drain currents of both transistors are equal i.e.

Here, current for both $M_1$ and $M_2$

$$I_{D1} = g_{m1}v_{G1} + g_{o1}\partial v_{D1}$$

$$I_{D2} = -g_{m2}v_{D1} - g_{o2}v_{D1}$$

$$where\ I_{D1} = I_{D2} = I_D$$

$$v_{D1} = -\frac{I_D}{g_{m2} + g_{o2}}$$

$$I_D = g_{m1}v_{G1} - I_D\frac{g_{o1}}{g_{m2} + g_{o2}}$$

$$I_D\left[1 + \frac{g_{o1}}{g_{m2} + g_{o2}}\right] = g_{m1}v_{G1}$$

$$g_{meq} = \frac{I_D}{v_{G1}} = g_{m1}\frac{1}{\left[1 + \frac{g_{o1}}{g_{m2} + g_{o2}}\right]}$$

$$g_{m2} >> g_{o2}$$

Generally $g_m$ values are very much higher than $g_o$ values. In this case, we can see that

$$g_{meq} \cong g_{m1}$$

$$g_{oeq} = \left.\frac{\partial I_D}{\partial v_{D2}}\right|_{\partial v_{G1}=0}$$

We should make $\partial v_{G1} = 0$ and evaluate the change of drain current $I_D$ according with change in the drain voltage of $M_2$ to get $g_{oeq}$.

$$\partial v_{gs1} = 0$$

$$\partial v_{gs2} = \partial v_{G2} - \partial v_{s2} = -\partial v_{d1}$$

$$\partial v_{ds2} = \partial v_{d2} - \partial v_{d1}$$

$$I_d = 0 + g_{o1}v_{d1} \quad (\text{for } M_1)$$

$$I_d = -g_{m2}v_{d1} + g_{o2}(v_{d2} - v_{d1}) \quad (\text{for } M_2)$$

$$v_{d1} = \frac{I_d}{g_{o1}}$$

$$I_d = -I_d\frac{g_{m2} + g_{o2}}{g_{o1}} + g_{o2}v_{d2}$$

$$g_{oeq} = \frac{I_D}{v_{D2}} = \frac{g_{o1}g_{o2}}{g_{o1} + g_{o2} + g_{m2}}$$

But $r_{oeq} = \frac{1}{g_{oeq}}$

$$g_{m2} >> g_{o1}\ and\ g_{o2}$$

$$g_{oeq} = \frac{g_{o1}g_{o2}}{g_{m2}}$$

$$r_{oeq} = g_{m2}.r_{o2}.r_{o1}$$

We can define the individual $DC$ gains of the two transistors (in CS and CG configurations respectively) [6]. Then the voltage gain $A_V$ can be defined as.

$$A_o = -\frac{g_{meq}}{g_{oeq}} = -\frac{g_{m1}(g_{m2}+g_{o2})}{g_{o1}+g_{o2}+g_{m2}} \times \frac{g_{o1}+g_{o2}+g_{m2}}{g_{o1}g_{o2}}$$

$$A_o = -\frac{g_{m1}(g_{m2} + g_{o2})}{g_{o1}g_{o2}}$$

$$A_o = -\frac{g_{m1}}{g_{o1}}\left[1 + \frac{g_{m2}}{g_{o2}}\right]$$

$$A_{o1} = -\frac{g_{m1}}{g_{o1}} \quad \text{------- For CS stage}$$

and

$$A_{o2} = \left[1 + \frac{g_{m2}}{g_{o2}}\right] \quad \text{---- For CG stage}$$

$$A_o = A_{o1}.A_{o2} \qquad (3)$$

Here, the effective $g_m$ of cscode is same as the single transistor amplifier.

#### *2.1.1. The Small-Signal Model Analysis*

The small- signal model analysis for cascode transistor shown in Fig. 2. The equivalent transconductance $g_{meq}$ for the cascode stage is regarding the similar to the single transistor stage, the product of Gain Bandwidth ($G \times B$) also remains unchanged. Because of high output impedance, the bandwidth is reduced and the DC gain is increased for a cascode-stage.

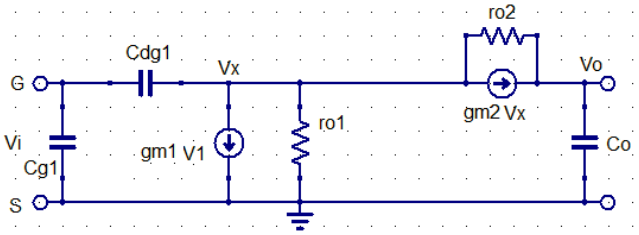


**Fig. 2. The small- signal model analysis for cascode.**

Writing the KCL equation at the output we get

$$g_{m2}v_x + \frac{v_x - v_o}{r_{o2}} = sC_o v_o$$

This leads to

$$v_x(1 + g_{m2}r_{o2}) = (1 + sC_o r_{o2})v_o$$

$$v_x = \frac{1 + s\,C_o r_{o2}}{1 + g_{m2}r_{o2}}v_o = \frac{1 + s\,C_o r_{o2}}{A_2}v_o$$

Since $A_2$ is quite large, $v_x$ is very small compare to $v_o$, $KCL$ at the drain of the lower transistor is.

$$sC_{dg1}(v_i - v_x) = g_{m1}v_i + \frac{v_x}{r_{o1}} + sC_o v_o$$

$$\left(sC_{dg1}v_i - sC_{dg1}v_x\right) = \frac{g_{m1}r_{o1}v_i + v_x + sC_o r_{o1}v_o}{r_{o1}}$$

$$\left(sC_{dg1}v_i - sC_{dg1}v_x\right)r_{o1} = g_{m1}r_{o1}v_i + v_x + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = v_x\left(1 + sC_{dg1}r_{o1}\right) + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = \frac{1 + s\,C_o r_{o2}}{A_2}v_o\left(1 + sC_{dg1}r_{o1}\right) + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = v_o\left[\frac{(1 + s\,C_o r_{o2})\left(1 + sC_{dg1}r_{o1}\right)}{A_2}\right] + sC_o r_{o1}v_o$$

$$v_i\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right) = v_o\left[\frac{(1 + s\,C_o r_{o2})\left(1 + sC_{dg1}r_{o1}\right) + A_2 sC_o r_{o1}v_o}{A_2}\right]$$

This gives

$$\frac{v_o}{v_i} = \frac{\left(sC_{dg1}r_{o1} - g_{m1}r_{o1}\right)A_2}{(1 + s\,C_o r_{o2})\left(1 + sC_{dg}r_{o1}\right) + A_2 sC_o r_{o1}}$$

$$\frac{v_o}{v_i} = -\frac{\left(A_1 - sC_{dg}r_{o1}\right)A_2}{(1 + s\,C_o r_{o2})\left(1 + sC_{dg}r_{o1}\right) + A_2 sC_o r_{o1}}$$

If $sr_{o1}C_{dg}$ is small we can simplify the above relation to get.

$$Voltage\ gain(A_v) = \frac{v_o}{v_i} = -\frac{A_1 A_2}{1 + s\,C_o r_{o1}\left(A_2 + \frac{r_{o2}}{r_{o1}}\right)} \qquad (4)$$

### 2.2. Differential Amplifier

The differential of LNA is broadly used because of its compensation of common-mode (CM) noise immunity [7]. The selection of cascode topology within initial stage degrades the noise presentation of the amplifier yet if it improves the gain. To occupied less chip area by using single ended LNAs, but if the amplifier design is single ended, it's a lot of vulnerable to noise and alternate interferences [8].

Alternatively, by using the differential amplifier very less amount of liable to noise and intervention are presented [9]. Also the differential amplifier has the benefit, of getting the signal swing which will be a double that of the single-ended swing lying on the similar supply voltage, in that way increasing signal-to-noise ratio (SNR) [8].

## IV. CIRCUIT DESCRIPTION

### A. Cascode Configuration.

The universal topology of LNA is consists of 3 stages: staring with input matching set-up, the core amplifier design, and finally the output matching set-up [16]. To begin with, input matching necessities are fulfilled by putting an inductor $L_g$ at gate of $MOSFET$ transistor it allows resonating at the centre freq. To realize low NF in given structure, an inductor $L_s$ is located on source terminal; it acts as inductive source degeneration [16]. The capacitance $C_{gd}$ is worn for wide-band matching. Therefore the $L_g$, $C_{gs}$ and $L_s$ provide the input matching network for wide-band matching. At the output side $L_d$ and $C_d$ is resonating to a particular frequency [16].

### B. Cascode Differential Configuration

The projected differential cascode LNA [17] [18] is illustrates in Fig. 3. This differential design includes the each side inductive degenerated CS and a CG stage of transistor $M_1$ and $M_2$. Also it consists of input $L_g$, $L_s$ inductors, gate-to-source capacitors $C_{gs}$, respectively for both sides [17]. The advantage of input-output and noise matching simultaneously, with the help of inductive source degenerated through inductor $L_s$. To avoid the DC signal at the input ports, the DC blocking capacitor $C_B$ and an off chip capacitor $C_p$ are used. To optimize the power gain & noise of the LNA, a very small value of shunt capacitance $C_s$ is connected at the input port. Transistors $M_3$ and $M_4$ commonly called as cascode devices, hence it formed as CG stage cascoded to the input stage [17] [19]. The benefit of the cascode device using in LNA circuit is essentially shields the output from the input stage; hence it extremely improves the power gain and reverse isolation ($S_{12}$) [20].

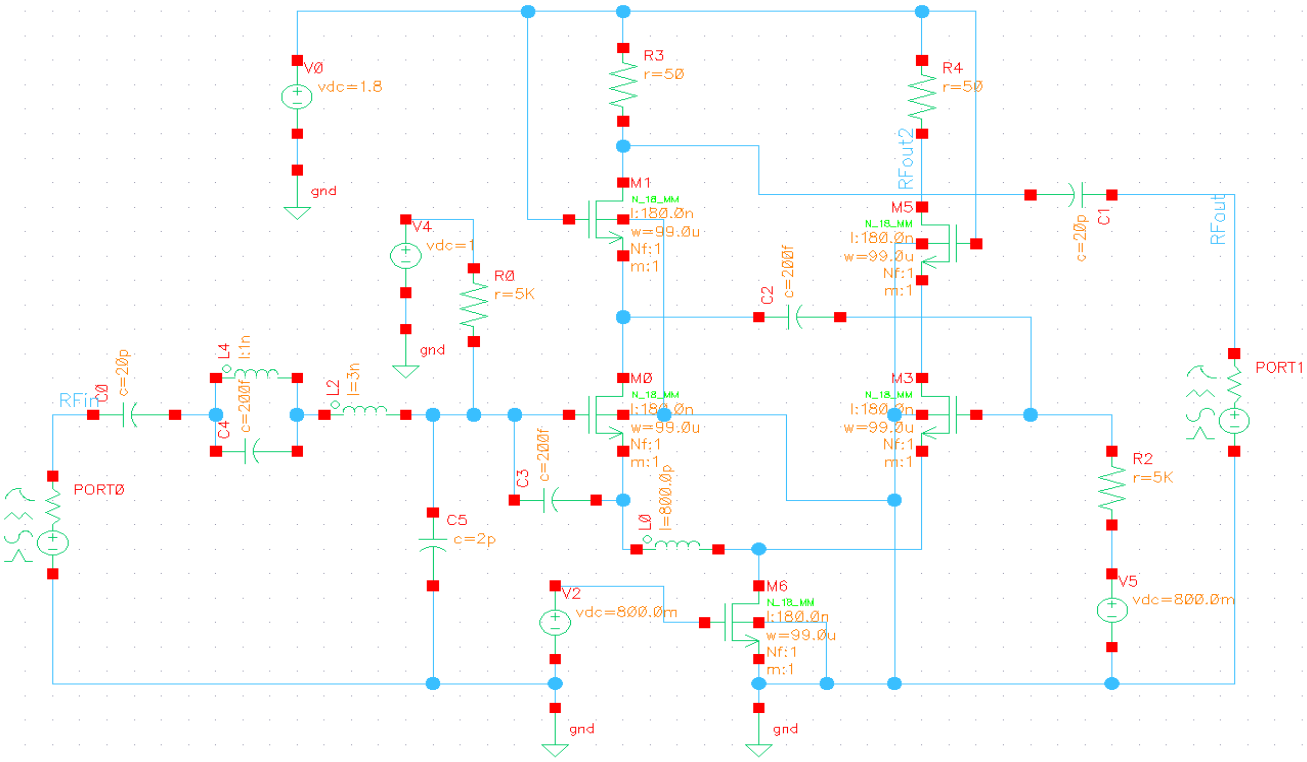


**Fig. 3. Schematic design of Differential LNA**

## V. RESULT ANALYSIS

The design parameters of the LNA circuit are analyzed with respect to the frequency of 3.4GHz operation. A plot of the S-parameters and required parameters is shown from Fig. 4 to Fig. 8. The $S_{21}$ plot is of importance as it gives the gain of the amplifier. As it can be seen from Fig. 4, a gain of 28dB is obtained at 3.4GHz which falls right in our desired range.

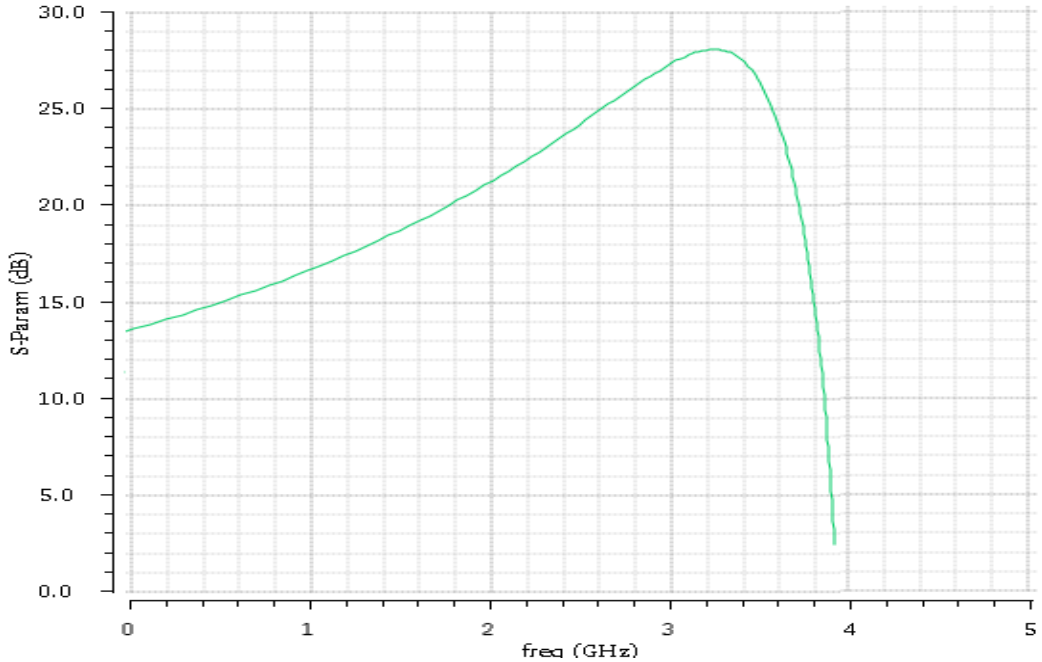


**Fig. 4 Simulated voltage gain $S_{21}$=28dB @ 3.4GHz center frequency**

The plot of Noise Figure is shown in the Fig. 5, a noise figure (NF) of 0.7dB @ 3.4GHz is obtained.

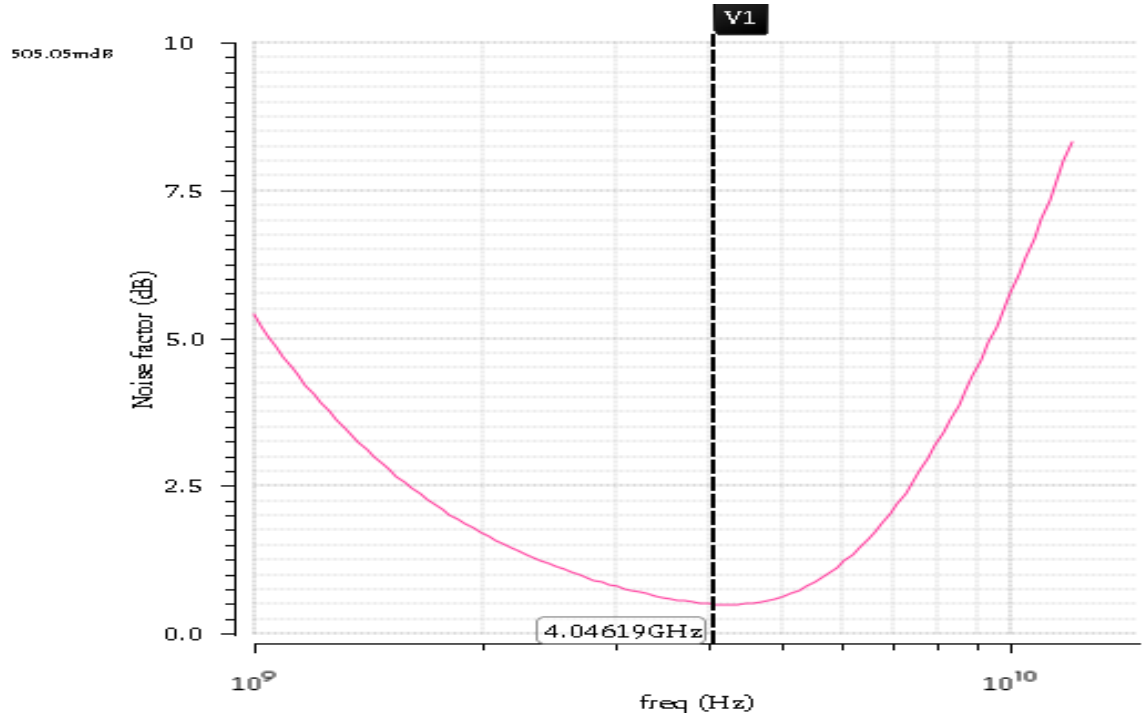


**Fig. 5 Simulated noise figure (NF) =0.7dB @ 3.4GHz center frequency**

Fig. 6 gives the reverse isolation ($S_{12}$) that is provided by the circuit. The value of the isolation that was obtained is -70dB @ 3.4GHz which are very good figure. This is attributed to the resonating circuit that is inserted between the two stages.

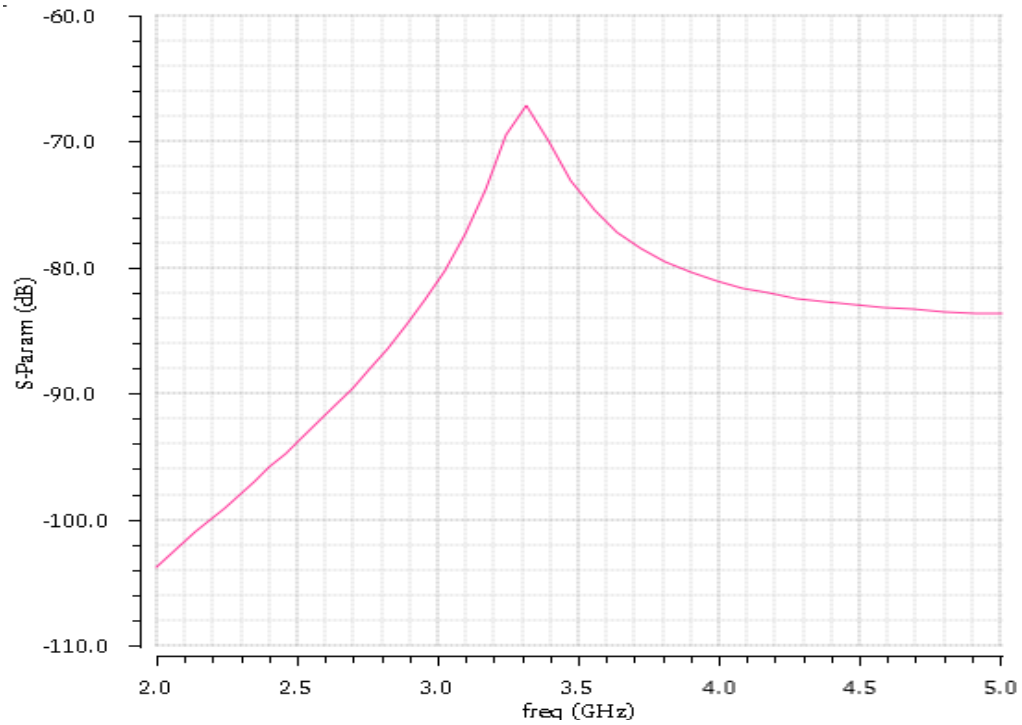


**Fig. 6 Simulated reverse isolation ($S_{12}$) = -70dB @3.4GHz center Frequency**

Fig. 7 gives the input reflection coefficients ($S_{11}$), and its obtained value is -6.5dB @ 3.4GHz

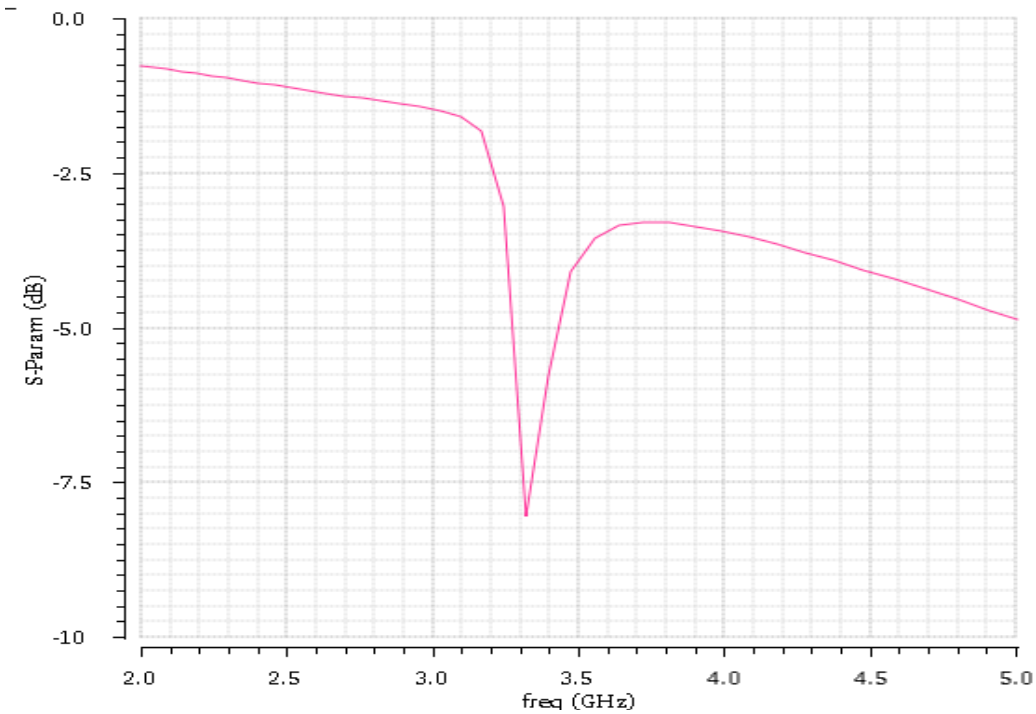


**Fig. 7 Simulated input return loss $S_{11}$= -6.5dB @ 3.4GHz center frequency**

Fig. 8 gives the output reflection coefficients ($S_{22}$), and its obtained value is -14dB @ 3.4GHz.

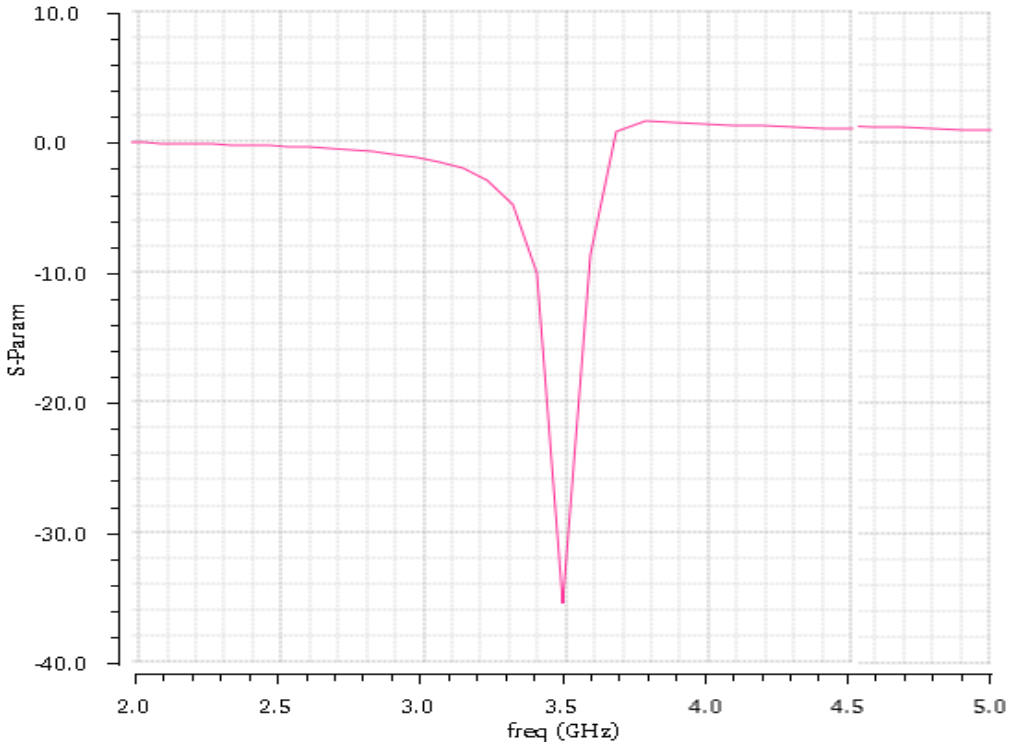


**Fig. 8 Simulated output return loss $S_{22}$= -14dB @ 3.4GHz center frequency**

The simulated results are summarized and compared to other related works in the area of LNA design and also with some designs employing the cascode strategy. The results are tabulated in table 1.

**Table 1: Performance summary and comparison of CMOS LNAs**

| **Parameters** | **This work** | **[9]** | [2] | | **[4 ]** | |
|---|---|---|---|---|---|---|
| Center Frequency (GHz) | **3.4** | 2.4 | 2.4 | 5.2 | 1.2 | 1.57 |
| CMOS Tech. (nm) | **180** | 180 | 180 | | 180 | |
| Power Gain (dB) | **28** | 12.68 | 16.5 | 11.1 | 26.9 | 27.5 |
| Noise Figure (dB) | **0.7** | 3.14 | 3.1 | 3.7 | 2.3 | 2.3 |
| $S_{11}$ (dB) | **-6.5** | -13.5 | -14 | -16 | -11 | -13 |
| $S_{12}$ (dB) | **-70** | -33.8 | -- | | | |
| $S_{21}$ (dB) | **28** | 12.68 | 16 | 11 | 26.9 | 27.5 |
| $S_{22}$ | **-14** | -10 | -6 | -8 | | |
| Stability Factor ($K_f$) ($B_{1f}$) | **1.09** **0.97** | 4.84 0.94 | 10 | 5 | -- | -- |
| Power supply (V) | **1.8** | 1.8 | 1.8 | | 1.8 | |

## VI. CONCLUSION

The field of wireless receiver communications has undergone enormous growth, moving quickly during a sequence of generations in the present scenario. The receiver design with low noise is a foremost design constraint. For this context, the design of the LNA for better performance is of immense importance. The proposed LNA for Radiofrequency front-end is designed with very little NF & high gain using 180nanometer in cadence virtuoso tool and simulate the results by using SpectreRF simulator. This LNA exhibits a NF of 0.7dB, a high voltage gain of 28dB, and a good reverse isolation ($S_{12}$) of -70dB. It gives the s-parameter value of $S_{11}$ of -6.5dB and $S_{22}$ of -14dB, and it maintains good stability of Rollet factor $K_f > 1$, and also alternate stability factor $B_{1f} < 1$, respectively.

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