Design and Implementation of Energy Efficient Power Gated MALFA Cell

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Abstract: Power gating is one of the power reduction techniques that is mostly suitable for low power VLSI applications. It reduces the power consumption by shutting of the current to the blocks not in use. Hybrid power gating is applied to Modified Adiabatic Logic based Full Adder (ALFA) cell. The proposed ALFA cell reduces the energy consumption by 67.21%, 51.31%, 55.86% and 27.01% when compared to CMOS FA, PTL with TG 16T, hybrid CMOS and PTL with TG 14T. ALFA cell with hybrid power gating technique reduces the power consumption by 1.76, 2.08%, 1.13%, 1.44%, 0.48% and delay by 5.92%, 11.19%, 11.19%, 5.92%, 24.92% when compared to ALFA cell with NMOS sleepy approach, PMOS sleepy approach, PMOS sleepy stack approach, NMOS sleepy stack approach and dual stack approach.

Keywords: ALFA cell, hybrid power gating, sleep transistor, stacking approach

I. INTRODUCTION

Digital systems are nowadays prevalently used in most of the electronics application circuits especially with the portable equipments. These portable handheld equipments have built in embedded processors need to operate for a long time with very less usage of power. Hence achieving the optimized static and dynamic power consumption in VLSI based embedded circuits in these hand held and other wireless communication based devices is the key area of contemporary research. The digital logic circuits built in with CMOS technology in the above application circuits must also embedded with the systems consuming low power[1].

In a way similar to CMOS digital logic circuits , when digital logic circuits are implemented using adiabatic logic, the method of dynamic power dissipation is due to the charging and discharging of the internal node and the load capacitances[2]. But in adiabatic logic the wastage of energy during the functioning of the circuit is very low because of the inherent characteristics of energy recovery[3,4].

In a thermodynamic process after transformation the energy occurs with no gain or loss, hence its reversible process in nature. In a adiabatic logic also most of the energy used for charging and discharging is recovered and used further. Hence it is also similar to a reversible process. Thus the term adiabatic is taken from the word thermodynamic. If the adiabatic process is made sufficiently slow then the energy loss can be achieved nearly zero. Such adiabatic logic architectures are embedded in most of the present electronics applications circuits[5].

Section 2 of this paper briefly discusses the works related to the adiabatic logic and full adders. Section 3 explains about fundamental operation of adiabatic logic circuits and its charging discharging and energy recovery process. Simulation results and performances are analyzed in Section 4. Conclusion is briefed in Section 5.

II. RELATED WORKS

A Group or a cluster based approach of controlling the power for selectively distributing the power to needed units is considered to be important design approach when power gating is employed. In the important design considerations during the adaptation of power gating technique is to minimize the total size of sleep transistors, the peak current, and the wakeup delay [6]. The trade-off between peak current and wake up delay is considered for each logic clusters and the wake up delay is considerably minimized even though the peak current is more.

Device stacking is employed in [8] to reduce the leakage power. In the device stacking a transistor is represented with the two half size transistors. Consider the trade-off between propagation delay and power reduction, the reduction of power is achieved with the help of reducing the leakage power in transistors with an increase in propagation delay. When the logic circuits are implemented in FPGA sleep transistor based power reduction based technique is mostly employed to reduce the leakage power. In [7] a preselected input vector is assumed for the placement of the alternating sleep transistors. Here Zigzag technique is used.

Adiabatic logic [9]-[10] based circuit implementation greatly decreases the dynamic power. With very less energy loss adiabatic logic based implementation of the CMOS circuit, the familiar use age of present application circuits. This kind of logic circuit has little amount of power consumption due to the existence of equivalent resistant when the transistor is switching.

III. FUNDAMENTALS OF ADIABATIC LOGIC

The energy moved from supply to Vdd or ground . switching transition function from high to low or low to high. So, for an every 0 to 1 switching transition the supplied energy is

$$E_{Suppy} = C_{Load} X V_{dd}^2$$

The total energy is divided two parts, energy saved and energy dissipated is an two part of energy [10]. The energy saved

$$E_{Saved} = C_{Load} X \frac{V_{dd}^2}{2}$$

For high to low 0 transition, the energy saved in the load capacitor (C_{load}) dissipated through the pull down circuit. The sum of current drive from time depended power source can operate as a stable current source is,

$$\text{Constant Current } i(t) =$$
$$C \frac{dv}{dt} = C \frac{Vdd}{T}$$

$$T = T_{charge} + T_{discharge}$$

At the time of charging , total energy in load capacitance C_L is,
Load capacitance energy E=I²R x T_{charge}

Total current time in charging,

$$\text{Charging current } I = \frac{C_L Vdd}{T_{charge}}$$

In our logic discharging energy is return back to the time based voltage source, the return energy is

$$E = I^2 R X T_{charge}$$
$$= \frac{\{(C_L)^2 X (Vdd)^2 X R\}}{T_{charge}}$$

This exposition_ that the diversion of energy is almost nullify in the logic. So, its termed as Energy restoration CMOS logic.

A. ALFA cell

The ALFA cell is particularly made nullify the transposing the energy in circumforaneous. This nullify loss occurs due to heat dissipation, increasing energy level applied for many applications. The CMOS structure of proposed ALFA cell is laid out in Fig. 1.
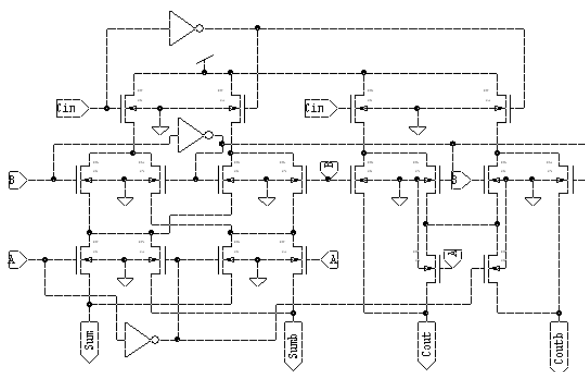

Fig.1. CMOS structure of ALFA cell

To given 5V mechanized to designed adder cell attain the exact output. Its designed by scanty voltage trance also working at the lower end. Comparing other logic techniques very less power consuming ALFA cell. This cell is performs the addition of 3 single bit inputs like A,B and C. Which provides the output as sum and carry output. It uses 24 transistors provides sum bar and C_{out} bar in a single construction which undergo reduce the level of area in this adder. It has much low lying power consumption than that of

the CMOS and PTL with TG versions of full adder cells. The truth table of ALFA cell is depicted in Table 1.

Table 1. Truth table of Full Adder

A	B	Cin	Sum	Cout
0	0	0	0	0
		1	1	0
	1	0	1	0
		1	0	1
1	0	0	1	0
		1	0	1
	1	0	0	1
		1	1	1

Full adder output splash the above truth table. For an example, if A=1, B=1 and Cin=0, the sum output Sum=0 and Cout=1. When carry input C_{in} changes from 0 to 1 sum changes from 0 to 1 and Cout = 1.

B. Proposed Power Gated Modified ALFA cell

In recent days, the usage of electronic products increases rapidly and these leads to power hungry. So there is a need of low power consumption which is the major concern in semiconductor technologies. The first one contributed to the overall low power consumption of an electronic Integrated circuits is the power consumed during dynamic moden (P_{active}). The second contribution to the low power consumption is the leakage power ($P_{leakage}$). $P_{leakage}$ is due to the existence of the undesired subthreshold current[16]. The equations representing these two contributions of low power consumption are:

$$P_{active} = CV^2 f$$

$$P_{leakage} = IV$$

$$I_{sub} = I_0 e^{\frac{(V_{gs} - V_{th} - \eta V_{ds} - \gamma V_{sb})}{nv_\theta}} \left(1 - e^{\left(\frac{-V_{ds}}{V_\theta}\right)} \right)$$

Where $I_0 = \mu c_{ox} \left(\frac{W}{L}\right) V_\theta^2 e^{18}$. Mobility is represented as μ. The Oxide capacitance is given as Cox. The Transistor's width is denoted as W, and length is denoted as L. The notation for the thermal voltage is V_θ and it is calculated as kT/q, η is the coefficient for the drain induced barrier lowering. n is termed as the co efficient to indicate the sub threshold swing .γ is body effect coefficient.

To decrease the dropping power, a mixture method is planned which is the blend of parallel sleep transistor and stacking power gating. In dropping power is controlled by method of parallel sleep transistor, two NMOS transistors are play the vital role to decrease the complete power utilization by decreasing flow of power. The sleep transistor is connected with pull up circuit and power supply (Vdd). This sleep circuit control the flow of leakage power supply to the undesired remaining loop of the circuits. Its operated two modes, which is decided by sleep transistor input.

Active mode is enabled when transistor input high , like idle mode activated when input close to the ground. In stacking effect the leakage power is reduced by turned off the transistors which are arranged in a series manner.

For further reduction in leakage power these two techniques are combined and the proposed architecture of power gated ALFA cell is shown in Fig.2.
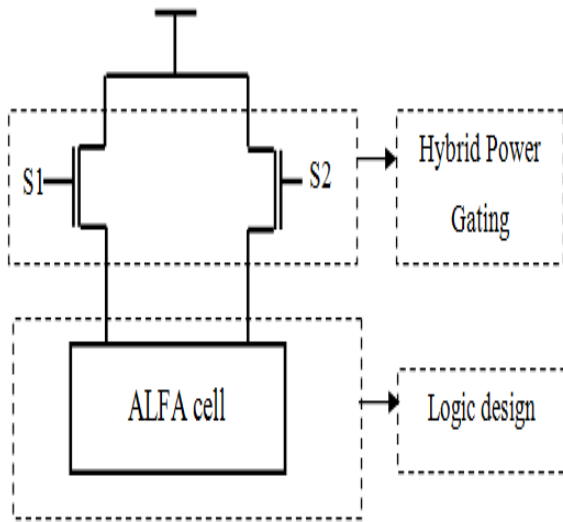

Fig.2. General Structure of Power gated ALFA cell

The proposed power gated ALFA cell is operated in three modes of operation based on the sleep signals S1 and S2. These are active mode, standby mode and cutoff mode. When two input of transistor enabled in active mode Vdd is driven to the pull down network. In standby mode, any one of the sleep signal is enabled as high and NMOS transistor in pull-down network shorts actual ground of the circuit to the virtual ground (V_{GND}) that permits Vdd to the logic circuit for high-speed operation. If both the sleep signals are kept at low, the flow of current to the ground is cut and it suppresses the path of drain into source subthreshold leakageThe leakage current is computed based on the characteristics of drain current with respect to drain voltage or source voltage. The threshold voltage V_{th} is represented as

$$V_{th} = V_{FB} + \phi_S + K_1\sqrt{\phi_S} - K_2\phi_S - \eta V_{dd}$$

Where$\phi_S = 2F_p$, F_P denotes the fermi potential, V_{FB} is a flatband voltage, K1, K2 are doping coefficients and η denotes Drain Induced Barrier Lowering (DIBL) effect. It reduces the subthreshold leakage current by increasing subthreshold voltage in pull-down network. The CMOS structure of power gated ALFA cell is shown in Fig.3.
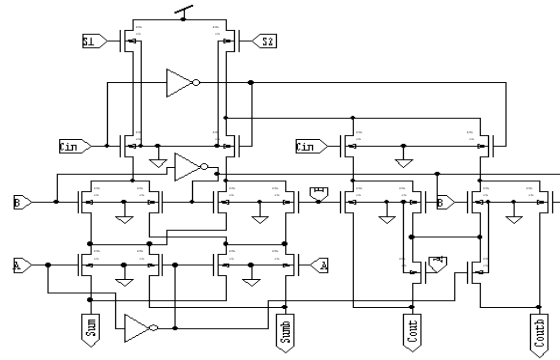

Fig.3. Power Gated MALFA cell

In MALFA cell, the supply voltage Vdd is connected to four transistors that lead to high power dissipation. But in power gated MALFA cell, the Vdd is connected to two transistors termed as sleep transistors that having the input signals as S1 and S2. Here, low leakage power can be attained by making any one of the sleep transistors turned off. If either S1 or S2 is turned OFF it cut down the power supply from power source to the pull up network that blocks the power to the unwanted devices leads to low leakage power. For example, in MALFA cell if A=1, B=1, Cin=1, the two NMOS transistors connected to the Cin are conducting 5V. But in power gated MALFA cell, if A=1, B=1, Cin=1, S1=1 the transistor connected to the Cin which is in series with the transistor having the input signal as S1 only conducts the 5V. Thus the power gated MALFA cell reduces the leakage power by cut down the power source.

1. Results and Discussions

The ALFA cell and power gated MALFA cell are designed and simulated using tanner EDA with 125nm technology. Its performances are compared in terms of area, power and delay. The simulation result of proposed power gated MALFA cell is display in Fig. 4.
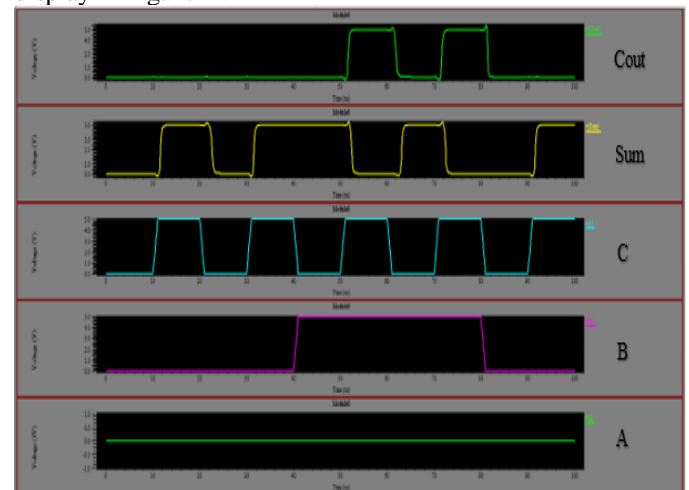

Fig.4. Simulation Result of power gated ALFA cell

The simulation results depicted the DC transient analysis of power gated ALFA cell. Here A, B, C are three single bit inputs and sum, cout are the outputs.
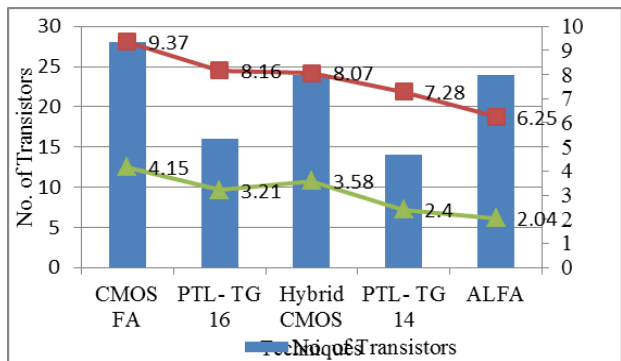
Fig.5. Comparison chart of power and delay for full adder with various logic styles

The proposed ALFA cell and hybrid CMOS logic full adder have the same number of transistors as 24. But it has some area overhead when compared to PTL based logic designs.

When compared to CMOS FA, PTL with TG 16T, hybrid CMOS FA and PTL with TG 14, the proposed ALFA cell diminish the power utilization and delay by 33.29%, 23.4%, 9.78%, 14.14% and 50.84%, 36.44%, 43.01%, 15% respectively.

Table 2: Performance Analysis of ALFA cell with leakage power reduction techniques

Technique	No. of Transistor	Power (Watts)	Delay (ns)
Sleep (NMOS)	25	6.23	2.53
Sleep (PMOS)	25	6.25	2.68
Sleepy Stack (PMOS)	28	6.19	2.68
Sleep Stack (NMOS)	28	6.21	2.53
Dual Stack	27	6.15	3.17
Proposed	26	6.12	2.38

Performances of ALFA cell with different power degradation method are evaluated in terms of area, power and delay and it is depicted in Table 4. Number of transistor count is deciding level of area. The proposed power gated ALFA cell has 26 number of transistors and it decrease the power consumption by 1.76, 2.08%, 1.13%, 1.44%, 0.48% and delay by 5.92%, 11.19%, 11.19%, 5.92%, 24.92% when compared to ALFA cell with NMOS sleepy approach, PMOS sleepy approach, PMOS sleepy stack approach, NMOS sleepy stack approach and dual stack approach.
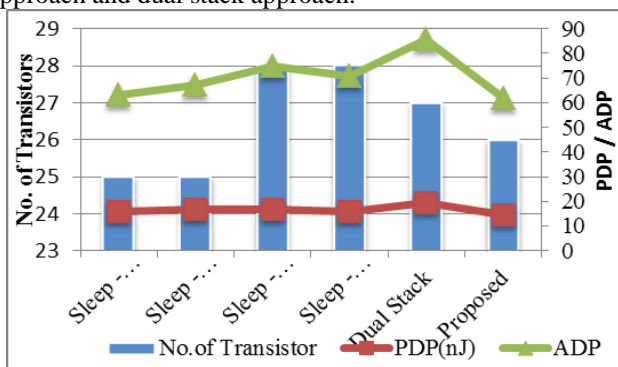

Fig.6. PDP and ADP of different power degradation method

Energy consumption and area delay product of different power degradation method of ALFA cell is shown in Fig.6. The proposed power gated ALFA reduces the PDP by 7.55%,

13.01%, 12.17%, 7.25% and 25.19% compared to NMOS sleepy, PMOS sleepy, NMOS sleepy stack, PMOS sleepy stack and dual stack.

IV. CONCLUSION

Developing modern world power utilization and power saving is an vital role. By taking this issue MALFA cell designed the combination of parallel sleep transistor and stacking power gating. The stacking method plays an important role to reduce the leakage power. The designed MALFA depending 125nm technology by using tanner EDA tool. The output results compared with other energy saving by 67.21%, 51.31%, 55.86% and 27.01% when compared to CMOS FA, PTL with TG 16T, hybrid CMOS and PTL with TG 14T. MALFA cell with hybrid power gating technique reduces the power consumption by 1.76, 2.08%, 1.13%, 1.44%, 0.48% and delay by 5.92%, 11.19%, 11.19%, 5.92%, 24.92% when compared to ALFA cell with NMOS sleepy approach, PMOS sleepy approach, PMOS sleepy stack approach, NMOS sleepy stack approach and dual stack approach.

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