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The Mixed Logic Style based Low Power and High Speed One-bit Binary adder for SOI designs AT 32NM Technology

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Abstract*: Binary adders are the fundamental building blocks to construct Data Processing arithmetic units. A novel one-bit full adder is presented in this paper which is designed by Mixed logic design style. In addition to small size transistors and reduced transistor activity compared to conventional CMOS (Complementary Metal Oxide Semiconductor) gates, it provides the priority between the High logic and Low logic for the computation of the output. Various logic topologies are used to design the one-bit full adder like High-Skew(Hi-Skew), Low-Skew(Li-Skew), TGL (Transmission Gate Logic) and DVL (Dual Voltage Logic). This new approach gives the better operating speed, low power consumption compared to conventional logic design by reducing the transistors activity and by improving the driving capability. This Mixed logic style provides 83.53% average power consumption and Propagation Delay of 14.02% at 0.8v. The H-SPICE simulation tool is used for construction and evaluation of the Full adder logic at different voltages. The 32nm model file is used for MOS transistors.

Keywords: CMOS logic, Low power CMOS, pass transistors, skew gates Transmission gate.

I. INTRODUCTION

Efficient realization of arithmetic circuits is crucial for Data Processing units in VLSI Design. Moreover, the Application Specific integrated circuit are dominating now a day for processor design [1]. The low power and high speed designs are addressed at design abstracts such as system level, circuit, layout and the process technology. The best possible achievement of power reduction and delay is observed at circuit level by choosing good choice of logic style implementation of combinational circuits. the performance parameter such as power dissipation, switching capacitance short circuit current and transition activity are strongly influenced by chosen logic style [2], [3]. The static CMOS (Complementary Metal Oxide Semiconductor) implementation is the one of the fundamental logic style which enables the integrated circuit design is more easy compared to dynamic gates. the Static gate comprise of pullup-network (usually NMOS transistors) and pulldown-network (usually PMOS transistors). the common point of both networks are call output and all the gates are connected by input signals. Design of such gates are called

Cell components which are useful for logic synthesis. It is noticed that primary inputs for CMOS logic drives the gate terminal of the transistor. Another possibility to construct the logic by driving primary input at the source and drain terminals of the transistor, this is called Pass Transistor Logic (PTL) [5]. It is possible to reduce the number of transistors to implement any logic function using this PTL logic. There are variety of logic implications alternative to CMOS logic to achieve less number of transistors, low delay and less area. PTL and TGL (Transmission Gate Logic) are most dominating logic style compared to Static CMOS with respect to number transistors [10]. The main deference among PTL, TGL and static CMOS is that in PTL implementation contains only NMOS or PMOS individual transistors are to be consider whereas parallel combination of NMOS and PMOS are considered in TGL but in CMOS systematic arrangement of NMOS and PMOS is used. Since the alternative CMOS logics had there one drawbacks related to threshold problem and more number of transistors another way of implementing the Static CMOS by using Skewed Gates where it is possible to reduce the size of the transistors instead of reduced number of transistors but obtained the good logic vales for both pullup and pulldown networks by prioritizing the logic values. This paper introduces a novel logic style methodology (i.e. Mixed logic style) for better improvement in power reduction and high speed of operation compared to single-style design. Mixed logic implementation is the new concept for array of gates that means same type of gates are realized with the help of various logic styles. For example, two XOR (Exclusive OR gate) gates are realized by any combination of two logic style (i.e. TGL or Skewed gates) instead same CMOS logic for two XOR gates.

The rest of this paper is as follows. The Low power requirements in Section II. Logic styles in Section III. Section IV presents the Mixed style realization of adder. Section V simulation setup and result discussion different final adder's structures. Finally, Section VI concludes this paper.

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II. LOW POWER REQUIRMENTS

The circuit parameters such as power consumption, speed and wiring capacitance are basically influenced by chosen logic styles [1], [2], [3]. The logic style requirement for the low power is govern by the following fundamental equation.

$$P_{dyn} = V_{dd}^2 \cdot f_{clk} \cdot \sum_n \alpha_n \cdot c_n + V_{dd} \cdot \sum_n i_{sc_n}$$

this power contains the supply voltage(Vdd), frequency(fclk), node(n) capacitance(Cn), switching activity (αn) and node short circuit current(isc). Therefore, these parameters are responsible for reduced power dissipation. Thus the low power circuit implementation of general logic style requirements is discussed here.

In general, the less number of transistors and fewer circuit nodes are necessary for reduced switched capacitors. it is achieved by downsizing of transistor dimensions. Therefore, it is noticed that the chosen logic style must be robust for downsizing of transistors on the noncritical signal paths. On the otherhand, even at low supply voltages, because of voltage scaling, the logic style must be robust for correct function of the gate. Because supply voltage and the logic style are related indirectly in terms of critical signal paths. the switching activity of the circuit is well defined by static or dynamic realization of the circuit. it is observed that static dynamic styles are having less switching activities that dynamic logic styles [2], [9]. The input signal slopes and transistor sizing are strongly effects the short circuit current. The reduction in short circuit current is possible by giving steep and balanced input signal slopes. A good logic style allows decoupling of input and outputs of the logic gates, good driving capability and full signal swings so that it is easy to use and work reliably. Thereby for cell based designs and synthesis of logics are mostly depending on these properties.

Static logic styles are called universal logic style in terms of achieving the robustness compared to dynamic logic styles. even though dynamic logics are having high speed of applications the power con summed by the logic is very hey since it depends on clock pre-charging and evaluation [2]. It is observed that for low power applications static logic styles dominates the counterpart.

III. LOGIC STYLES

Various logic styles are discussed here; the first fundamental circuit implementation is Complementary MOS Logic Style [1], [2]. As it is mention that CMOS follows the generalized architecture which consist of pull up network(pMOS) and pull down network(nMOS) as shown in the Fig. 1(a) and its equivalent circuit shown in Fig. 1(b) represents the resistors and output capacitance. In addition to that the static CMOS is considered for comparisons. It is observed that the greatest advantage of robustness against transistor sizing and voltage scaling is obtained by CMOS logic style implementation. thereby high noise margin and functional operation doesn't depend on the aspect ratio of the transistors. In addition to that since the input signal is directly connected to the gate terminal of the transistor, the cell characterization is an easy task. In spite of these many advantage it is also noticed that number of transistors for functional implementation is high.

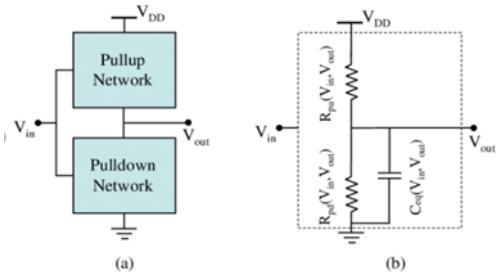

Fig.1.1 (a) General structure of a CMOS gate.
(b) Equivalent circuit representation of the gate

Instead of using both transistors in CMOS it is possible to use anyone of the transistors (either nMOS or pMOS) kind to implement function such logic style is called pass transistor gate as shown in Fig1.2. It is noticed that unlike the input signal is directly connected to the source terminal(A) of transistor where as in CMOS we use power lines for source and drain. Since only one kind of transistor used for implementation less number of transistors are used this is the basic fundamental advantage thereby area power and delay will decreases compared to the CMOS logic counterpart. In spite of less number of transistors it suffers from threshold loss problem which is acknowledged by restoration logic at the output of each function because the maximum output voltage that can be observed Vout=(Vdd-Vtn)

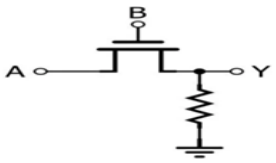

Fig.1.2 Pass transistor

There are several pass transistor logics are developed. the best possible pass transistor logic is Dual Voltage Logic which is to be consider for our comparisons. DVL is basically derived from DPL [10], [11], [12]. The elimination of redundant branches and rearrangement of signals allows the DVL is advantageous compared to DPL. The speed compensation degrades due to PMOS transistors and straightforward full swing operation make it possible to use DVL logic style.

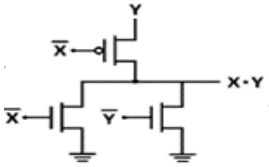

Fig.1.3 DVL based AND gate

Fig 1.3 shows the DVL implementation of AND gate it requires only three transistors to implement it is just like static gate. CMOS with pass gates are also called as transmission gate. Where both nMOS and pMOS are connected in parallel. The basic advantage is that it eliminates the problem of threshold loss by choosing the signal of logic low by nMOS and logic high by pMOS.

In addition to that implementation of XOR and multiplexer are done efficiently by keeping less number of transistors.

CMOS gate with pass transistors offers better realization as shown in the Fig. Implementation of NAND gate or NOR/ AOI or OAI are (monotonic gate) are effective in conventional CMOS architecture because it offers less number transistors nodes and one single inversion level. Whereas non-monotonic gates like XOR and multiplexer are complicated with general architecture. Therefor it is more convenient with mixing of transmission gates and Pass transistors [9], [10].

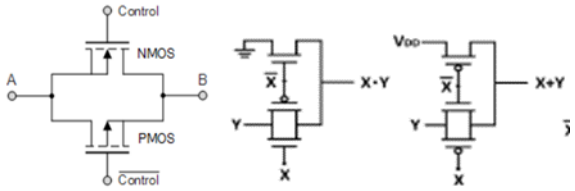

Fig.1.4 (a) Transmission gate (b)TGL AND gate (c) TGL OR gate

As shown in the Fig 1.4(b) and Fig 1.4(c) output is controlled by the control signal. figure 1(b) shows the implementation of TGL AND and TGL OR gates respectively. It is observed that inverters in the propagation path increase the delay drastically so it is necessary and also good practice not has too many complementary inputs. If at all complementation requires like (A'B) and (A'+B) apply complement of A as control signal in transmission gates. Other possibilities for propagation is as shown in the following table.

Table-I: Choosing control signals

Functions	Control signal
A'B	A should be
A'+B	A should be
AB	A or B
A+B	A or B
A'B'	A or B
A'+B'	A or B

Another way of implementing the logic functions using static manner is skewed logic style. in order to improve the speed of the combinational circuits and reduction in the leakage current in certain designs skewed gates are more attractive [1], [6]. The unskewed gates trans-conductance parameters are equal (i.e. βn=βp). This condition allows the capacitor charging and discharging in equal times by providing equal current source and sink capabilities, thereby it maximize the noise margin and the switching threshold will be VDD/2. In otherhand Skewed gates beta ratios are different. For example, Hi-Skew gate's beta ratio follows as βp>βn and Lo-Skew gate's beta ratio is βp<βn. It is also observed that switching thresholds are sifted to right side and left side of VDD/2 respectively.

All the critical paths are realized by the skewed gate technology. The fundamental idea to implement this is making one transition is critical compared to other transition which means that prioritizing the rise output transition or fall output transition. The logical effort is the one the standard method to qualify the gates, here it is necessary to consider the sked gates logical effort so that it is possible to use in the function realizations [7].

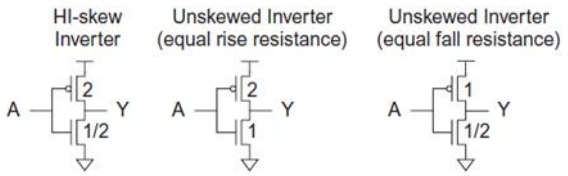

Fig.1.5 Logical effort calculation for HI-skew inverter

The logical effort of the gates is calculated in the following manner. Fig 1.5 shows downsized the nMOS transistor to construct HI-skew inverter. The effective resistant of skewed gate is same as that of unskewed by reducing the input capacitance related to unskewed gate. Therefore, the logical effort of critical transition is reduced by gu =2.5/3 = 5/6. but it is also noticed that noncritical path logical effort will get effected. The logical effort of falling network is calculated by comparing the smaller unskewed inverter with equal pull down currents which is estimated as gd = 2.5/1.5 = 5/3.

The degree of skewing (e.g., the ratio of effective resistance for the fast transition relative to the slow transition) impacts the logical efforts and noise margins; a factor of two is common. Logical efforts of various gates as shown in the Table-II.

IV. MIXED LOGIC STYLE

In digital design one-bit full adder is a fundamental building block which decides the performance of the digital processors [5]. the truth table and mathematical expressions are shown in Fig.2.2. Full adder is a combinational circuit and has got 3 inputs and 2 outputs [4], [6], [8], [14].

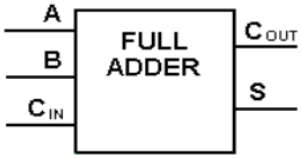

Fig. 2.1 Block diagram

Table-III: Truth table of Full adder

INPUTS			OUTPUTS	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Here A, B, Cin are the inputs and S, Cout are outputs

$S(sum)=A \oplus B \oplus Cin$ (1)

$Cout(carry)=AB+BCin+ACin$ (2)

The logic realization of circuit is as shown in the Fig 2.2. equation (1) is implemented with 2 input XOR gates whereas equation (2) of carry output is realized with effectively using universal gates as follows

Cout(carry)=AB+BCin+ACin (3)
alternatively using NAND gates for carry output as
Cout(carry)={[(A+B) Cin]'. (AB)'}' (4)

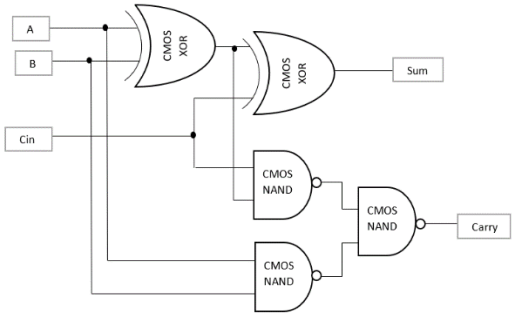

Fig.2.2 Single style realization of full adder

It is observed that all the gates are realized with same CMOS static gates which is known as single style of realization. this implementation requires more number of transistors in spite of full output swing. Another way of realizing the adder using various mixed logic style as shown in following Figures. the basic idea is choosing best logic styles for different gates. Thereby the number transistors reduce and noticed that less power consumption, high performance is possible but in the expanse of extra metal interconnect is required.

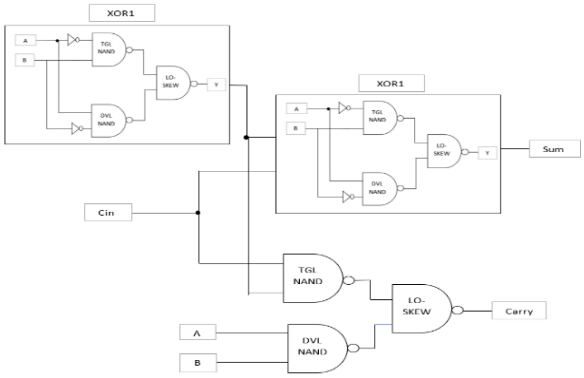

Fig.2.3 FA_Mixed Logic Style-1

As shown in the Fig. 2.3 consists of TGL, DVL and Lo-skew NAND gates. The Lo skew gate output of xor1 is connected to the gate input of xor2 by downsizing the pMOS so that the input capacitance of succeeding stage xor2 is reduced so that the delay of the circuit is decreased. The sum signal and carry output will attain the full output swing without changing the effective resistance.

As shown in the Fig. 2.4 consists of TGL, DVL and Lo-skew NAND gates. The Hi- skew gate output of xor1 is connected to the gate input of xor2 by downsizing the nMOS so that the input capacitance of succeeding stage xor2 is reduced so that the delay of the circuit is decreased. The sum signal and carry output will attain the full output swing without changing the effective resistance.

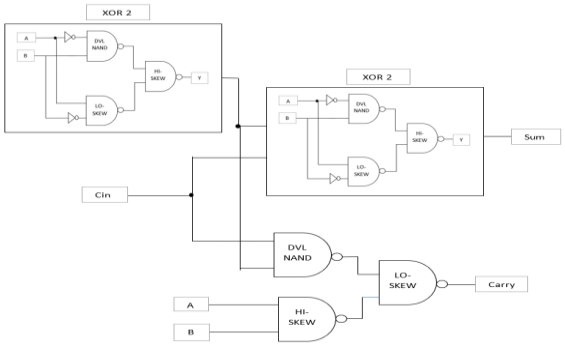

Fig.2.4 FA_Mixed Logic Style-2

V. SIMULATION SETUP

Simulations are performed using H-Spice Synopsis tools. Simulations are done at 0.8v, 1.0v, 1.2 v supplies and under 32nm technology [15]. Power consumption and time delay are calculated using features provided in the H-Spice Software. PDP is calculated as the product of Power consumption and time delay. All circuits are simulated with frequency 2.0 GHz and at a temperature of 25^{o} C and the average power/delay is calculated and presented in each case. All inputs are buffered with balanced inverters (Lon = Lap = 32 nm, Wn = 64 nm, Wp = 128 nm) and all outputs are loaded with a capacitance of 0.2 fF, Furthermore, proper bit sequences are inserted to the inputs, in order to cover all possible transitions.

The simulation wave forma are shown in the Fig.3.1

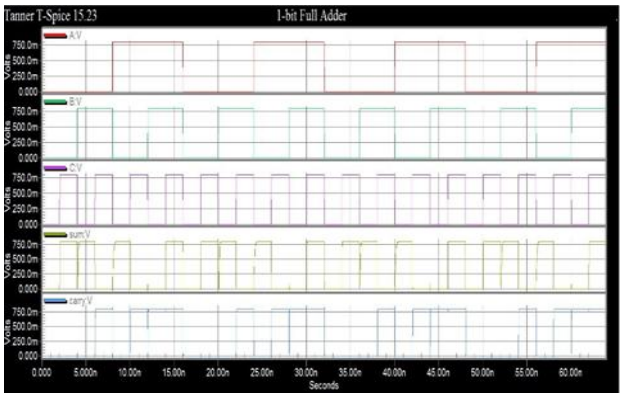

Fig 3.1 Output wave form of full adder.

A. *RESULT DISCUSSION*

The obtained average power consumption and propagation delays are listed below Table-I. It is noticed that FA_Mixed logic style-1 and FA_Mixed logic style-2 has the percentage of average power consumption reduction at supply voltage 0.8v as 77.95%, 83.53% compared to static single style CMOS respectively. At 1.0v supply the power reduction is 76.51%, 80.76% respectively. Similarly, at 1.2v supply the average percentage power reduction is 67.14%, 80.09% respectively.

It is also observed that FA_Mixed logic style-1 and FA_Mixed logic style-2 has the percentage of propagation delay reduction at supply voltage 0.8v as 14.02%, 13.98% compared to static single style CMOS respectively. At 1.0v supply the power reduction is 12.80%, 12.13% respectively.

Similarly, at 1.2v supply the average percentage power reduction is 12.11%, 11.60% respectively.

Finally, the PDP of the circuit is calculated by taking the product of average power consumption and propagation delay for each and every power supply values. the percentage improvements are as shown follows.

The graphical representation of results is shown in the Fig3.2, Fig 3.3.

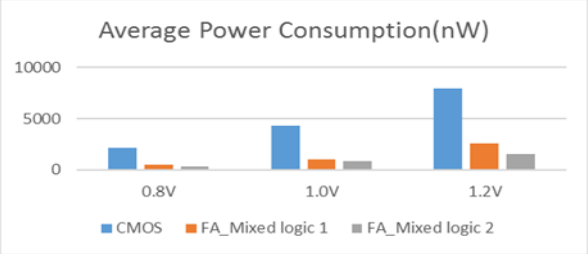

Fig. 3.2 Average Power Consumption

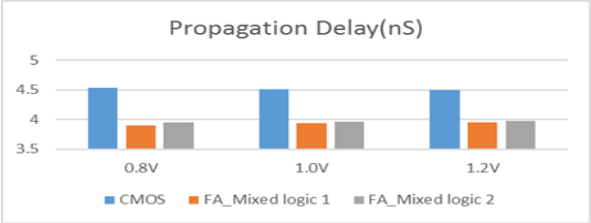

Fig. 3.3 Propagation Delay

FA_Mixed logic style-1 and FA_Mixed logic style-2 has the percentage of PDP reduction at supply voltage 0.8v as 81%, 85% compared to static single style CMOS respectively. At 1.0v supply the PDP reduction is 67.14%, 80.09% respectively. Similarly, at 1.2v supply the PDP reduction is 71.13%, 82.40% respectively.

Table-II: Logical efforts of basic gates.

Gate type	Un-skew CMOS gates					HI-skew CMOS gates					LO-skew CMOS gates				
	Number of Inputs					Number of Inputs					Number of Inputs				
	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5
Inverter	1					5/4					1				
NAND		4/3	5/3	6/3	7/3		3/2	7/4	12/6	27/12		3/2	4/2	5/2	6/2
NOR		5/3	7/3	9/3	11/3		9/4	13/4	15/4	21/4		3/2	4/2	5/2	6/2
XOR/XNOR		4	12				3	9				4	12		

Table IV: Comparison of Average power, propagation delay and PDP of various technologies

1-bit Full Adder	Average Power (in nW)			PropagationDelay (in ns)			PDP (x106 pJ)		
	0.8v	1.0v	1.2v	0.8v	1.0v	1.2v	0.8v	1.0v	1.2v
CMOS	2145.19	4293.72	7928.08	4.537	4.515	4.497	9732.7	19386	35652
Mixed logic style-1	472.979	1008.37	2604.43	3.901	3.937	3.952	1845	3969.9	10292
Mixed logic style-2	353.232	826.048	1577.97	3.948	3.967	3.975	1394.5	3276.9	6272.4

VI. CONCLUSION

This paper has introduced an efficient implementation of Binary adder using Mixed logic style which combines the TGL, Hi-Skew, Lo-Skew and DVL logics. Mixed Logic Style offers the greatest advantage of low power dissipation compared to single static style realizations and also improved power delay compared to conventional CMOS styles. A variety of comparative spice simulations was performed at 32 nm, verifying, in most cases, a definite advantage in favor of the proposed Mixed Logic designs. The proposed adder is suitable where low power and high speed is predominant since it offers 83.53% reduced power dissipation and 14.02% decreased propagation delay compared to conventional static CMOS logic style. Therefore, the proposed mixed logic style binary adder is used to as basic building blocks in the design of larger decoders, multiplexers, and other combinational circuits of varying performance requirements. Moreover, the presented reduced low power characteristics can benefit both bulk CMOS and SOI designs as well.

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