Next Generation Logic Gate Designs using Improved Polarity Control Bipolar Junction Transistor

Lokesh Kumar Bramhane, Santosh D. Chede, Premanand K. Kadbe, Balasaheb Patil, Sudhir B. Lande

Abstract*: In this paper, we have proposed a dopingless reconfigurable polarity control bipolar junction transistor (PC-BJT) with enhanced current gain and currentoff frequency. It can be used as both n-i-n or p-i-p type transistors by applying an appropriate voltage (±1 V) on its polarity control electrodes. It is very first time that BJTs are used to implemented in XOR logic gate design with the concepts of reconfigurability and polarity control electrodes. For this, a new symbol is introduced to demonstrate the behavior of logic gates. Moreover, series and parallel combination of the proposed device exhibits the behavior of two-input NAND-NOR (PC=+1 V) and AND-OR (PC=-1 V) gates. Moreover, the proposed device exhibits the low on-time voltage and improved breakdown voltage compared to the conventional PC-BJT.

Keywords: On-time voltage, reconfigurability, polarity control · logic gates, current gain, cut-off, frequency, TCAD Simulator.

I. INTRODUCTION

Bipolar junction transistors have emerged as most favorable candidates for investigating the analog amplifiers as well as the mixed-mode circuits. It has paved the way for BiCMOS devices due to their efficient control on high current gain and cut-off frequency. Moreover, high package density of these devices made it the firstchoice for the integration with CMOS [1] [2]. To make the bipolar process more compatible to CMOS process, lots of efforts have been made to eliminate the problem of high thermal budget requirement during the doping process. Such a doping-free device named symmetric bipolar charge plasma transistors (BCPTs) proposed in [3] that have had eliminated the associated problems during the doping process and because of symmetric nature, it is now possible to exchange the emitter and collector electrodes like source-drain electrodes of MOSFETs [4]. But, these doping-free devices require different work function metals to induce the charge carriers at targeted regions. It means that using the work function engineering or charge-plasma (CP) concept has certain limits. Although, to solve this problem, electrostatic polarity control (PC) concept has also been initially proposed that doped the required amount of dopants in pre-specific regions for carbon nanotube field-effect

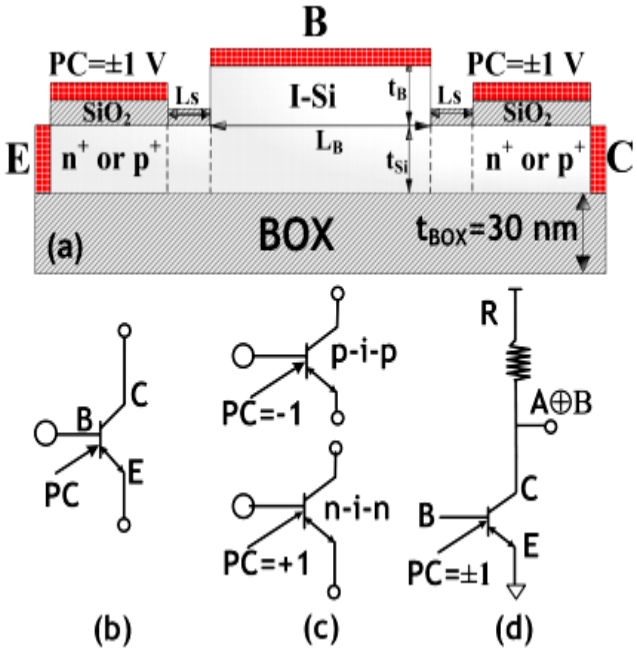

Fig. 1 (a) Cross sectional views of lateral symmetrical polarity control bipolar junction transistor (PC-BJT). (b) Symbol of PC-BJT. (c) p-i-p (PC=-1) and n-i-n (PC=+1). (d) XOR gate.

transistors (CNFETs) [5]. PC concepts widely reported in literature for reconfigurability-the capability of changing the polarity (n or p type) [6]. Moreover, to exploit full benefits of this concept, configurable BJT have also been built to exhibit switching between n-i-n to p-ip and vice versa [7] [8]. Hence, due to polarity control, problems associated with CP concept in BJT devices have now been resolved, and also have opened the integration possibility with other devices [9] [10] [11]. However, β of PC based devices are very poor compared to those devices that are based on CP concept. Moreover, very high on-time voltage (>0.6 V) required to switch-on the PC based devices results increment in input voltage required to extract both current gain (β) and cut-off frequency (f_T) [7].

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***** Correspondence Author
Lokesh Kumar Bramhane*, department of E&TC, VPKBIET Baramati, Pune, India. Email:lokesh.bramhane@vpkbiet.org
Santosh D. Chede, Department of E&TC, VPKBIET Baramati, Pune, India. Email:santosh.chede@vpkbiet.org
Premanand K. Kadbe, Department of E&TC, VPKBIET Baramati, Pune, India. Email:premanand.kadbe@vpkbiet.org
Balasaheb Patil, department of E&TC, VPKBIET Baramati, Pune, India. Email:balasaheb.patil@vpkbiet.org
S. B. Lande, department of E&TC, VPKBIET Baramati, Pune, India. Email:sudhir.lande@vpkbiet.org

Hence, in searching the best and to resolve aforementioned issues, we have proposed a polarity control bipolar junction transistor with reduced on-time voltage to minimise the switching power. Moreover, implementation of logic gates (XOR, OR and NAND) using reconfigurability concept is also demonstrated with fewer resources. A new symbol for PC-BJT is also proposed for easy understanding of the functionality of these logic gates. Apart from this, β and f_T of the proposed device are now greater than the conventional device based on polarity control. β and f_T of the proposed PC-BJT are of 3177.86 and 545 GHz compared to conventional device (78 and 423.8 GHz). Also, on-time voltage of the proposed PC-BJT is now reduced to 0.45 V.

II. STRUCTURE AND SIMULATION PARAMETERS

Polarity control technique facilitates the creation of electron and hole concentrations at the specified regions (emitter or collector). When the PC electrodes are biased with the positive or negative voltage accordingly it proposed device forms n-i-n or p-i-p type structures of BJT. For example, to induce electron concentrations to form the n-type region, PC electrodes should have to be bias with positive voltage and if it is biased with a negative voltage, it results in accumulation of hole concentration to form the p-type region. Fig. 1(a) shows crosssectional view of the proposed polarity control bipolar junction transistor (PC-BJT), where LB, n+ or p+, tSi, and tB represent the length of base region, emitter or collector regions, silicon thickness, and extended base height, respectively. In contrast to the conventional device based on polarity control [7], the proposed PC-BJT structure differs in terms t_B, t_{Si}, L_B, emitter/collector length (L_E/L_C) and intrinsic gap presence between the emitter-base and base-collector regions. After, all these modifications, the overall length of the proposed device are now reduced to 190 nm compared to the overall length of the conventional device (199 nm). Rest all parameters of both devices have been shown in Table 1. Moreover, silicon film is uniformly doped with p-type impurity (1×10^{13} cm^{-3}). For the base region, electronhole concentrations under thermal equilibrium (V_{BE} = V_{CE} = 0 V) have shown in Fig. 2(a). Under thermal equilibrium, induced electron or hole concentrations in the emitter or collector regions of PC-BJT are the order of 4×10^{19} cm^{-3} and can be controlled by varying the voltage across the PC electrodes. Apart from this, a SiO2 layer is introduced between the emitter and collector

Table- II: Device Parameters

Parameters	*Proposed PC-BJT*	*Conv. PC-BJT*
Base length (*LB*)	120 nm	98 nm
Extended base width (*tB*)	20 nm	15 nm
Emitter or Collector length	30 nm	45.5 nm
Si thickness (*tsi*)	30 nm	20 nm
Intrinsic Gap	5 nm	5 nm
SiO2 thickness (*tSiO2*)	5 nm	5 nm
Polarity control voltage (PC)	+1 V (n-i-n) & -1 V (p-i-p)	+1 V (n-i-n) & -1 V (p-i-p)

contact metals and the silicon film to make the distribution of electrons or holes more uniform. Cutlines were made 2 nm below from the interface of Si-SiO2. Throughout the TCAD simulation of the proposed PC-BJT, we have incorporated the Selberherr (SELB) model to evaluate the electric field [12]. KLAASSEN model included to consider the effect of carrier scattering [13]. Further, auger (AUG) model calculates the dissipated energy for generation-recombination process [14]. To accurately model the β and the thermally generated electron-hole pair of the proposed PC-BJT, band gap narrowing (BGN) model and Shockley-Read-Hall (SRH) model have been incorporated with intrinsic carrier lifetimes

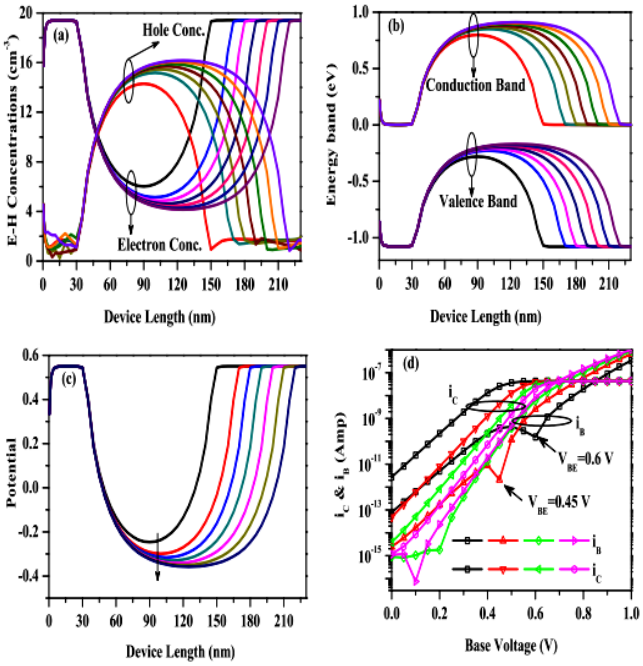

Fig. 2 (a) Electron-hole distribution, (b) energy band diagram, and (C) potential variation of PC-BJT under thermal equilibrium for increasing base length from 98 nm-160 nm. (d) Gummel plot.

n_{ie} = n_{ih} = 0.2 µs [15] [16]. Process resistances of the base, emitter and collector contacts are assumed negligible for rest of the simulation [17] [18].The electrical characteristics of the proposed and conventional devices are simulated and compared using SILVACO ATLAS (2-D Device simulator) and SPICE [14].

III. RESULTS AND DISCUSSION

The effective base length is the limiting factor in scalability of the BJT devices which should be wide enough to accommodate depletion layers across the base-emitter and base-collector junctions that can play a significant role tocharacterize the device parameters. Further, hole concentration at base region increases due to increment in base length; as a result, depletion width decreases that reduces the potential across both the junctions. Fig. 2(a) demonstrating the increment in hole concentration with base length variation.

Moreover, the decrement in potential at base-emitter junction results reduction in on-time voltage of the proposed PC-BJT which is illustrated in Fig. 2(c). While improves the breakdown voltage due to decrement in potential across the base-collector junction. Also, under the thermal equilibrium (V_{BE} = V_{CE} = 0 V), due to increment in hole concentration, the energy band diagram of the proposed PC-BJT at the base region demonstrates the upward shifting

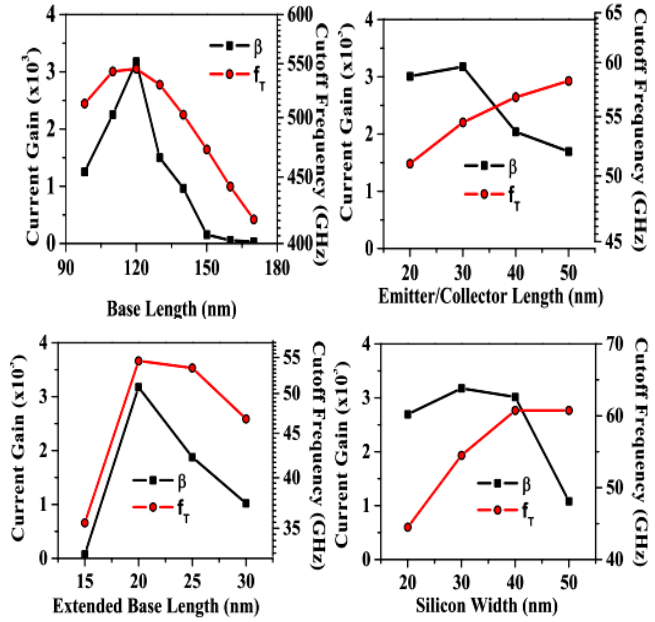

Fig. 3 Current gain (β) and cut-off frequency (f_T) of proposed PC-BJT with variation in (a) physical base length, (b) emitter/collector length, (c) extended base width (t_B), and (d) silicon width (t_{Si}).

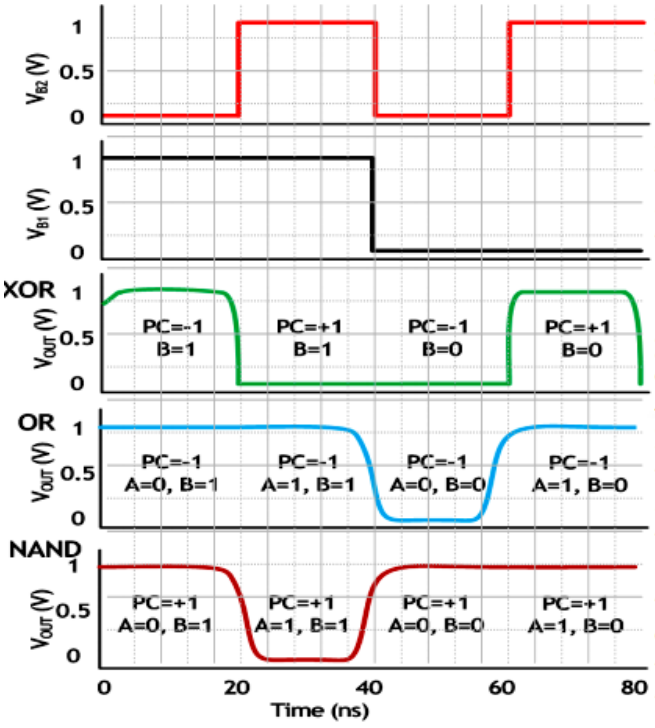

Fig. 4 Input-output voltage waveform in time-domain for NAND and XOR gates.

of both conduction band and valence band which is illustrated in Fig. 2(b).

Gummel plots for different base lengths of PC-BJT have been shown in Fig. 2(d) to justify again the reduction in on-time voltage and to see the impact on β. From the Gummel plot, it can be observed that ontime voltage is decreasing with increment in the base length. However, appropriate selection of base length is very important as it also affects both β and f_T of the proposed device. Therefore, as shown in Fig. 3(a), both β and f_T were estimated for the proposed PC-BJT as a

Table- II: Input-output combination of OR, NAND, and XOR gates

B1	B2	OR	NAND	PC	B2	XOR
0	0	0	1	-1	0	0
0	1	1	1	-1	1	1
1	0	1	1	+1	0	1
1	1	1	0	+1	1	0

Table- III: Comparision of current gain, cut-off frequency and on-time voltage

Parameters	Proposed PC-BJT	Conv. PC-BJT
β	3177.86	78
f_T(GHz)	545	423.8
On-time voltage (V)	0.45	0.62

function of base length variation. It can be inferred that both β and f_T are decreasing beyond the base length of 120 nm. Moreover, at the optimised base length of 120 nm, on-time voltage of the proposed PC-BJT is 0.45 V which is 28 % less than the device demonstrated in [7]. Beyond the optimised base length, on-time voltage of the proposed device decreases but there is a degradation in both β and f_T , hence we chosen base length as 120 nm for the rest of the simulation. Moreover, β and f_T have the contradictory relation with variation in emitter or collector length. But beyond 30 nm, fT increases and there is a degradation in β which is shown in Fig. 3(b). Moreover, extended base length plays an important role in base capacitance reduction which is the inverse of f_T . Hence, both f_T along with β have also been optimized for extended base width and demonstrate their peak value at the extended base width of 20 nm as illustrated in Fig. 3(c). Apart from this, silicon width has also been optimized and a contradictory relation between β and fT was again found with increment in silicon width as shown in Fig. 3(d). Also, Fig. 5 illustrates the value of base-emitter voltage (ontime voltage) along with base and collector currents as a function of base length to make the picture clearer. For the proposed PC-BJT, finally optimized device dimensions are: L_B = 120 nm, $L_{E/C}$ = 30 nm, t_B = 20 nm and t_{si} = 30 nm. Moreover, extracted results are summarized in Table 3.

Moreover, using proposed PC-BJT having on-time voltage of 0.45 V, β of 3177.85, and f_T of 545 GHz, a fully functional XOR logic gate is also investigated to explore the reconfigurability concept which is shown in Fig. 1(d). Due to reconfigurability, PC-BJT can exhibit switching between n-i-n to p-i-n and vice versa as shown in

Fig. 1(b) and Fig. 1(c). When PC terminal is biased with +1 V, there is an accumulation of electrons at emitter and collector regions that forms n-i-n type transistor, and when it is biased with -1 Volt, there is a an accumulation of holes at emitter and collector region then p-i-p type transistor come into in existence.

XOR gate is implemented using the recently explained biasing of PC electrode along with the biasing of base electrode. For this, PC electrode is biased with -1 Volt and base electrode is set to 0 Volt, then PCBJT act as a p-i-p type transistor and due to 0 volt at the base electrode, the transistor will be in ON-state and logic output '0' is obtained

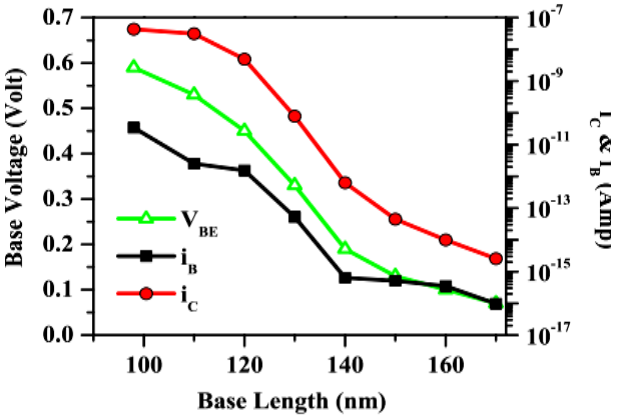

Fig. 5 Base-emitter voltage, collector current, and base current with variation in base length of the proposed PC-BJT.

(Fig. 1(d)) and due to 1 volt at the base electrode, transistor will be in OFF-state, and logic output will become '1'. Moreover, when PC electrode is biased with +1 Volt, and the base electrode is set to 0 Volt, then PC-BJT act as an n-i-n type transistor and due to 0 volt at the base electrode, transistor will be in OFF-state and logic output '1' is obtained. And due to 1 volt at the base electrode, transistor will be in ON-state and logic output will become '0' that also can be understood through the Table 2. Hence, by this way XOR logic gate can be easily implemented using single transistor (PC-BJT) with the help of reconfigurability concept.

For the realization of NAND logic gate, there is a requirement of two PC-BJT connected in series. When PC electrode is set or biased with +1 Volt then both transistors will act as n-i-n type, if we apply +1 V to both inputs (i.e. B1 and B2) then both the series transistors will be in ON-state and logic output '0' is obtained. And if both inputs (i.e. B1 and B2) are biased with 0 volt then both transistors will be in OFF-state and logic output '1' is obtained. If either of its two inputs is high then it will give a high output. However, to implement the logic gate OR, PC electrode should have to be biased with -1 Volt then both transistors will act as a p-i-p type. If we will apply +1 V to both inputs (i.e. B1 and B2) then both the series transistors will be in OFF-state and logic output '1' is obtained. And if both inputs (i.e. B1 and B2) are biased with 0 volt then both transistors will be in ON-state and logic output '0' is obtained. If either, but not both, of its two inputs are high then it will give a high output. By this way, we are able to implement NAND and OR gates by forcing PC electrode to +1 and -1 Volt, respectively. Apart from this, the input-output waveforms of logic gates (XOR, OR, and NAND) are also have shown in Fig. 4 with possible input-output combinations.

IV. CONCLUSION

In this paper, we have proposed a symmetric PC-BJT with reduced on-time voltage, high breakdown voltage, high current gain, and cut-off frequency. Moreover, using single transistor, we have successfully demonstrated the implemented XOR logic gate. Also, using the series combination of two same proposed devices, NAND and OR logic gates are also implemented. For this, a proposed symbol for PC-BJT is very useful to elaborate functionality of different logic gates.

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AUTHORS PROFILE

Lokesh Kumar Bramhane received the B.E. degree in Electronics and Telecommunication Engineering from the Shri Govindram Seksaria Institute of Technology and Science, Indore, India, in 2007. He has completed his M-Tech degree in VLSI & Embedded System Design from NIT Bhopal in 2012. He has received his Ph.D. in 'Performance Projection and Analysis of Dopingless Configurable Bipolar Junction Transistors' under the supervision of Dr. Jawar Singh in the Department of Electronics and Communication Engineering, PDPM Indian Institute of Information Technology Design and Manufacturing, Jabalpur, India. He is currently working as an Assistant Professor in E&TC department of VPKBIET, Baramati-Pune.

Dr. Santosh D. Chede received his B.E. degree in Industrial Electronics and M.E. in Electronics in 1990 and 2000 resp. from SGB Amravati University and completed DIM, PGDIM, PGDHRM and MBA from IGNOU. He has been awarded PhD on "Low power design aspects of Embedded System: A case study of Implantable pacemaker" from Visvesvaraya National Institute of Technology (VNIT) Nagpur in 2010 under the guidance of Dr. K.D.Kulat. He has more than 26 years of teaching experience and guided UG and PG projects. He was a chairman Board of Studies (Electrical Engg.) at RTMNU, Nagpur University.

Premanand K. Kadbe received his BE degree in E&TC in 2 003 from Amravati University, and M.Tech. in the Electronics Engineering in 2007 from R.S.T.M. Nagpur University. He has industrial experience of 2 years and teaching experience of 8 years. Premanand is a Reviewer and Member of Editorial Board for various International Journals and Conferences, and a life member of MIE, IETE and ISTE. He had reviewed 78 peer International Journal and Conference Papers. Premanand attended various workshops on VLSI, Communication and Embedded Systems at Govt. Institutes, IIT, NIT, and private institutes. Presently Premanand is an Assistant Professor in Electronics and Telecommunication department.

Balasaheb Patil has received his graduate degree in Electronics and Telecommunication Engineering in 2004 and M.E. in the Microwave Communication Engineering in 2010. He is pursuing PhD in Savitribai Phule Pune University. He has Industrial experience of one year in R & D and teaching experience of 11 years. He has guided various projects in Digital Image Processing, Instrumentation and Communication. His project on "Prepaid Energy Meter" has won 2nd prize in "Avishkar" at National level competition. He is working as ISTE coordinator. His areas of interests include Digital Image Processing and Microwave Engineering.

Dr. S. B. Lande acquired B.E. (Electronics Engineering.), from KITS, Ramtek, Nagpur University in 1996 and M. Tech. in Telecommunication System Engineering (TSE) from IIT, Kharagpur in 2002. He has been awarded Ph.D. on "Resource Allocation and Management in OFDMA with CSI and QoS for Next generation wireless Network" by RTM Nagpur University in 2014. He has worked as a HOD for more than 3 Years, Professor in-charge for NBA work, Vice Principal and handled many more responsibilities.