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A Low Input Referred Noise Dynamic Comparator for High Speed Applications

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***Abstract*: Comparators play a pivotal role in design of analog and mixed signal circuits. Comparators employ regenerative feedback both in input pre-amplifier stage and output stage. The designed comparator resolves 5mV with resolution of 8 bits and dissipates 11mW of power using 1.2V supply in 130nm CMOS technology while operating at clock frequency of 1.25 GHz.**

***Keywords* : Dynamic comparator, offset voltage, kickback noise.**

I. INTRODUCTION

Comparators are used in the design of analog to digital converters resolving the bits based on the required resolution. The main constraints involved in the design of comparator varies with application and resolving time. Operational transconductance amplifiers work as high speed comparators in open loop but with reduction of minimum channel length the available voltage headroom is reduced which reduces both gain and voltage swing. Circuit's topology such as cascode when use in output stage in Op-amps reduce the available swing. Applications such as RF receiver and data converters have power dissipation as bottle neck hence use of comparator for such design needed to exercised due caution. The need for power reduction has opened the circuit design to look for topology such as dynamic comparator [2],[3],[4],[5],[6].

Conventional dynamic comparator

Operation:

There are many circuits of dynamic comparators. The basic circuit of conventional dynamic comparator is shown in Fig.1.

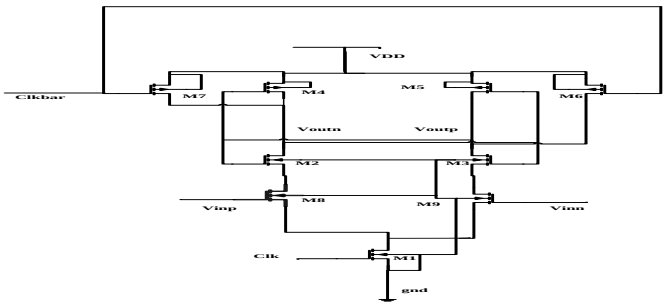

Fig.1 Schematic of conventional dynamic comparator

The operation of above circuit is as follows, initially when clk is low, transistors M1,M8,M9 operate in cutoff region and transistors M7 and M6 are turned on[4]. This phase of operation is reset phase. Nodes Voutp and Voutn are now pre charged to supply potential. In the next clock phase i.e. when clk is high transistors M1, M8 and M9 begin to turn on and draw current. The voltage stored across parasitic capacitance present at the output nodes begins to change according to the differential input voltage. After certain amount of time the cross coupled pair start to operate until one of the transistor turns off and other turns on completely[7]. This is the regenerative phase. There are certain problems associated with the above circuitry such as kickback noise and limited gain. The kickback noise is due to low impedance path between the output nodes and inputs due to parasitic capacitance[8].

II. CONVENTIONAL DOUBLE TAIL DYNAMIC COMPARATOR

Operation:

The circuit of conventional double tail dynamic comparator is shown in Fig.2. When clk is low the transistors M1,M2 M3 and M12 are in cutoff region, transistors M4,M5 are turned on . So there is no power dissipation[9]. The intermediate nodes vp1,vn1 (gate nodes of transistors M6 and M7) pre-charged to supply voltage which in turn turns on transistors M6,M7 which pulls the output nodes Voutp and Voutn low. This is the reset phase of comparator. When clk is high transistors M1,M12 are turned on. The voltage stored across parasitic capacitance present at the intermediate output nodes vp1,vn1 begins to change according to the differential input voltage. According to difference of voltage across vp1,vn1 nodes transistors M6 and M7 starts discharging the Voutp and Voutn nodes. As clkbar is low transistor M12 is turned on .The two cross coupled transistors form a positive feedback loop and the voltages ross nodes starts to regenerated according to input voltage difference. The problem of kickback noise is reduced by adding M6 and M7 transistors.

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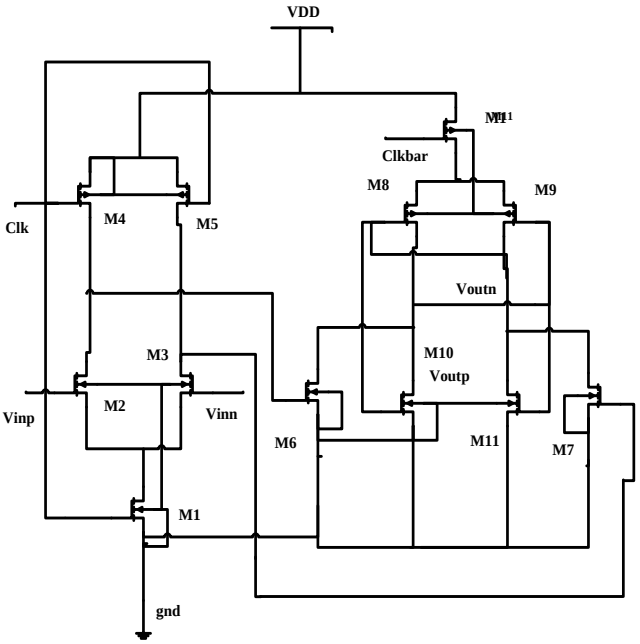

Fig.2 Schematic of Conventional dual tail dynamic comparator

The output of conventional dual tail dynamic comparator is shown Fig.3. An input differential voltage,vid 5mVapplied at the input of comparator. When clk is low, the comparator is in reset phase, so both output are discharged to ground. When clk is high both the output nodes start to rise until t_0 after which one of output discharges while other charges to the supply.

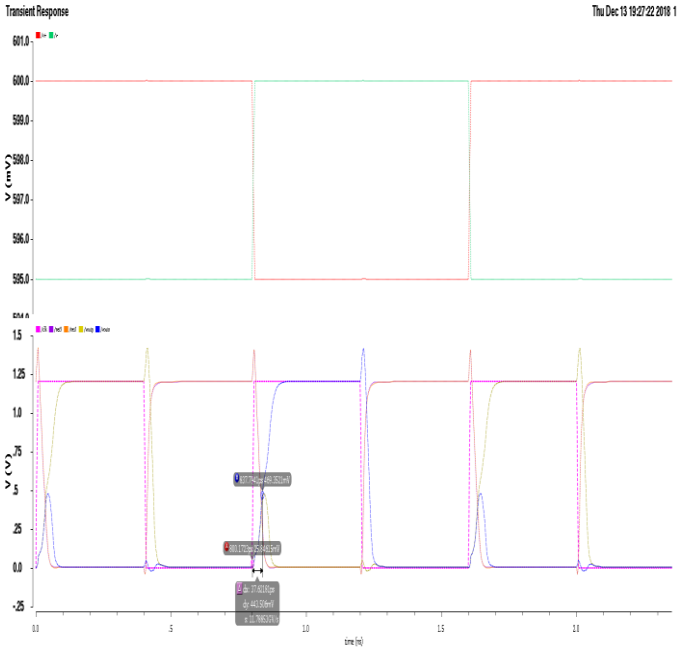

Fig.3 Output of conventional double tail comparator

III. DOUBLE REGENERATIVE DOUBLE TAIL COMPARATOR

Operation:

The circuit of double regenerative double tail comparator is shown in Fig.4. The operation is as follows, when clk is low transistors M16 , M3 ,M4,M1,M2 are turned off. The intermediated nodes voutp1, voutn1 are pre charged high to the power supply which turns on the transistors M10,M11 which pulls the output nodes low. This is the reset phase. When clk is high transistors M1,M3 are turned on. The voltage stored across parasitic capacitance present at the output nodes begins to change according to the differential input voltage. According to difference of voltage across Voutp1,Voutn1 nodes transistors M10 and M11 starts discharging the Voutp and Voutn nodes. As clkbar is low, the two cross coupled transistors form a positive feedback loop and the voltages across nodes starts to regenerate according to input voltage difference. When nodes voutp1 and voutn1 have discharged sufficiently low to turn on transistors M14,M15. The two transistors M14,M15 form a cross coupled pair. The potential across output nodes Voutp and Voutn start to increase until the two transistor M12 and M13 turn on. The two inverter pairs formed by transistors M14,M13 and M15,M12 form a cross coupled pair. This is regenerative phase. The time required to regenerate decreases as gain is increases already in the input preamplifier stage due to the cross coupled pair formed due to transistors M2,M7 and M8,M3. The gain of this circuit is increased compared to circuit shown in Fig.2. The output of double regenerative double comparator is shown in Fig.5. The input vid of 5mV is applied to across gates of transistors M4.M5. The output nodes Voutp,Voutn is low when clk is low. When clk is high, the both the outputs start to increase until the cross coupled pair regenerate after time t_0.

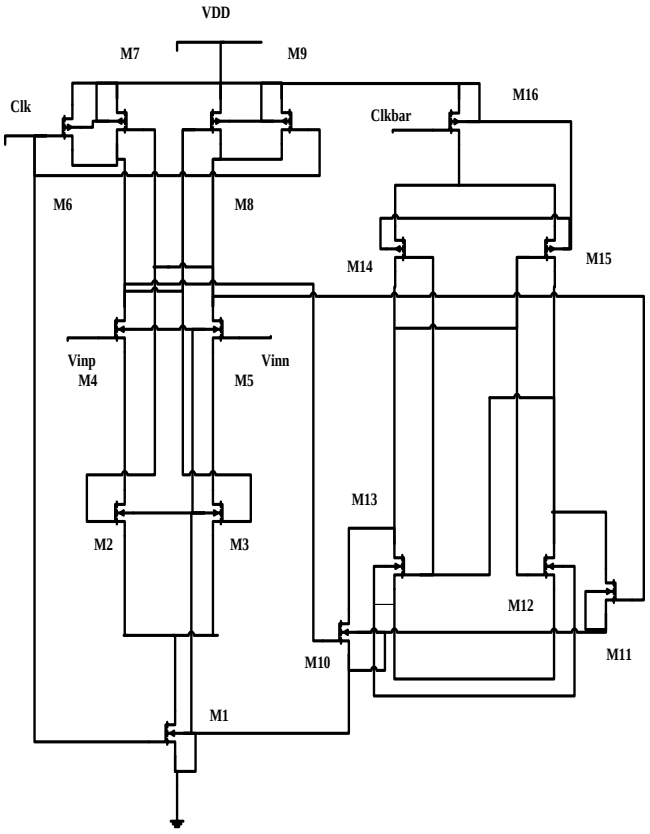

Fig.4 Double regenerative double tail comparator

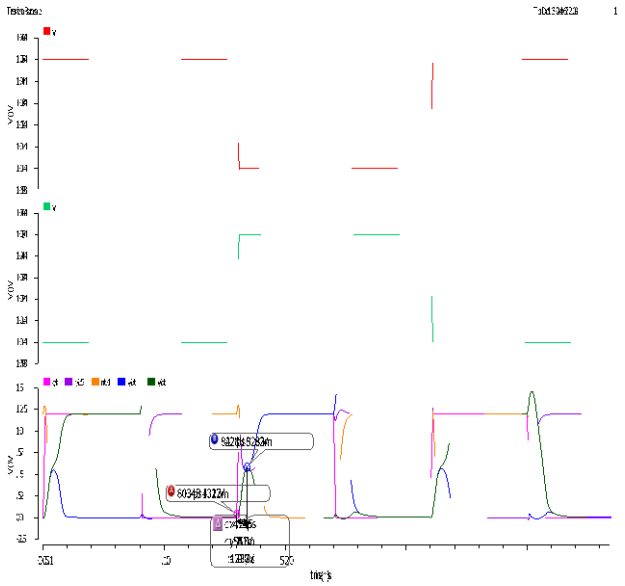

Fig.5 Output of double regenerative double tail comparator

IV. PROPOSED REGENERATIVE DYNAMIC COMPARATOR

Operation:

The circuit of proposed regenerative dynamic comparator is shown in Fig.6. Initially when clk is low transistors M1,M2,M3, Mtail, are turned off and transistors M7,M8 are turned on. The intermediate output nodes voutp1,voutn1 are pre-charged high. The output nodes are pull low as transistors M11,M12 are turned on. As clock is high, transistors M1 Mtail is turned on, the transistors M6,M9 begin to turn on as the node voltages begin to drop , which turns in turn turns on the cross coupled pair formed by transistors M6,M9. When the intermediate nodes begins to rise the transistors M2,M3 begin to turn on, the two inverter pair M6,M2 and M9,M3 form a cross coupled pair further boosting the gain. The gain is boosted in output stage by gain boosted cascode which is class c inverter configuration. The circuits here employs gain boosting which increases the output resistance. The back to back connected gain boosted cascode stages are in positive feedback loop which further increases the gain. The output wave forms of proposed regenerative dynamic comparator is shown in Fig.7. Input differential voltage vid of 5mV is applied to input of comparator. When clk is low the intermediate nodes voutp1, voutn1 are pre-charged high, which pulls the output nodes low. This phase is reset phase of the comparator. When clk is high the tail current sources are turned on. The gain is increased input preamplifier stage, which reduces the kickback noise which is discussed shortly. All the above discussed comparator's have rail to rail signal excursions at the output nodes. This causes the kickback noise. The high speed and power efficient dynamic comparator architectures gives the author to explore technique to reduce kickback noise. There are many circuit topologies present to minimize the effect of kickback noise, mostly all or one technique is followed to reduce the same.

1. As the voltages across the drains of signal transistors change in opposite direction to input, so the signal can be coupled back to the input in opposite direction, this topology is neutralization techniques.
2. The second technique is to provide a low impedance path from the output pre-amplifier stage to ground during pre-charge phase. This disables the path between the regenerative stages and pre-amplifies stage.

The Proposed technique uses class-C inverter stage as output. As output resistance is increased the kickback noise is attenuated by as factor of gain. This reduces the kickback noise. The circuit used for show increase in output resistance due to gain boosting is shown in Fig.8.

The transistors M3,M1 form cascade amplifier, while transistor M2 is used for gain boosting. The currents i1,i2,i3 are the currents flowing through the transistors M1,M2,M3.

As the current i is a function of input gate to source voltage and drain to source voltage the mathematical analysis is shown by equations. It gain be seen that the output resistance is boosted by a factor of A2*A3, where A2 and A3 are the self -gains of M2 and M3 transistors.

$$i1 = gm1 * f(vgs) + gds1 * f(vds) \quad (1)$$

$$i1 = gm1 * 0 + gds1 * v2 \quad (2)$$

$$i1 = v2 * gds1 \quad (3)$$

$$i3 = gm3 * (v2 - v1) + gds3 * (v0 - v1)$$

$$i3 = gm3 * v2 - v1 * (gm3 + gds3) + gds3 * v0 \quad (4)$$

$$v1 = rds1 * i1$$

$$v2 = v * gm2 * rds2 \quad (5)$$

As $i1 = i3$

$$(vo / i1) = rout = rds1 * (A3 + 1) - rds1 * A2 * A3$$

$$rout = rds1 * A2 * A3 \quad (6)$$

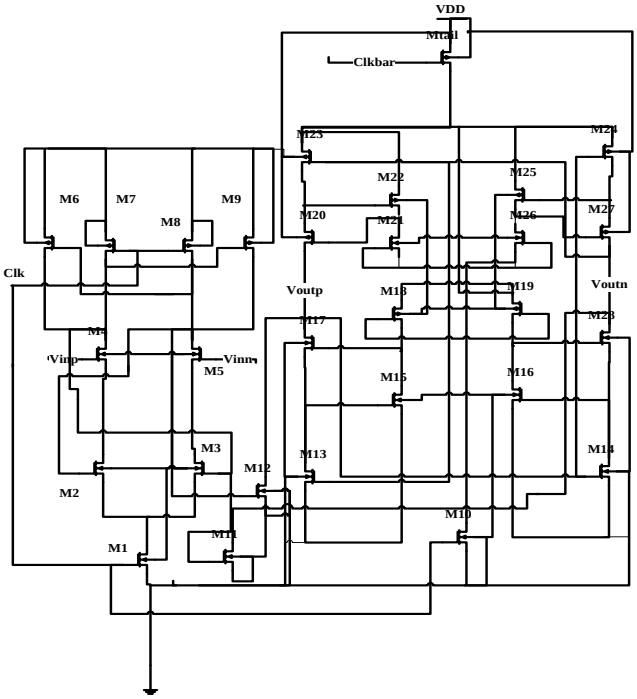

Fig.6 Proposed regenerative dynamic comparator

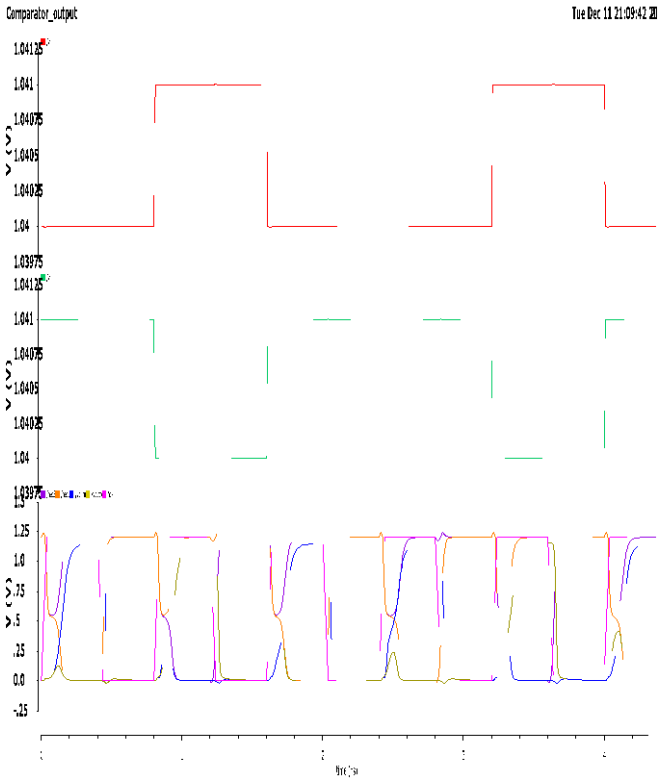

Fig.7 Output of proposed regenerative dynamic comparator

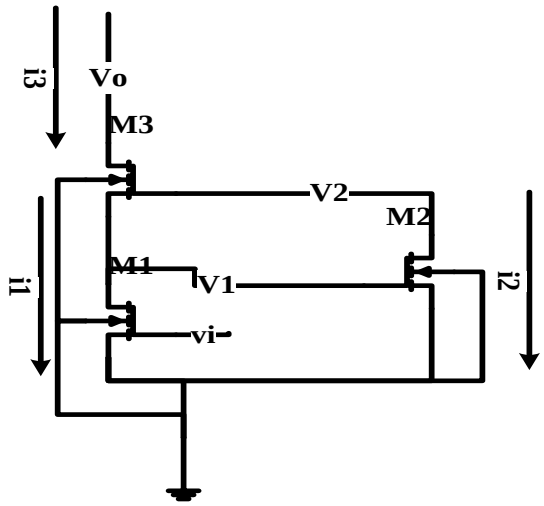

Fig.8 Circuit used calculating output resistance in proposed regenerative dynamic comparator

V. RESULTS AND DISCUSSION

The designed comparator exhibits offset voltage of 0.59mV of offset without cancellation. The output is measured using Monte Carlo sampling method for 200 samples and can be seen in Fig.9.

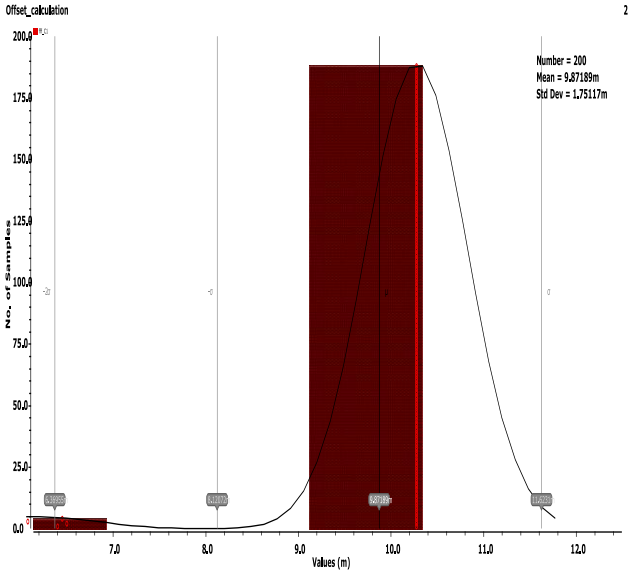

Fig.9 Output offset of proposed regenerative dynamic comparator

The designed circuit shows a kickback noise of 25.6e-6V by following the procedure used in [1].

The input referred noise of circuit is

$$\bar{V}_{n,in}^{2} = \left(\left(\frac{4kT}{gm}\right) + \left(\frac{k}{(c_{ox})(W*L)}\right)\frac{1}{f}\right) + \left(\frac{4KT}{(g_m^2)R_0}\right) \quad (7)$$

Where R_0 is the output resistance of gain boosted stage. The layout of proposed comparator is shown in Fig.10. The obtained results are compared and summarised in TABLE I.

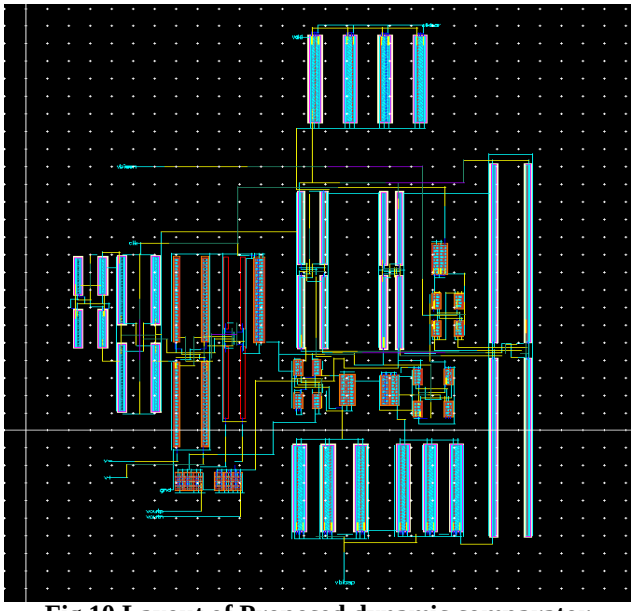

Fig.10 Layout of Proposed dynamic comparator

Table I

Reference	[3]	[5]	This work
Technology	180nm	65nm	130nm
Supply Voltage	0.8V	1.2V	1.2
Clock frequency	2.4GHz	500Mhz	1.25Ghz

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Resolution	-	-	8bits
Offset 3-sigma standard deviation	-	2.075mV	1.75mV
Output referred voltage	-	-	183.37e-6 V
Kickback noise	43mV	-	29e-6V

VI. CONCLUSION

This paper describes gain boosted comparator which has the advantages of low input referred noise, low kick back noise with added advantage of high speed operation which can be used in high speed analog to digital converters.

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