Static Synchronous Series Compensator (SSSC) for Series Compensation of Transmission Line using Flying Capacitor Multilevel Inverter (FCMLI)

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Abstract— This paper deals with Five-Level Flying Capacitor Multilevel Inverter (FCMLI) based Static Synchronous Series Compensator (SSSC) as used for the series compensation of transmission line. Here, voltage is injected in series with the transmission line. It is preferred to other compensating devices because apart from controlling the active and reactive power flow, it helps to damp out unwanted oscillations, such as reducing the Sub-Synchronous Resonance (SSR), Ferro-resonance and thus helps in improving the Power Quality (PQ). Hence, FCMLI is used which helps to ameliorate the output waveform and reduces the auxiliary filtering requirements. Moreover, the control logic for the inverter that has been shown in such a way that voltage stress across each capacitor connected to DC-link voltage is equal. The control logic has been implemented in MATLAB/Simulink environment and the result is shown as there are no SSR phenomena and considerable less line loss.

Keywords : Custom Power Device, Flexible AC Transmission (FACTS), Flying Capacitor Multilevel Inverter (FCMLI), Sinusoidal Pulse Width Modulation (SPWM).

I. INTRODUCTION

An usual assumption for most utilities is that the central generation utility produces sinusoidal voltage. In transmission system, voltage variation is less and may possibly be kept within the specified limit. But in distribution systems due to unbalanced loading, at large number of locations, the voltage distortions is significant. At several load points, the current waveform rarely seems to be a sine wave. This anomaly gave rise to the concept of *harmonics,* for the description of distortion in waveform leads to the deterioration of quality of electrical power with decrease in the efficiency of the system[1].

Basically the predominant reason of current harmonics is

customer non-linear loads. The current so drawn is indirectly related to the magnitude and phase of the supply voltage. Hence, non-linear loads experiences with transients or steady-state currents with frequencies other than that of the fundamental one. These harmonic currents that passing through linear and series impedance of distribution power system interacted with system impedance results in harmonic voltage distortion. Nonlinear load results with a deformed current even the source bus is completely sinusoidal. These harmonic currents along with system impedance consequences voltage drop for each harmonic component that results with biased voltages appearing at the common point of coupling/point of common coupling (PCC), must be considered as vital parameters for designing various harmonic compensators. Apart from that, earlier day's power transmission was reliable through AC as well as high voltage AC transmission system, with appreciable transmission losses. To overcome the issues of HVAC system, HVDC were introduced to carry bulk amount of power. But introducing HVDC into the system, enhances use of various power electronic devices and converters who are more responsible for injecting harmonic current onto the system. Also insertion of cables into the network may infuriate the degree of voltage waveform distortion as network impedance alters [2].

The harmonic distortion is regarded as the most vital issue at this point of time for the power system designers to rethink about the elimination of harmonics by the equipments designed to operate at fundamental frequency. Therefore, the power engineers have to deal with this unprecedented operating conditions posed by harmonics in the system. Particularly the end-user is affected by the harmonic problems more severely than the utility sector. A number of features may be used in various ways to reduce the consequences of harmonics. In general harmonics in the power system increases total system current flow whose instantaneous consequences are high losses converted to waste heat. Also it enforces an ampacity limit of consumer's end capacity to be served pointlessly restricts the current carrying capacity of the conductor which results with failure of appliances [3]. In today's world, there has been always an ever growing demand in electricity because of rapid growth in industrialization and increased standards of living of the people.

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As electricity consumption is increasing, so proper quality of power and its reliability is highly desired. For that the concept of a Flexible AC Transmission System (FACTS) came into the picture. The use of high-power electronics equipment under the concept of FACTS is a must that increases the transmission capacity, controls power flow in the transmission line and enhances the performance of the existing systems. Apart from these, it also helps in mitigating the PQ issues in present deregulated and highly competitive power industry. Basic FACTS controllers are the Static Compensator (STATCOM), the Static Var Compensator (SVC), the Unified Power Flow Controller (UPFC), the Interline Power Flow Controller (IPFC) and the Static Synchronous Series Compensator (SSSC). Therefore, the inverters should be such that its power handling capacity should be high, performance is good and is relatively inexpensive for the achievement of FACTS. But in near future it may so happen that the utilization of these inverters will be problematic because the power-electronic devices have their functional limitations. For high power applications voltage range is also large (more than 2KV) and the semiconductor devices require just a fraction of it. Hence, series connected FACTS devices are preferred as competent in supervising such voltage range [4].

Therefore it is now very much essential in removing harmonics for power quality (PQ) improvement by the use of various compensating devices e.g., SVC (implemented for reactive power compensation in power transmission lines), TCSC, TCPAR, STATCOM, SSSC, ShAPF, SAF, UPFC, UPQC, UPLC, etc., commonly known as FACTS controllers under the heading of Custom Power Devices (CPDs) [5].

Among series connected FACTS devices, SSSC consists of a converter in series with the transmission line through a coupling transformer. The SSSC using voltage source inverters has tremendous merits for transmitting power over a long distance such as: 1) improves power system stability, 2) increases the transmission lines capacity 3) controls the power flow, 4) damp out power system oscillations and Sub-Synchronous Resonance (SSR) [6]. Since, both voltage and power requirement are high, design of multilevel inverter (MLI) for SSSC should be well suited.

In general Multilevel Inverter classifications are i) Diode-Clamped Multilevel Inverter (DCMLI) ii) cascaded H-bridge inverter iii) Flying Capacitor based multilevel inverter (FCMLI). The demerit of DCMLI is that it is subjected to voltage imbalance in the DC-link. Similarly, in H-bridge inverter to lessen the harmonics enormous number of inverters is required and the voltage regulation loop is quite difficult. In addition to that, as power undulates two times of the frequency for the interchange of reactive power, this leads to requirement of over-sized link capacitors [7]. So, as far as such above-mentioned limitations are considered FCMLI is considered to be the best alternative. FCMLI along with capacitors connected in a cascaded manner aids in declining the difficulties especially during the transient conditions. Further, the control strategy in FCMLI is very simple to implement as that of a normal two-level inverter and does not depend on the voltage level across the output. This is possible as the voltage gets balanced is distributed among several switches of lower ratings. As a result, the potential gradient is equalized. With redundancy in the

switching combination, this structure makes it possible to attain enhancement in the output voltage waveform. As the desired value is almost achieved so, there is no requirement of unnecessary expenditure on filtering the output [8].

In this paper we propose the design of control logic of a five-level FCMLI-based SSSC. Principle of SSSC and its distinguished features have been explained in Section II. Further basic configuration of Flying Capacitor based MLI, its Switching Scheme, Modulation Strategy, Control Logic in MATLAB/Simulink is conferred in Section III. The results from simulation with the proposed Control Logic have been discussed in Section IV and the end note as conclusion has been conferred in Section V.
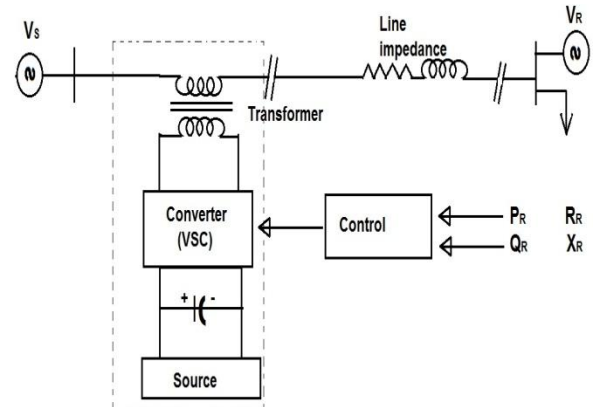
SSSC

Fig. 1. Block diagram of SSSC connected to line

The Static Synchronous Series Compensator (SSSC), one of the FACTS controller devices is associated in cascade with the line. It is a semi-conductor based voltage source inverter, comprises a voltage source converter, transformer and energy sources (optional). The block diagram of SSSC linked with the transmission line is shown in Fig 1. The control technique is applied to voltage source converter (VSC) whereas transformer that links the SSSC to the main line and the energy sources neutralizes the losses in the system. Distinguished features of SSSC over other series compensating devices are its constant compensating voltage independent of line current, supports fast control and is innately neutral to SSR [9].

The operation of SSSC either with or without an external source acts as a cascaded compensating device with output voltage independently controllable of the line current with an objective to increase or decrease the total reactive voltage drop across the line and thereby the transmitted active power is controlled [10-11].

The series capacitive compensation operates with increase in voltage across the line impedance increasing the equivalent line current along with the transmitted power. Steady-state power transmission is entrenched by series compensation as supported through a synchronous ac voltage source with output accurately bouts with the voltage of the series capacitor, i.e.,

$$V_q = V_c = -jX_cI = -jkXI \qquad (1)$$

The voltage across the line reactance would, in all practical cases, be more than, and inherently restricted to fixed compensating voltage as produced by the SSSC.

This compensating voltage is set by the control and is independent of network impedance changes, i.e., the voltage V_x across an ideal line of reactance X at a fixed δ is the function of the compensating voltage V_q only as injected by the SSSC and is expressed as:

$$V_x = IX = V_q + 2V \sin \frac{\delta}{2} \qquad (2)$$

There are generally three modes of operation of SSSC and they are Normal Mode of Operation, Inductive Mode of Operation and Capacitive Mode of Operation [12]. The SSSC employed in elementary two machine system and phasor diagram for capacitive mode of operation is given in the Fig 2.
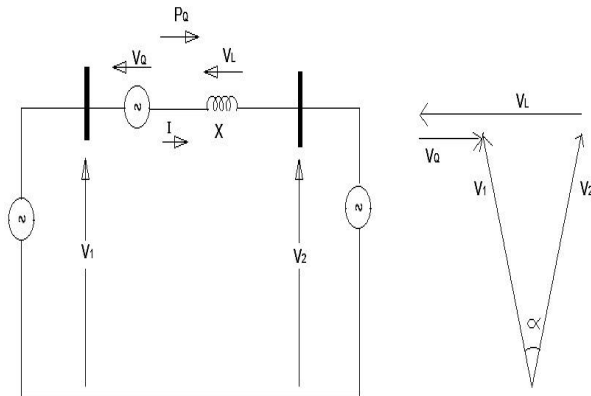

Fig. 2. The conventional two-machine system employing SSSC and related phasor diagram

Here, V_1 : Sending end voltage; V_2 : Receiving end voltage; α : Difference in phase between the two end voltages; I : Current flowing from V_1 to V_2 ; V_L : Line impedance voltage drop; P_Q : Active power and V_Q : Voltage impressed by SSSC.

The injected voltage is almost about 90° to the line current. But a fraction of the incoming voltage is in same phase with the line current that leads to notable drop in the inverter. But the remaining part of the impressed voltage is 90° with the line current, imitates inductive or capacitive reactance in series with the transmission line. The emulated reactance change, introduced through incoming voltage source accelerates the power flow through the transmission line [13].

The power governing equation expressed for a system is given by:

$$P_Q = \frac{V^2 \sin \alpha}{X} + \frac{V}{X} V_Q \cos \frac{\alpha}{2} \qquad (3)$$

The transmitted power due to SSSC either improves or declines by a fixed proportion of the peak power which is exchangeable by an un-compensated line. It is independent of α that lies in the range $0^0 \leq \alpha \leq 90^0$. Further, if this incoming voltage is greater than the voltage considered across the un-compensated line between both the ends, then the power flow will be opposite in direction.

By reducing the line reactance drop the reactive power delivered can be increased, besides there is reduction in line reactance resulting the real power handling capacity to increase, so the steady state stability limit of the line increases, keeps the entire power system under stability limit.

The voltage injected is by a capacitor bank through PWM inverter to inject harmonic free voltage.

In general Multilevel Inverters are classified as:
i) Diode Clamped Multilevel Inverter (DCMLI)
ii) Cascaded H-bridge Inverter
iii) Flying Capacitor based Multilevel Inverter (FCMLI).

The demerit of DCMLI is that it is subjected to voltage imbalance in the DC-link. Similarly, in H-bridge inverter in order to lessen the harmonics enormous number of inverters is required and the voltage regulation loop is quite difficult. In addition to that, as power undulates two times of the frequency for the interchange of reactive power, this leads to requirement of over-sized link capacitors. So, as far as such above-mentioned limitations are considered FCMLI is considered to be the best alternative. Further, the control strategy in FCMLI is very simple to implement as that of a normal two-level inverter and does not depend on the voltage level across the output. This is possible as the voltage gets balanced is distributed among several switches of lower ratings resulting equalization of potential gradient. With redundancy in the switching combination, this structure makes it possible to attain enhancement in the output voltage waveform. As the desired value is almost achieved so, there is no requirement of unnecessary expenditure on filtering the output [14-15].

II. FLYING CAPACITOR BASED MLI & RESULTS

A. Basic Configuration

The Fig 3 shows the arrangement of capacitors in a five-level flying capacitor inverter for one phase only.

Here in this figure there are 8 switches $S_1, S_2, S_3, S_4, S_{11}, S_{22}, S_{33}, S_{44}$ along with it anti-parallel diodes are connected. The switching of pair of switches occurs in a reciprocal fashion. Considering a case, if S_1 is ON, then S_{11} is OFF and contrariwise. Voltage across each capacitor is identical. Considering capacitor of the first leg near to V_{dc} among which C_1 being the main DC link capacitor is required to be controlled. So, an accumulator of suitable rating is connected as the external source. The number of capacitors in each leg goes on decreasing by 1 starting from the main leg to the innermost leg.
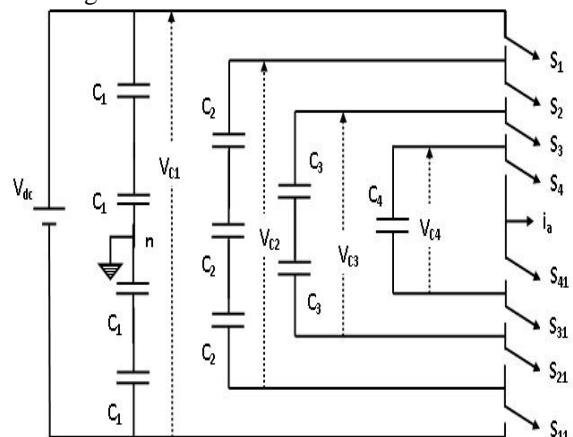

Fig. 3. Arrangement of capacitors in one phase FCMLI

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Total clamping capacitor per phase, main DC bus capacitors, voltage of the innermost capacitor are listed in the Table I.

Table I: Number of Capacitors and Voltage per phase in FCMLI

Clamping capacitor per phase	$\dfrac{(n-1)^2}{2}$
Main DC-link bus capacitors	$(n-1)$
Voltage across the innermost capacitor	$\dfrac{V_{dc}}{(n-1)}$

Voltage across the next innermost capacitor	$\dfrac{V_{dc}}{2(n-1)}$

Similarly, it follows for the other two phases with the similar construction that are coupled with the same dc-link. C_1 is the main DC-link capacitor and apart from that, the three capacitors are the flying-based capacitors which actually help in providing the desired voltage range. The flying capacitors of every phase are independent

B.Switching Scheme

The switching scheme of 1-phase leg of 5-level FCMLI has been presented in Table II

Table II: Switching scheme of 1-phase leg of 5-level FCMLI

S_1	S_2	S_3	S_4	C_2	C_3	C_4	V_{an}
1	1	1	1	UC	UC	UC	$V_{dc}/2$
1	1	1	0	UC	UC	+	$V_{dc}/4$
1	1	0	1	UC	+	−	$V_{dc}/4$
1	0	1	1	+	−	UC	$V_{dc}/4$
0	1	1	1	−	UC	UC	$V_{dc}/4$
0	0	1	1	UC	−	UC	0
0	1	0	1	−	+	−	0
0	1	1	0	−	UC	+	0
1	0	0	1	+	UC	−	0
1	0	1	0	+	−	+	0
1	1	0	0	UC	+	UC	0
1	0	0	0	+	UC	UC	$-V_{dc}/4$
0	1	0	0	−	+	UC	$-V_{dc}/4$
0	0	1	0	UC	−	+	$-V_{dc}/4$
0	0	0	1	UC	UC	−	$-V_{dc}/4$
0	0	0	0	UC	UC	UC	$-V_{dc}/2$

The expression for number of devices required 'n' level inverter is as follows:

Numbers of voltage sources $N_{dc} = (n-1)$

Numbers of switching devices $N_{sd} = 2(n-1)$

Numbers of balancing capacitors $N_{bc} = (n-1)(n-2)/2$

Numbers of DC bus capacitors $N_c = (n-1)$

The switching combination of the four switches along with three flying capacitor to get a desired waveform is such that if all the switches are ON/OFF and the capacitor value remains unchanged (UC), then output voltage is either $+\dfrac{V_{dc}}{2}$ or $-\dfrac{V_{dc}}{2}$. Similarly, if any three switches are ON/OFF, then output voltage is either $+\dfrac{V_{dc}}{4}$ or $-\dfrac{V_{dc}}{4}$. For an output voltage level $V_0 = V_{dc}$, turn on all upper half switches S_1 through S_4, whereas output voltage level $V_0 = V_{dc}/2$, turn on three upper switches S_1 through S_3 and one lower switch S_{41}.

Similarly, for an output voltage level $V_0 = 0$, turn on two upper switches S_1 & S_2 and two lower switch S_{41} & S_{31} and for output voltage level $V_0 = -\dfrac{V_{dc}}{2}$, turn on one upper switch S_1 and three lower switches S_{41} through S_{21}. For an output voltage level $V_0 = -V_{dc}$, turn on all lower half switches S_{41} through S_{11}.

It can be seen that as there is a constant repetition of output voltage, this calls for better choice of switching so that desirable output is achieved. Here, the switching pair is optimized in such a way that they do not adversely affect the capacitor. Moreover, it minimizes the capacitor cost and losses in the system.

C. Modulation Strategy

The purpose of using sinusoidal PWM for the inverters controlling the output of the series capacitors is to do away with harmonics. If the voltage is directly injected in series with the line may introduce voltage harmonics. The Fig 4 shows the modulated waveform using sinusoidal PWM and its corresponding output waveform. Here the modulation strategy considered for the inverter is based on Sinusoidal Pulse Width Modulation (SPWM).
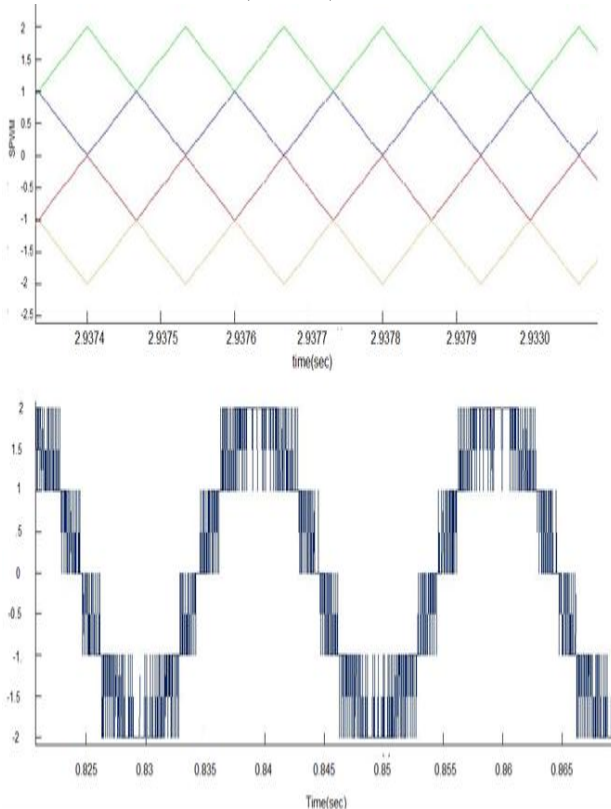

Fig. 4. Modulated Waveform: SPWM and Output Waveform

This scheme is preferred for the suppression of harmonics and reduction in switching losses. Here, the carrier signal in triangular form is compared with a sinusoidal signal and the corresponding output of modulated signal is presented in the Fig 4 where for a 5-level MLI, a modulating sinusoidal signal and four carrier triangular waves are compared for all the three phases of the inverter. Accordingly, output waveform appears in stages. Though, the magnitudes of modulating signal of three-phase are equal, but they are phase shifted by some angle. The amplitude modulation index can be varied to obtain better harmonic response. The output waveform shows 5 level voltage output justifying the control strategy of 5-level FCMLI.

The logic applied is such that when the modulating signal surpass the carrier wave the output of the comparator is positive unity otherwise zero. The outputs of these comparators are arithmetically combined to generate output voltage at the different stages.

D. Five-Level FCMLI

The SSSC is based on 5-Level Flying Capacitor MLI connected to transmission line as shown in Fig 5. It is used to control both the active and reactive power and keeps the entire power system under stability limit.

It is connected in cascaded manner to the main line and the voltage injected is such that its magnitude and phase are both manageable. Again this incoming voltage is almost in 90˚ to the current flowing in the line and hence, controls the power flow.
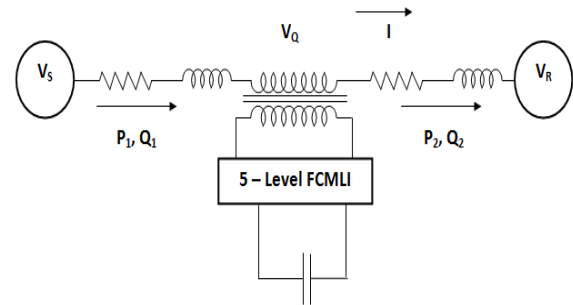

Fig. 5. FCMLI connected to transmission line

It is series associate with the main line and the voltage injected is such that its magnitude and phase are both manageable. Again this incoming voltage is almost in 90˚ to the current flowing in the line and hence, controls the power flow.

Control Logic:

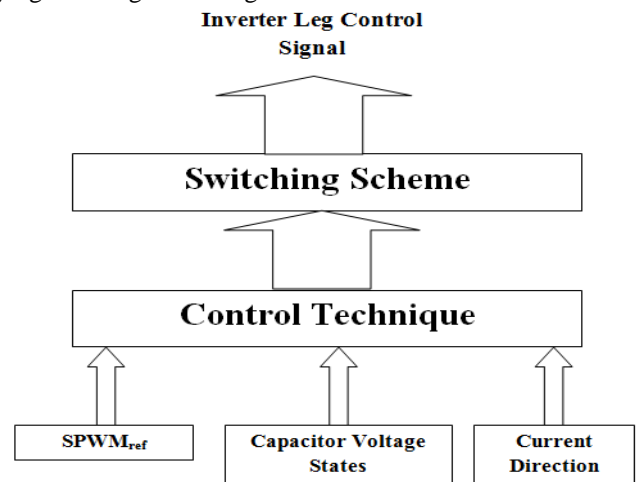The block diagram of control algorithm for the Five Level Flying MLI is given in Fig 6.

Fig. 6. Block diagram of Control Algorithm

It involves the techniques of managing the voltages of flying capacitor around its reference dc-voltage values along with the desired level of voltage at the output. In this case, dc bus voltage V_{dc} which is taken under consideration needs an external adjustment. This adjustment is done by taking into account capacitor voltage state, and a current detection block which gives the accurate positive sequence signal for generation of control signal. In addition to that, the control technique requires the additional data regarding the current orientation of the inverter and voltage status of the capacitor, which are obtained from suitable devices and networks.

The control logic of 5-level FCMLI is given in Fig. 7. With respect to the logic, the P_{ref} (reference Power) and P_{actual} (actual Power) obtained from V_{ref} and I_{ref} generates an error which is fed to PI Controller-I. Again further the signal is subtracted from $V_{d,actual}$ and fed to PI Controller –II. Its output angle β is then added with θ, and then SPWM signal is generated on comparing sinusoidal signal with triangular signal. Then the Switching Strategy is obtained which controls the 5-level FCMLI.
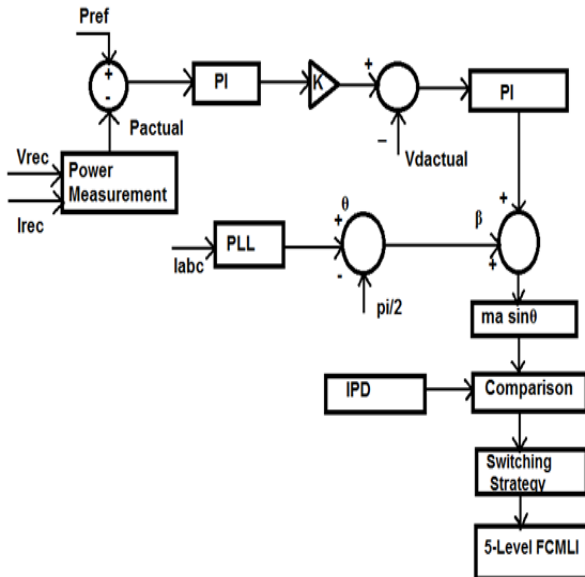

**Fig. 7. Control Logic of 5-level FCMLI**

IV. RESULTS AND DISCUSSION

A five-level FCMLI is simulated using MATLAB/Simulink environment with the system parameters as given in the Table III.

Table III: Simulation Parameters

Voltage Magnitude (L-L, rms)	154 kV
Frequency	50 Hz
Angle difference between source	30^0
Capacitance	$220\mu F$

The Fig 8 represents the simulation result of Variable DC voltage strategy.
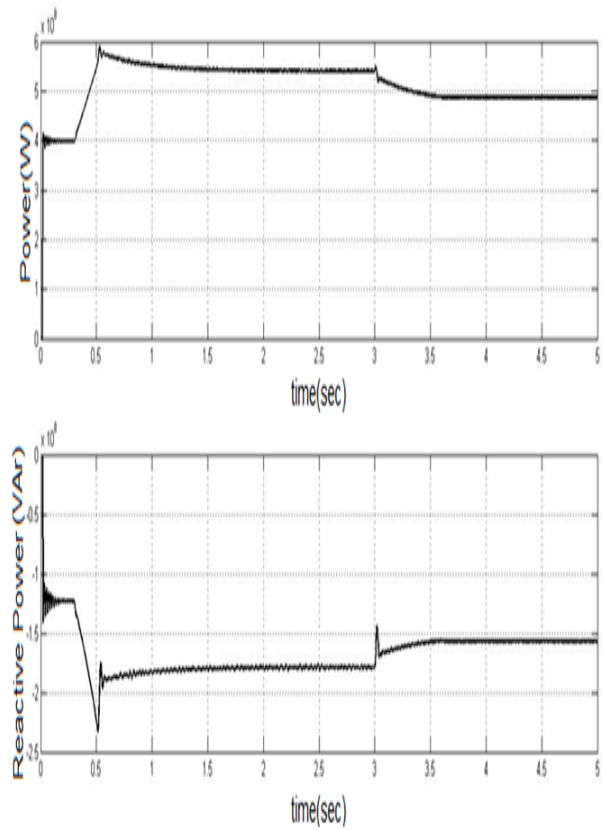
From Fig 8 it is observed that the active power is maintained nearly constant within the range of 5.4 MW whereas after 3 sec it decreases and settled to 4.8 MW. Simultaneously the reactive power has also changed. It is observed that the reactive power see a transient during a change in active power. This indicates that active power transfer can be regulated with the change in reactive power. So such control is named as coupled control.

The simulation result for compensating voltage and line current is shown in Fig 9. There is no SSR phenomenon observed as the compensating voltage is 90˚ to line current which is an inherent property of the SSSC
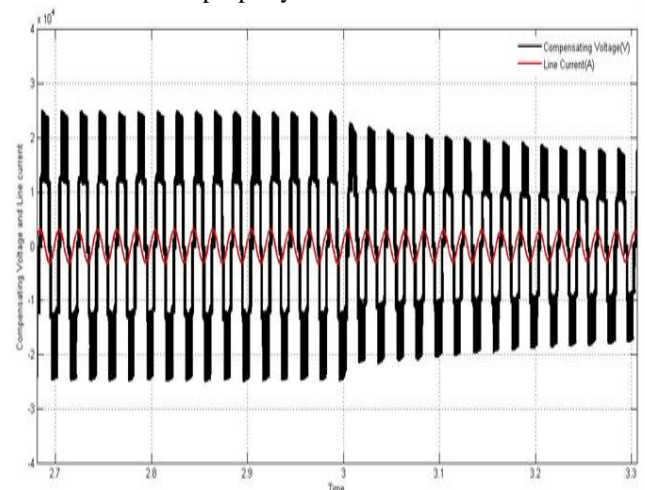

Fig. 9. Simulation result for Compensating Voltage and Line Current

The simulation result of the inverter output voltage and inverter output current is presented in Fig 10. From the Fig 10(a) it is observed that the there is a change in output voltage level after 3 sec and remain constant in the range 10 kV to -10 kV with the output inverter current between 6kA and -6kA after 6sec as shown in the Fig 10(b).
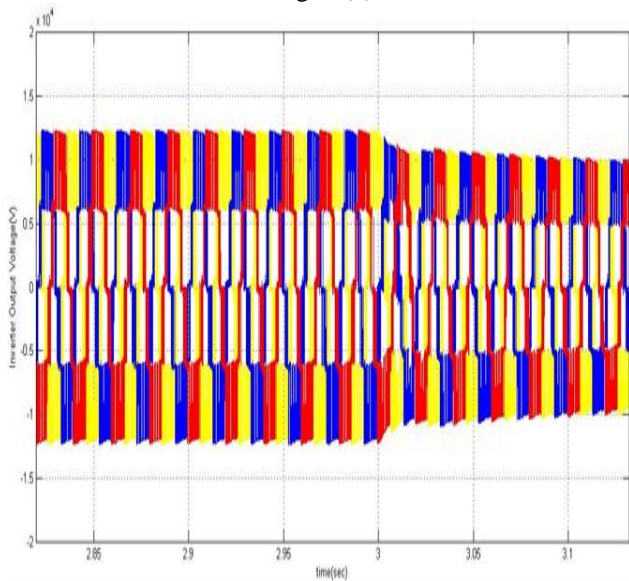
(a)
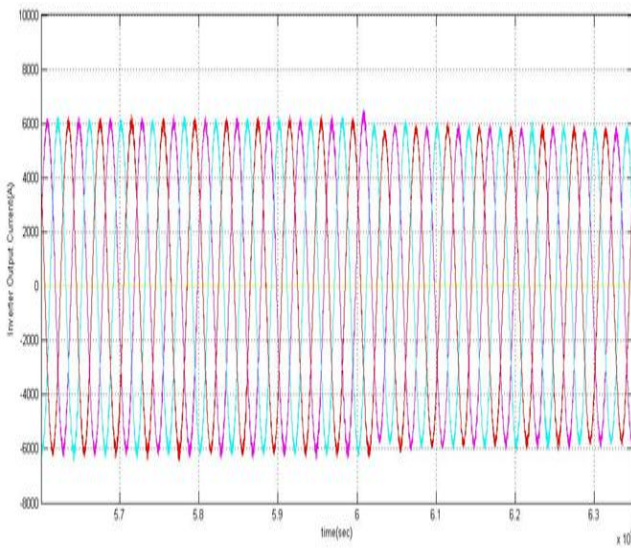
(b)

Fig. 10. Simulation Result: a) Inverter Output Voltage b) Inverter Output Current

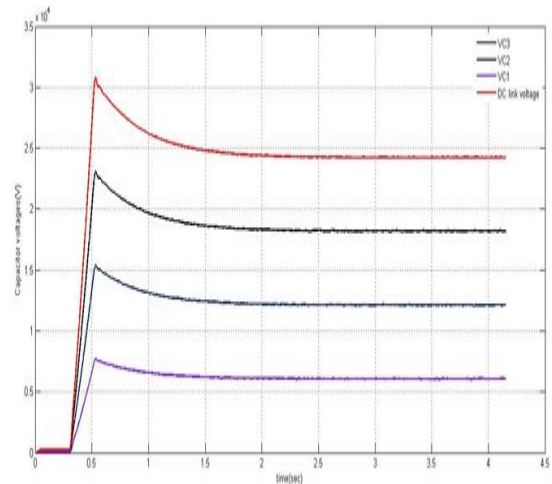Fig 11 represents the simulation result of capacitor voltage and DC link

Fig. 11. Simulation result of individual Capacitor Voltage

Here, the reference DC Voltage is taken as 30kV and it is observed that based on the reference voltage the individual capacitor voltage got balanced at starting from V_{C_1} to V_{C_3}. The same phenomenon is represented in the Fig 12, where the capacitor voltage balancing occurs even if the reference voltage changes after 3 seconds.
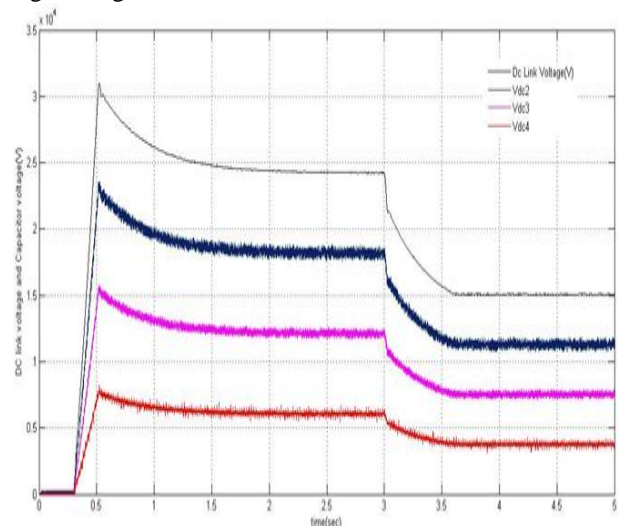

Fig. 12. Simulation result of DC link voltage and capacitor voltage

The Fig 12 shows DC-link voltage and flying capacitor voltage of all three phases. It is noticed that the control technique is capable of regulating the capacitor voltage of phase around 24kV, and DC link voltage around 24 kV during capacitive mode and 15kV during inductive mode. Further, it can be observed that the SSSC operates in capacitive mode up to 3sec and inductive mode after 3 sec. But Capacitor voltage is maintained throughout. It is to be noted here that as SSSC has to maintain DC link voltage itself, there is only one degree of freedom for SSSC. So SSSC cannot control active as well as reactive power at the same time.

The above simulation result establishes the fact that the SSSC can be implemented in the 3-phase distribution network in the micro grid system to mitigate voltage related disturbances. It has been observed that the SSSC is more capable of mitigating the voltage related issues properly. But SSSC is less reactive towards the current related issues.

The performance of SSSC is compared with results given in some previous work which is given in the Table IV below.

Table IV: Validation Table

Author	Proposed Methodology	Voltage level	Comments
Ameri et al. [2]	Cascaded h-bridge inverter	9	More switching devices, higher switching loss
Proposed Sinusoidal Current Control Strategy	Diode clamped MLI, Flying Capacitor MLI	5	Low switching losses, Better dynamic performance

V. CONCLUSION

A 5-level FCMLI based SSSC is used for series compensation of transmission line with injected voltage in series with that of transmission line. This is claimed to be better in comparison to other compensating devices as it not only controls the active and reactive power flow, but also damps unnecessary oscillations with reduction in SSR and hence improving PQ. FCMLI helps in reducing auxiliary filtering devices up to certain extent. The control strategy so adopted in this paper equalizes the potential stress across each capacitor connected to DC-link. However the effectiveness of the proposed strategy has been validated.

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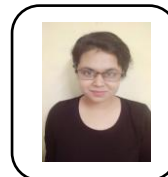
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