High Speed FIR Filter Design using Multiplier Sharing and Sub-Expression Elimination Method

Chitra M, Priyanka S, Prabha V C, Ramya S

Abstract— FIR filter is the basic filter used in many DSP applications because of its linear phase , stability , low cost and simple structure . Designing a high- speed and hardware efficient FIR filter is a very difficult task as the complexity increases with the filter order .In most Application the higher order filters are required but the memory usage of filter increases exponentially with the order of the filter using multipliers occupy a large chip area and need more access time. So the design and implementation of highly efficient look up table (LUT) based circuit for the implementation using DA Algorithm increases the speed. Multiplier sharing and sub-expression elimination methods are proposed to optimize the Structural adders. These methods split the structural adders into smaller adder blocks to reduce the delay. In order to reduce the complexity of structural adders round-off can be performed at the cost of sacrificing precision of the filter.

Keywords: FIR filter, Look Up Table(LUT),Multiplier Sharing Method(MSM) , Sub-expression Elimination Method(SEM)

I. INTRODUCTION

Designing a high- speed and hardware efficient FIR filter is a very difficult task as the complexity increases with the increase of filter order . In most applications higher order filters are required but the memory usage of filter increases exponentially with the order of the filter ,number of multipliers increased and occupies large chip area access time needed will be more . The fundamental building block in digital signal processing systems is FIR filter. Direct form or transposed direct form (TDF) can be used for implementation. Due to its inherent pipelined accumulation section a transposed direct form is mainly used. To reduce the complexity of FIR filters, a lot of effort has been put into the efficient implementation of MCM blocks and many design techniques have been proposed. Multiplier sharing

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and sub-expression elimination methods are proposed to optimize the Structural adders. These methods split the structural adders into smaller adder blocks to reduce the delay. In order to reduce the complexity of structural adders round-off can be performed at the cost of sacrificing precision of the filter. In [1] common sub expression algorithm based on tree structure is proposed to minimize the complexity of multiple constant multiplication. In [8] efficient hardware architecture for reconfigurable multiple constant multiplication block is proposed to improve area. In [11] the number of adders in multipliers is reduced by common sub expression elimination algorithm . In [13] by designing FIR filter using multiplier sharing method and carry select adder delay is reduced. The main key problem in design of VLSI circuits are larger area utilization, high power consumption and delay which affect the speed of computation and also result in power dissipation. For solving this problem, a new architecture has been proposed.

II. FIR FILTER

The filter is a frequency selective network. It passes a band of frequencies while attenuating the others. The Filters are classified into the analog filter and the digital filter depending on the nature of inputs and outputs. Digital filters are used extensively in all areas of the electronics industry. Comparing to analog filters digital filters have the ability to attain much better signal to noise ratios and at each intermediate stage the analog filter adds more noise to the signal, the digital filter performs mathematical operations also at noiseless at each intermediate step of the transform.

The digital filters were designed as a strong option for removing noise, shaping the spectrum, and minimizing Inter-Symbol Interference (ISI) in communication architectural systems. These digital filters have become popular because of their precise reproducibility and this will allow design engineers to achieve better performance levels that are difficult to obtain with the analog filters. One can construct digital from these three fundamental mathematical operations.

• Addition (or Subtraction).
• Multiplication (multiplication of the signals with the constants).
    Time delay

In order to enhance certain aspects of that signal a digital filter performs mathematical operations on a sampled or discrete time signals. Filters are of two types namely Infinite impulse response and finite impulse response .

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FIR filter is one type of stable digital filter which gives a linear phase response. FIR filter consists of Multipliers, adders and delay

elements.

The upper part of the filter shows a delay line with N+1 taps. The output of the filter is determined by Convoluting its input signal x with its impulse response h. represented as

$$Y(n) = \sum_{k=0}^{N-1} H(K) \, X(n-K) \qquad \text{-(1.1)}$$

Where

X(n) is the input signal

Y(n) is the output signal

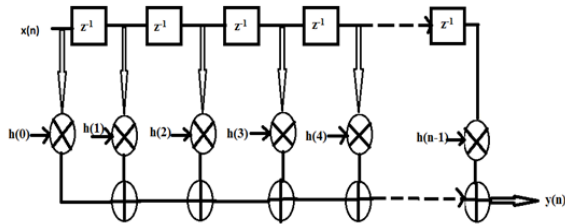H(K) the filter coefficients which are also known as taps.

Fig . 1. FIR filter structure

II EXISTING SYSTEM

In existing system the transpose form of FIR filter with ripple carry adder.
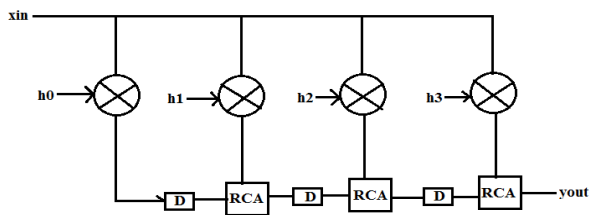

Fig . 2. Transposed form of fir filter with ripple carry adder

The fig 2 shows the transposed form of FIR filter with ripple carry adder as Structural Adders(SA).

The transposed form FIR structure is obtained by applying Transposition theorem on the Direct form. Here, same number of delay elements are used. The input signal is directly broadcast to the multipliers and multiplied with the coefficients. Hence, it is also termed as Data Broadcast structure. The delayed signal is the multiplication result hence, the number of input and output bit for the D Flips-Flops is n + m bit, where m is the coefficient word length.
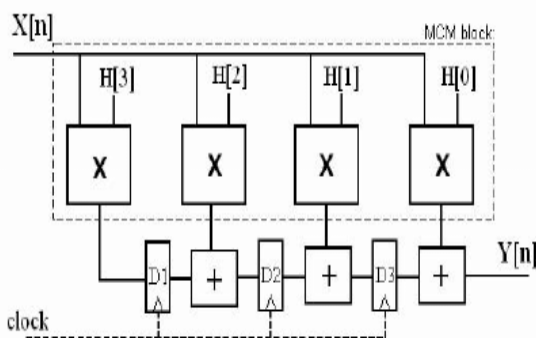

Fig . 3. Transpose form of FIR filter with MCM block and structural adders

The Fig 3 shows the transposed form of FIR filter with

MCM block , structural adders and delay .

The flexibility of transceiver design makes it possible to design reconfigurable FIR filter in digital domain and is used in Software Defined radio Technology.SDR requires separate FIR filters of different specifications in order to extract narrow-band channels from the wideband RF front end. FIR filters need to be reconfigurable in order to support multi-standard wireless communication .

To construct an N- bit parallel adder, there must be N number of full adder circuits. In a four bit ripple carry adder the carry in of the succeeding next most full adder is the carry out from the previous full adder. Inside the logic circuitry propagation delays are there. It is the time elapsed between the application of an input and occurance of the corresponding output. The time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal is he carry propagation delay.
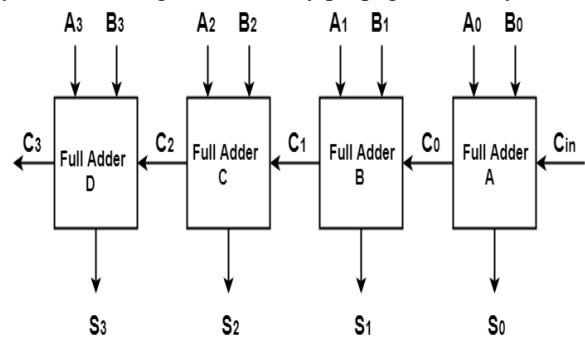

Fig . 4. Ripple Carry adder

The Fig 4 shows the two input ripple carry adder with sum and carry as output. A and B are inputs cin is the input carry, C3 is the output carry,C0,C1,C2 are the intermediate carry signals for the next stage.

III. PROPOSED SYSTEM

In the proposed system the transposed form of the FIR filter structure is modified into two structures of multiplier sharing and sub-expression method.

MULTIPLIER SHARING METHOD

Step 1 : The input signal is decided as per the need.

Step 2: In previous transposed form according to the number of taps of filter the number of coefficients are used but in multiplier sharing method the same coefficients are multiplied using same multiplier.

Step 3: The co-efficients are the designed as per the application frequency and rounded is value made to multiply with the input signal.

Step 4: The decimal value of the co-efficients are rounded by normalizing the values with the smallest and greatest values.

Step 5:The multiplied output is added using the Wallace tree adders , the adders remain same as the previous transposed method.

Step 6: The final output is obtained at the final adder as per the given input and co-efficient.
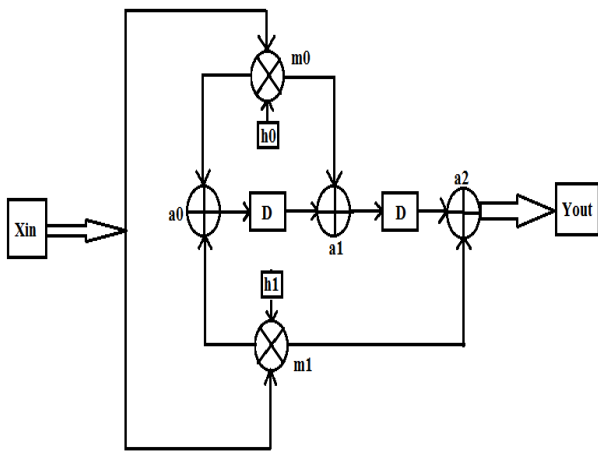
Fig. 5. Shared multiplier structure.

Fig 5 shows multipier is shared among the same coffecients to obtain the required result.

Xin is the given input value given to the filter.

h0 and h1 are the coefficient values given to the filter in which the coefficients are same as h2 and h3 in transposed form.

m0 and m1 are the multipliers which multiplies the input values with the coefficients of the flter.

a0 ,a1 and a2 are the adders in which values from the multipliers are added.

Yout is the result obtained from filter.

SUB - EXPRESSION ELIMINATION METHOD

Step1: The input values are given as per the need.

Step2: In the previous method the coefficient and input values are multiplied using the same multiplier but in this method the multiplied values are already stored in the Look Up Table and retrieved using the selection unit.

Step3: In previous step the multiplied output in obtained by retrieving, then the multiplied output is added using the adder.

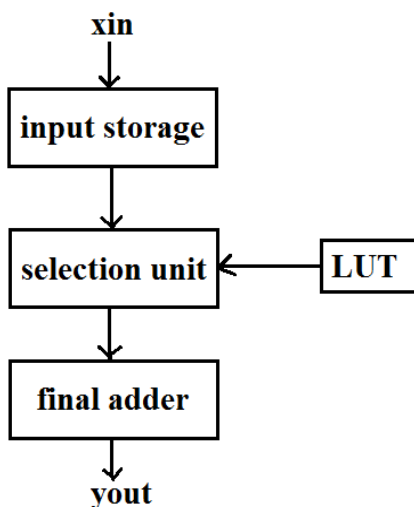**Step 4:** The output is obtained from the adder.

Fig. 6. Flow chart of sub-expression elimination method.

Fig 6 shows the steps involved on sub-expression elimination method of designing FIR filter.

IV. RESULT AND DISCUSSION

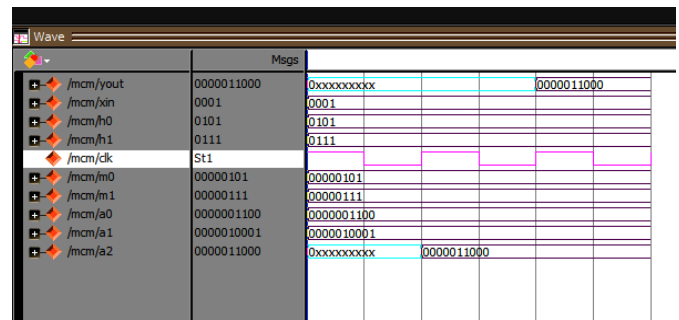*SIMULATION RESULT OF MULTIPLIER SHARING METHOD*

Fig. 7. Simulation results of the Multiplier sharing Method

Fig 7 shows the simulation result of the multiplier sharing method where,

xin is the 4-bit input signal given to the filter.

h0 is the 4-bit first coefficient of the filter.

h1 is the 4-bit second coefficient of the filter.

h2 is the 4-bit third coefficient of the filter.

m0 is the 8-bit value obtained by multiplying input and first co-efficient.

m1 is the 8-bit value obtained by multiplying input and second co-efficient.

a0 is the 8bit output obtained from the Wallace tree adder.

a1 is the 8bit output obtained from the Wallace tree adder.

a2 is the 8bit output obtained from the Wallace tree adder.

clk is the clock frequency applied to the filter.

yout is the 8-bit output obtained from the filter.
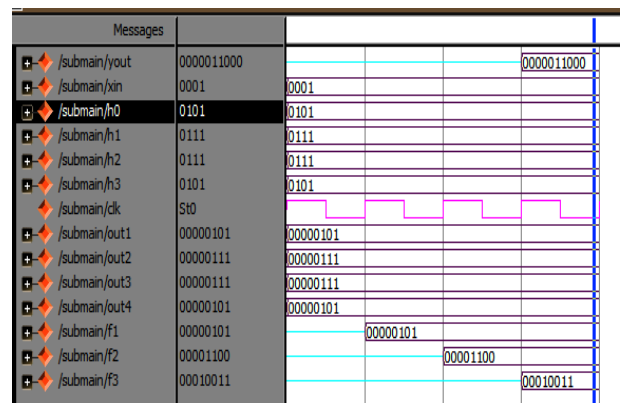
SIMULATION RESULT OF SUB-EXPRESSION ELIMINATION METHOD

Fig. 8. Simulation results of Sub Expression Elimination method

Fig 8 shows that xin is the 4-bit input signal given to the filter.

h0 is the 4-bit first coefficient of the filter.

h1 is the 4-bit second coefficient of the filter.

h2 is the 4-bit third coefficient of the filter.

h3 is the 4-bit fourth coefficient of the filter.

Out1 is the 8-bit value obtained by multiplying input and first co-efficient from LUT1.

Out2 is the 8-bit value obtained by multiplying input and second co-efficient from LUT2.

Out3 is the 8-bit value obtained by multiplying input and third co-efficient from LUT3.

Table I. Performance Analysis of Existing Method And Proposed Method

Parameter	Existing system	Proposed System	Proposed system
Method name	Tranposed form with ripple carry adder(RCA)	Multiplier sharing method	Sub-expression Elimination Method
Delay	6.140ns	5.497 ns	5.98ns
No of slices	92 out of 768	66 out of 768	179 out of 768
No of 4-input LUTs	154 out of 1536	112 out of 1536	300 out of 1536
Power	76mw	51mw	65mw

From the table I It is concluded from Table 1 there is a significant reduction in delay in FIR filter Design using Sub-Expression Elimination and there is a reduction in number of LUTs when filter is designed using Multiplier Sharing Method.
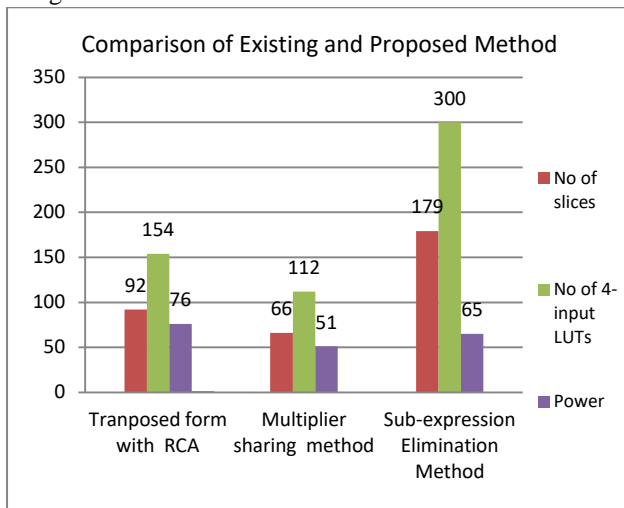

Fig. 9. Comparison of Existing and Proposed Method

Figure 9 shows the comparison of number of slices and number of four input LUT's used and power for Transposed form with Ripple carry adder and Multiplier Sharing and Sub Expression elimination methods.

V. CONCLUSION

In this project , we have designed a High speed FIR filter design by making modification in Multiple Constant Multiplication block(MCM block). All the methods are designed using verilog language and simulated using Xilinx ISE simulator. The proposed methodology which consists of shared multiplier structure and sub-expression elimination method. Modified methods are used for reduction of partial product which takes places by using efficient methods which reduce delay while increasing the area at the same time. Wallace tree adder design is used for fast addition of partial products and for final accumulation (i.e. for final addition). This proposed multiplier sharing method and sub-expression elimination method may be used in digital processing system such as digital signal processors, adaptive filters for denoising ECG signals and ALU in microprocessors .In future the number of LUT's may be reduced which in turn reduces the memory space.

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