International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-4, November 2019

Delay Minimization in on Chip Interconnects by the Method of Logical Effort

S.A.Sivasankari, B.Sakthi Kumar, R.Ohmsakthi Vel

Abstract— The ultimate aim of the work is to minimize the delay in on-chip interconnects. Our objective is to analyze the wire geometry impact for delay minimization. Here proposed effect is achieved by Logical effort(LE).The analyzes which is on the low swing where it was implemented by using CMOS circuit in 90 nm GPDK library and simulations on the cadence virtuoso ADE EDA tools. Once by reducing the delay the application is oriented for high speed applications. The logical effort (LE) model which reduces the delay minimization. This work which compensates both the long interconnects and short interconnects.

Index terms: Interconnects, Inductive effects, Wire geometry, Crosstalk, Transmission line, Logical effort.

I. INTRODUCTION

On chip inductive effects are predominant one in all DSM VLSI devices[1]. The interconnects are nothing. These are the transmission lines. The transmission lines are R, L, C components. The components present in the transmission lines where the inductance cause noises in the signals and affect the performance of the devices[1]. The inductive coupling for long interconnects are significant and shorter interconnects can be negligible. Interconnect lengths can be increased or decreased. But the clocking speeds are increased. By the trends the delay and cross talk which are very important parameters came in to picture in DSM VLSI. If the delay which happened in the circuits or RC networks because of the passive components and its parasitic.. The wire geometry impacts on this delay. Technology growing very intensively in such a way that over all coupling capacitances takes part in the device design. The signal which was passed over through one line which is aggressor. But the other line gets affected termed as victim. The noise is termed as delay noise which happened due to the victim arrival time. The techniques which used already are wire sizing, buffer sizing and buffer insertion[2]. The wire geometry is the extension technique of the wire sizing. This interconnect network can design by FPGA architecture and this architecture carriers two unidirectional programmable networks, where different optimization techniques are used in such a way that to get an optimized architecture[16],[6].

Objective here is to design the logical effort to minimize delay in the in both the gate and interconnect in the logical path. The logical effort is the combination of the logic and the CMOS and the delay optimization.

This paper comprises of the following sections. Section II which describes on the RC delay where the delay comprises of R and C values as well the voltage swing. Section III describes the Proposed work. Section IV where the schematic diagram for the LE drawn in the cadence Schematic composer is shown in figure. Section V describes the simulation by using cadence virtuoso ADE EDA tools.

II. RC DELAY

It is obtained by multiplying R and C. R is the wire resistance and C is the interconnect capacitance. Thus $\tau = RC$. The wire geometry which was taken in to account is only for RC minimization [2]. Thus any one of the element should be minimized. Thus one element should be trade off. Here by trade off capacitance for resistance. Thus for designing useful design rules to be followed. In such a way that the R should be low. But the capacitance must high ever. Delay is proportional to the square of the length. There are two different networks as lumped network and the distributed networks. Timing synchronization [3] is the biggest issue in the multiple interconnects. Since all the devices are high speed devices. Delay and length are directly proportional.

Scaling the devices to the nanometer scale leads to reduction in the gate delay. The circuit delay totally defined as the interconnect delay produced and happened due to the gate delay and global interconnect delay. The technology changing abruptly and aggressively this increases the capacitances and inductances. The voltage swing which carries the main part of the delay. Delay is the part which is directly proportional to the voltage. Based on the voltage the delay can be controllable.

III. PROPOSED WORK

Effect of the inductance on the interconnects the propagation delay can be minimized. Thus take an account of RLC devices. In the RLC models the inductance also taken part in the delay. Whenever high frequency signals are using then the inductance coupling effect must be considered as the very important issue. The cross talk problems will be increased a lot due to the line thickness increment, density of the components and the space lining reduction[4].

Manuscript published on November 30, 2019.
* Correspondence Author
S.A.Sivasankari*, Assistant Professor, Department of ECE, Koneru Lakshmaiah Education Foundation,Vaddeswaram ,A.P., India.
B.Sakthi Kumar, Assistant Professor, Department of ECE, Koneru Lakshmaiah Education Foundation,Vaddeswaram ,A.P., India.
R.Ohmsakthi Vel, Assistant Professor, Department of Mechatronics Engineering, Agni College of Technology,Chennai, Tamilnadu, India.

The general interconnects are transmission lines as RLCG for some proposals. Once the inductance comes in to picture then the mutual inductance characterizing also gets involved. Thus the delay which will happen. Based on the logic effort (LE) for fast evaluation and delay optimization in cross logic circuits [5]. Thus delay depends on the logic's fully rather than the chip wire. The logical effort is path delay will be minimum and then are fixed capacitances and hence delay will be minimum. While designing the circuits the methodologies are as follows: Logic gates without wire and with using Repeaters.[5].

Logical effort model can be rebuild by including the interconnect delay. Thus the circuit which has the delay by having the gates, inverters and CMOS devices. The output which depends on the voltage swing. The voltage swing is low then the power consumption is low. Thus the delay may increase more. The logical effort model is highly accurate and the delay minimized here is better performed. The interconnections are the predominat factor and the logical effort which achieves the minimum delay. That is performed by using the voltage swing.

The LE model which was modified by me here is with the combination of CMOS. By adjusting the voltage swing power which are adjusted in the way the delay can be reduced. While using LE have to carry out the capacitance coupling, Inductive coupling and the gate sizing also.

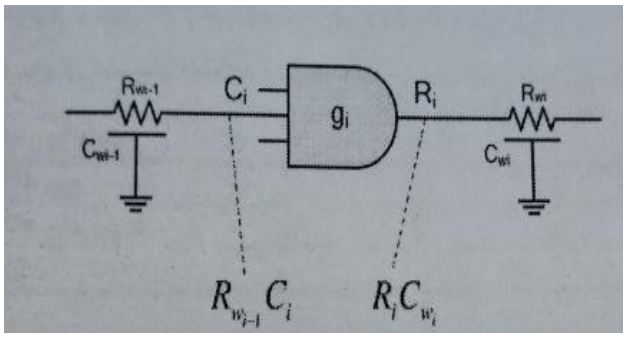

Fig. 1. Delay component for long wires[5]

Trade-off

When describe about the interconnects the trade offs are to be considered delay and power. Speed power product to be constant. The technique here which is applied to the 90nm technology.

Working principle

This method which provides the optimized timing on on-chip interconnects. Even though the scaling happened in DSM VLSI.But not at all in wires. Thus reducing the delay the LE path which reduces the delay in such a way that the long interconnects are broken down in to shorter sections. The fan out issue which are avoided by using the CMOS circuit and this behavior shows the delay reduction. There are the uniform sizes of all the devices and the delay component which is an effect of gate capacitance which is same as the ressistance of the gate. The accuracy which is increased here when compared with other models. Optimization can done by using the repeater insertion also.

This LE model which shows the better performance when compared with elmore delay model. Here the low swing reduces the delay. In such a way paved for high speed applications.

IV. SCHEMATIC DIAGRAM

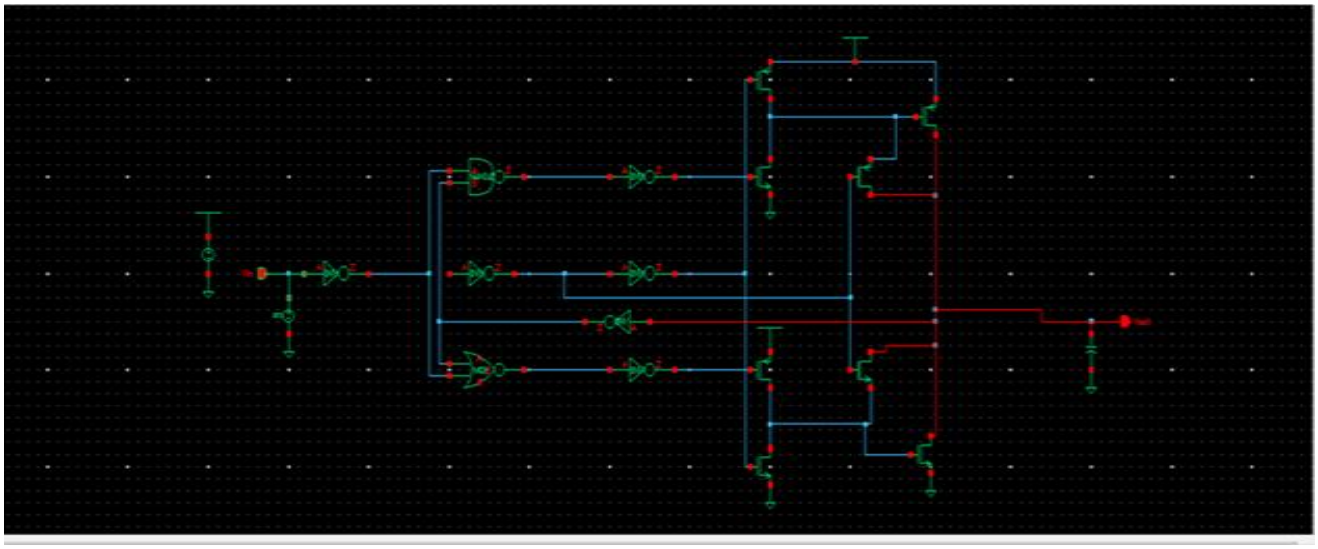

Fig.2 Schematic diagram

V. RESULTS AND DISCUSSIONS

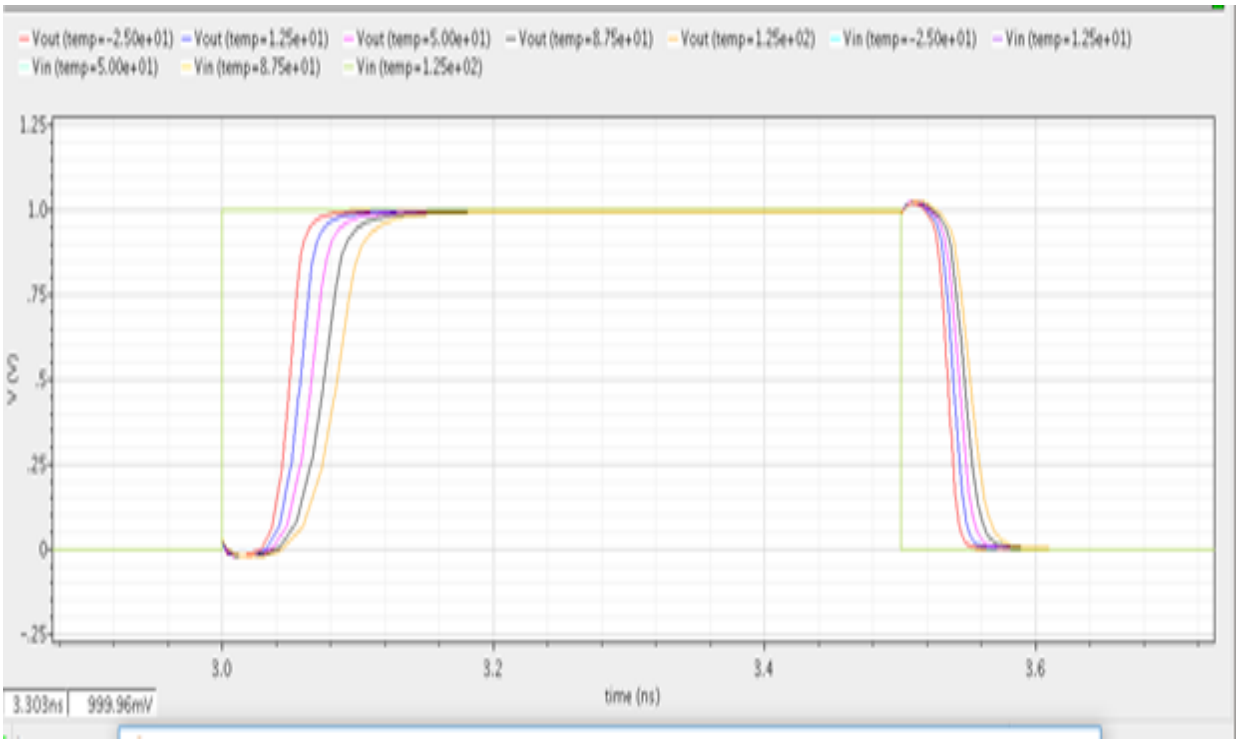

Fig. 3. Over all delay effect on LE

LOW SWING OUTPUT 1

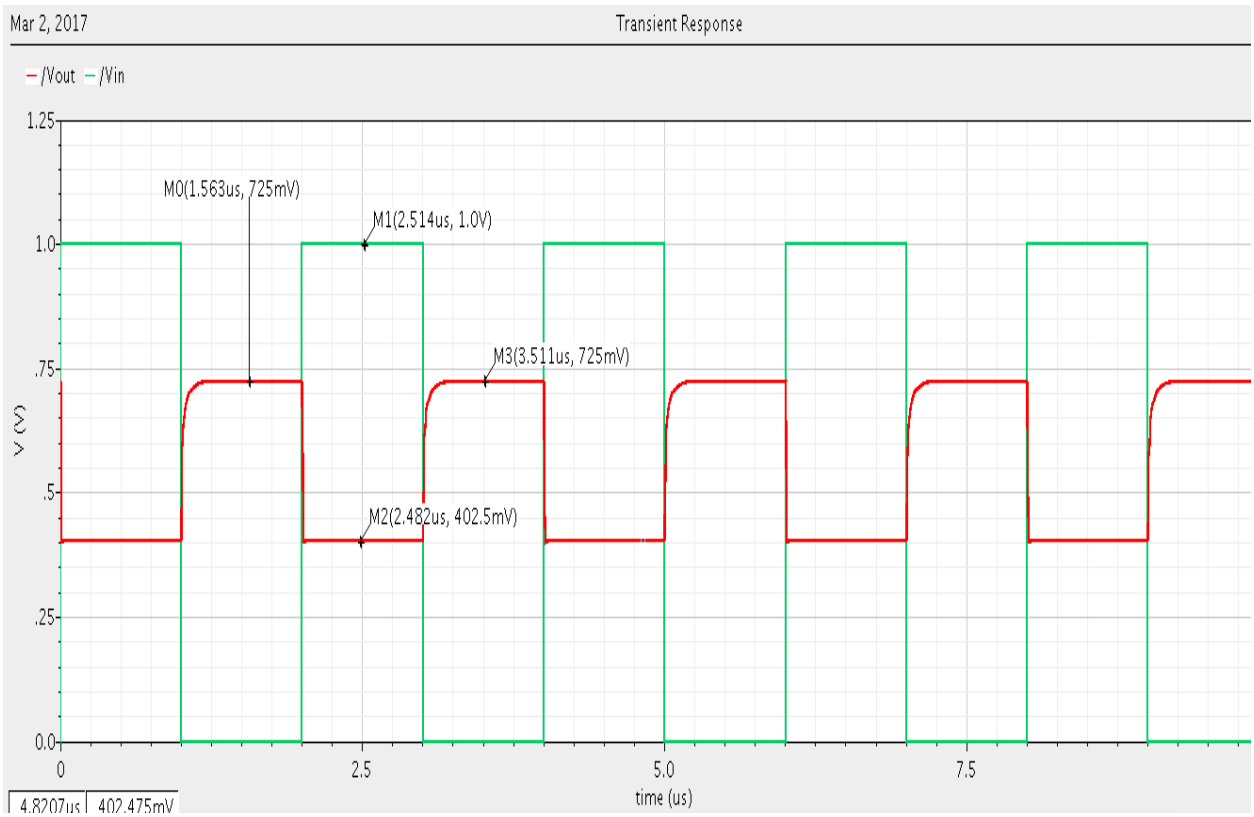

Fig 4 delay on low swing 0.75

LOW SWING OUTPUT 2

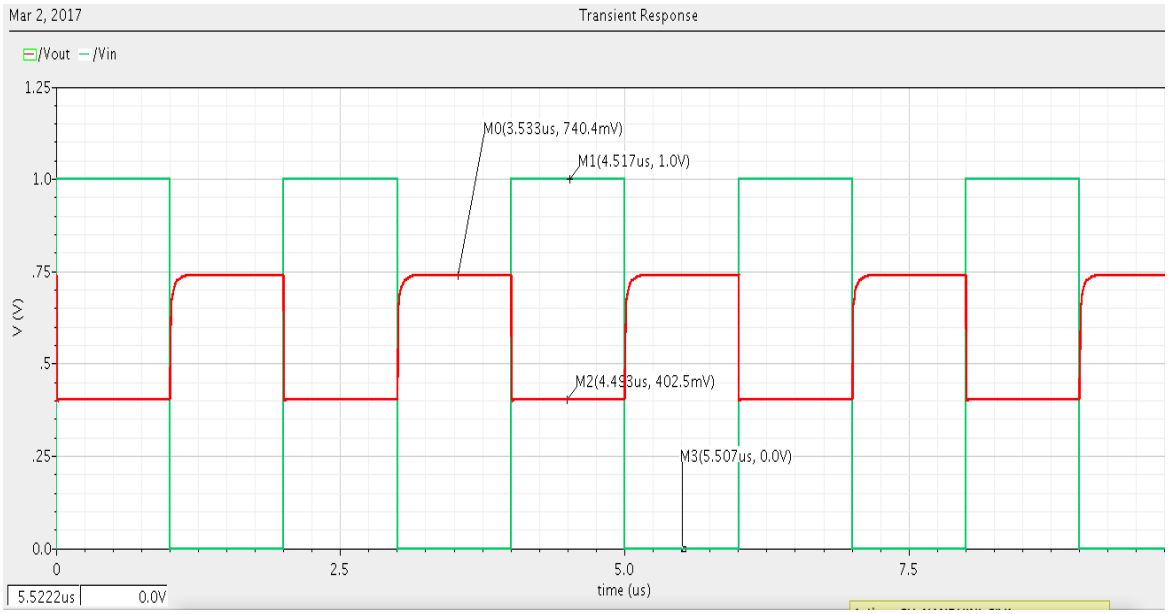

Fig 5 delay on low swing 1 V

LOW SWING OUTPUT 3

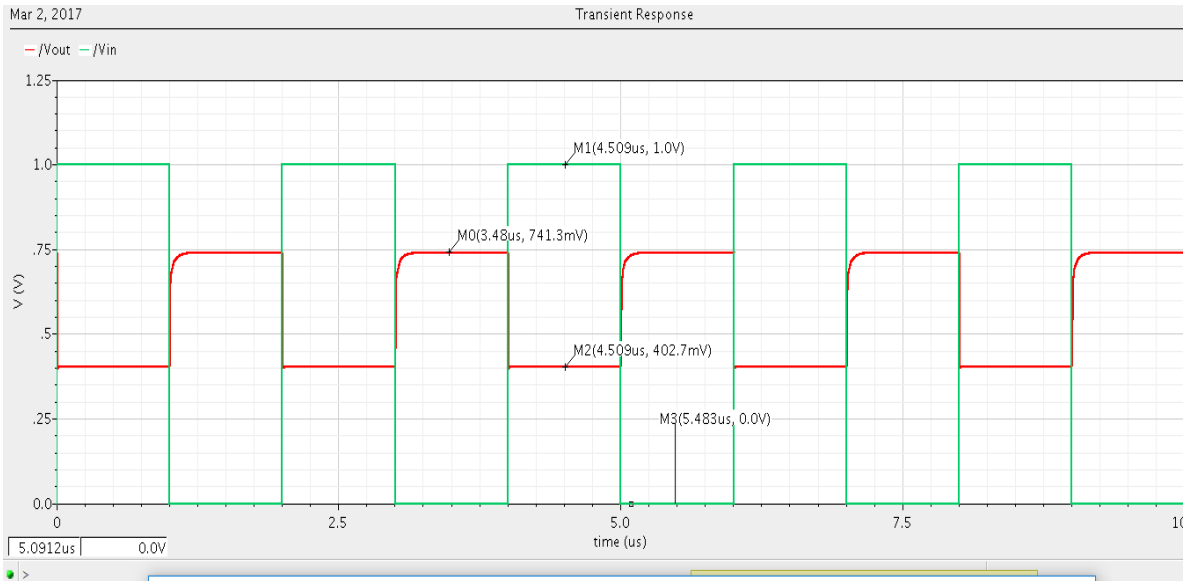

Fig 4 delay on low swing 1.5 V

Table .1. Delay with respect to swing

swing	Rise time(ns)	Fall time(ns)	Delay(ns)
0.75	0.951	1.028	0.9895
1	0.984	1.014	0.999
1.5	1.029	0.974	1.0015

VI. CONCLUSION

The RC delay model which was available here as the equivalent circuits of MOS transistors. The CMOS which is there in the schematic diagram is designed in such a way that it acts as ideal switch and capacitance as well the ON resistance can take an account. The unit for NMOS has resistance R and capacitance C .But the unit for PMOS has resistance of 2R resistance and C capacitance. Capacitance which is proportional to the width of the wire and the resistance which is inversely proportional to the width of the wire. The low output swing minimizes the power consumption. Wires also have the capacitance per unit length to the neighbours and to the layers above and below too. Thus the total capacitance is addition of top capacitance, bottom capacitance and Adjacent 2C.Interconnect delay model in 90nm on-Chip IC has been implemented. Simulation results were plotted for different transistor width. Simulation results shows that the output swing can be changed by changing the width of the transistor.

REFERENCES

1 Ravindra,Pandurangaiah Yagateela, Narasimha Prasad,"A Novel analytical model for analysis of delay and cross talk in Non linear RLC interconnects for ultra Low power Applications," UKSim 15th international conference on computer modelling and simulation,2013.

2 S.A.Sivasankari,Dr.D.Dhanasekaran,"Transmission line effects and cross talk effets on interconnects in deep submicron VLSI ,"International Journal of Pure and Applied Mathematics, Volume 119 No. 14 2018, 181-185.

3 Guang-Hwa shiue, Member, IEEE, Jia-Hung Shiu, Yi-Chin, and Che-Ming Hsu," Analysis of common mode noise for weakly coupled differential serpentine delay microstrip line in high speed digital circuits", IEEE transactions on Electromagnetis compatibility,Vol 54, No.3, June 2012.
4 Narendra Babu T., Noorbasha F., Krishna S., Sai Charan K., Sai Kalyan R.S.V.S., FPGA implementation of cryptographic system using BODMAS sequence of operations ,2016, ARPN Journal of Engineering and Applied Sciences, Vol: 11, Issue: 19, pp: 11475 - 11479, ISSN 18196608.
5 Arkadiy Morgenshtein, Eby G.Friedman,IEEE,Ran Ginosar,Senior Member, IEEE, and Avinoam Kolodny,Member,IEEE,"Unified logical effort- A method for delay evaluation and minimization in logic paths with RC interconnect,"IEEE transactions on very large integration (VLSI) systems, VOL, 18 ,NO.5, May 2010.
6 *zied marrakchi,hayder mrabet,umer farooqand habib mehrez, ,"FPGA Interconnect Topologies Exploration,"International journal of reconfigurable computinh, vol 2009*
7 International Technology Roadmap for Semiconductors. [Online]. Available: http://public.itrs.net
8 K. Schuegraf, M. C. Abraham, A. Brand, M. Naik, and R. Thakur, "Semiconductor logic technology innovation to achieve sub-10 nm manufacturing," IEEE J. Electron Devices Soc., vol. 1, no. 3, pp. 66–75, Mar. 2013.
9 P. J. Roussel et al., "Semi-empirical interconnect resistance model for advanced technology nodes," in Proc. Int. Rel. Phys. Symp., 2016.
10 A. Matthiessen and C. Vogt, "The electrical resistivity of alloys," Ann. Phys. Chem. (Pogg. Folge), vol. 122, pp. 19–31, 1864.
11 C. Arenas, R. Henriquez, L. Moraga, E. Muñoz, and R. C. Munoz, "The effect of electron scattering from disordered grain boundaries on the resistivity of metallic nanostructures," Appl. Surf. Sci., vol. 329, pp. 184–196, Feb. 2015.
12 H. Li, S. Jin, J. Proost, M. Van Hove, L. Froyen, and K. Maex, "A new approach for the measurement of resistivity and cross-sectional area of a aluminium interconnect line: Principle and applications," in Proc. ULSI 13th Mater. Res. Soc., 1998, pp. 197–203.
13 Raphael User Manual. [Online]. Available: http://www.synopsys.com/TOOLS/TCAD
14 P. Cocchini, G. Piccinini, and M. Zamboni, "A comprehensive submicrometer MOST delay model and its application to CMOS buffers," IEEE J. Solid-State Circuits, vol. 32, no. 8, pp. 1254–1262, Aug. 1997.
15 S. C. Song et al., "Holistic technology optimization and key enablers for 7 nm mobile SoC," in IEEE Symp. VLSI Technol. Dig., Jun. 2015, pp. T198–T199.
16 Murali Krishna B., Rakesh Chowdary G., Chandra Vardhan G., Siva Ram K., Sai Kishore P., Madhumati G.L., Khan H., FPGA based wireless electronic security system with sensor interface through GSM ,2016, Journal of Theoretical and Applied Information Technology, Vol: 89, Issue: 2, pp: 489 - 494, ISSN 19928645.