International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-4, November 2019

Implementation of Staggered Pulse Repetition Frequency RADAR Tracking with Xilinx FPGA

P.A.Harsha Vardhini, P.Upender

Abstract—This paper implements a Pulse Repetition Interval tracker against Staggered PRI Radar. Tracking of Staggered PRI is done using the IAR Embedded Workbench on STR710 microcontroller. Staggered Pulse Repetition Frequency is generated using Pseudorandom Number Generator using Linear Feed Back Shift Register in VHDL and implemented in Spartan-3E.

I. INTRODUCTION

Radar and communications are pivotal components in any modern air defense system. There has been a substantial progress in India's ability to design and manufacture high power radar systems of its own design and with locally manufactured components and system. During the past 30 years, radar systems design has considerably improved. Radars manufactured today are more complex versatile, sensitive, accurate, both powerful, and provide more data processing aids to the operator at the display console. Radars manufactured today are having low probability intercept (LPI) features, which include less transmitted power, frequency agility, low side lobe levels etc.,

Radars will have complex pulse pattern. Electronic use passive spectrum to gain intelligence about other parties on the battle field in order to find, identify, locate and intercept potential threats. Modern Radars use PRF agility to avoid blind speed and to avoid synchronous jamming, Pulse Repetitive Interval (PRI) is varied randomly among the successive signal transmissions. This is called staggered PRI. In multi threat environment it is necessary to predict the expected arrival the radar pulse in order to effectively allocate the jammer resources for handling such threats. For countering such staggered PRI Radars, the EA system must have the capability to track the PRI of victim Radar. This is accomplished by measuring the successive PRIs of received radar signal for the entire pattern and predict the next PRI that has to be generated by EA system.

This work highlights the tracking of Staggered Pulse Repetition Frequency (PRF) radar. The programming code is developed using both C and VHDL. This work uses both hardware and software development tools of Xilinx. ISE is used for generating staggered PRI. Tracking is implemented in C using IAR Embedded Workbench. Fig. 1 shows the entire procedure carried out in this paper

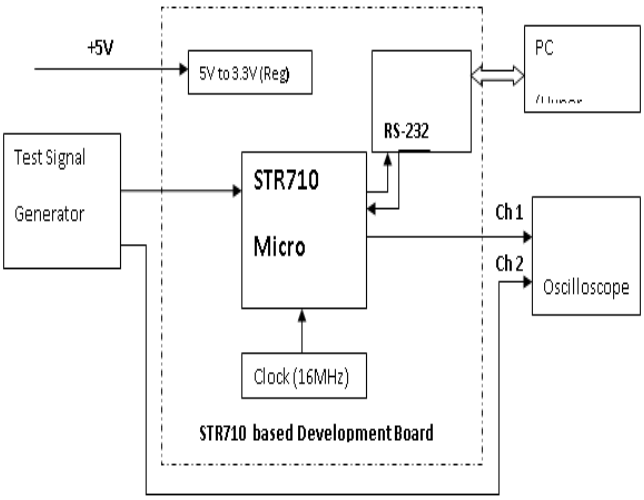

Fig 1. PRI Tracker Implementation using FPGA and ARM controller

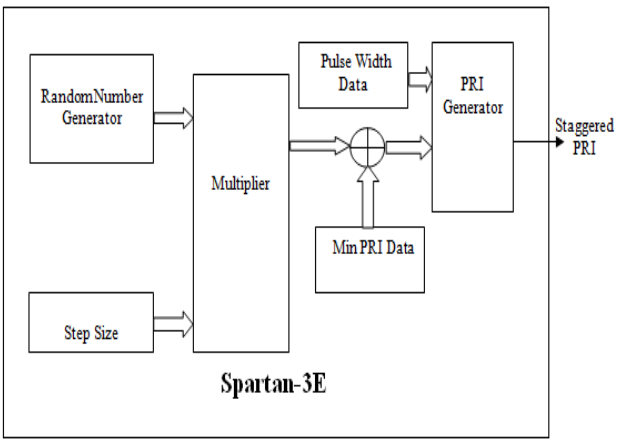

Fig 2. Generation of Staggered PRI with Spartan3E FPGA

II. GENERATION OF STAGGERED PRI AND HARDWARE IMPLEMENTATION

The test signal Staggered PRI can be generated using Spartan-3E FPGA. Fig. 2 is the block diagram for the generation of Staggered PRI. Step size should be selected according to the level of the staggering. Random number is generated using LFSR (Linear Feedback Shift Register) with the help of random number generator as per the required number of staggering levels.

Manuscript published on November 30, 2019.
* Correspondence Author
P.A.HarshaVardhini*, Department of ECE, Vignan Institute of Technology and Science, Deshmukhi, Telangana, India.
P.Upender, Department of ECE, Vignan Institute of Technology and Science, Deshmukhi, Telangana, India.

Step size and random number are multiplied using multiplier. The output of the multiplier is added to the minimum PRI data to get the Pulse period of
individual pulse in the Staggering PRI. Pulse period and Pulse width are used to generate Pulse using PRI generator. As this process continues PRI generator will generate pulses of different periods. Hence the output of the Spartan-3E kit will be staggering Pulse Repetition Interval (PRI).

A. STR710 Microcontroller

The STR710 series is a family of ARM-powered 32-bit microcontrollers with embedded Flash and RAM.

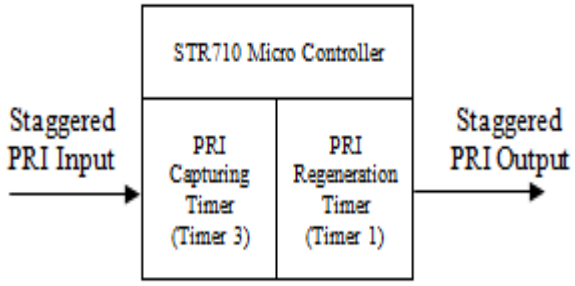

Fig 3. Block Diagram of STR710 Microcontroller for Capturing & Regeneration of Staggered PRI

The microcontroller contains the PLL which is used to increase the processor core operating frequency to 48 MHz for tracking PRI first PRI has to be measured. The input signal is applied to ICAPA (Input capture A) signal. The Timer will be configured as PWMI mode which measures the Pulse width and PRI of the signal. Timer starts counting the clock pulses with the Rising edge of input signal. Two counters are used to capture the Pulse width and PRI value.

Every time the input signal edge appears at ICAPA pin an interrupt is generated which will be used to store the PRI and PW data in an array. Data structures are used to hold the PRI and Pulse width data.

Another timer is used to Generate the tracking PRI. This Timer is used in PWM generation mode. The input parameters for this mode are PW and PRI data which is retrieved from the measured parameters. The clock for the timer counters is 48MHz so that the Measurement resolution is 20ns approximately. The PWM generation is synchronized with the incoming PRI patterns at regular intervals to retain the synchronization. Sync will be lost due to the difference in the stability of the clocks for generating input signal and the signal generated by the Microcontroller. The PRI patterns are observed with an oscilloscope to validate the synchronization process. In the absence of the input signal the Microcontroller has to continue generating the PRI pattern. Once again when the input signal is present it should remain in Sync with input.

III. IMPLEMENTATION AND RESULTS

A. Staggered PRI Implementation in Spartan-3E using ISE

FPGA receives the input from the select lines. The FPGA pins are assigned to the input and output of the Top Level Entity based on the interface details given in the Spartan-3E kit. Since the FPGA pins are already connected to the accessory pins we have to assign corresponding signals to the FPGA pins in the User Constraints File (UCF). Once this is done the design can be implemented in the FPGA.

The output of the implementation procedure is the .bit file which will be used to configure the FPGA through USB interface using iMPACT application provided by the Xilinx as a part of Generating Programming File as in fig. 4.

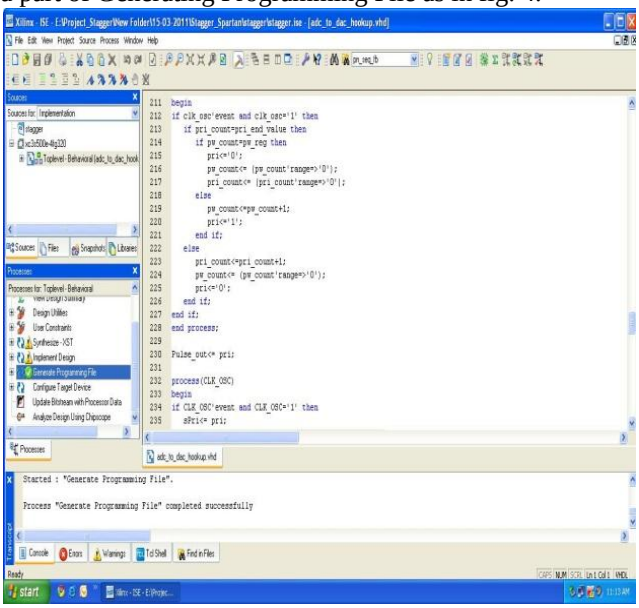

Fig 4. Window showing Generated Programming File

After assigning the bit files and programming the device, the ISE generates a program succeed dialog in the same window which is shown in fig. 5 as follows.

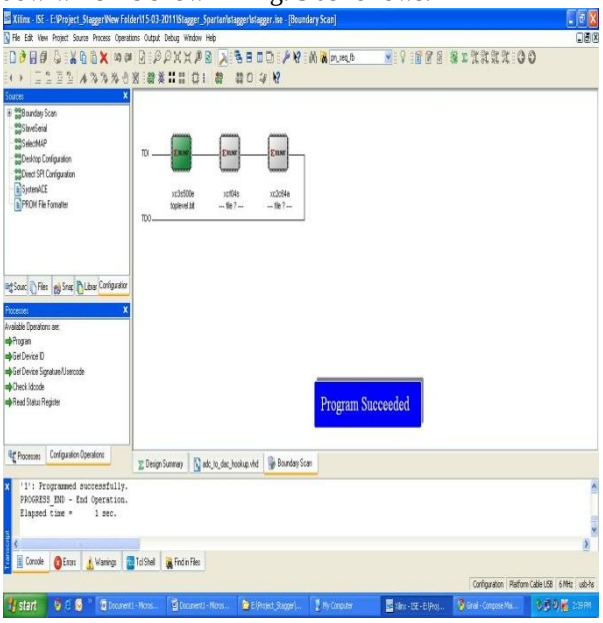

Fig. 5. Window showing succeed dialog

Once the FPGA is programmed different leveled Staggered PRI can be generated by selecting different Slide Switches.

B. Programming the Microcontroller

Once required connections are made, the .bin file generated after compiling the project in IAR embedded workbench is programmed in to the micro controller STR710 as in fig. 6.

Fig 6. Programming of STR710

Below fig. 7 is the dialog box showing the programming of the micro controller being successful.

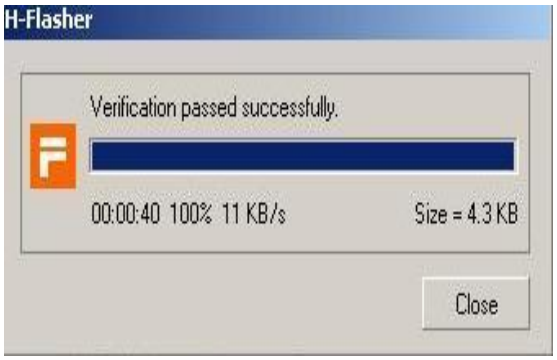

Fig 7. Dialog box

C. Output results

After configuration and programming of the FPGA, the output pin of the Spartan-3E FPGA is connected to the digital storage oscilloscope to observe the waveforms. The output of the pulse generator which can controlled using select pin of Spartan-3E, can be configured to generate a square with pulse width 5microseconds and period varying between 150microseconds and 250microseconds. Once all the appropriate connections are made for output from the Spartan-3E to the input capture pin of the ARM micro controller. The staggered PRI is captured using the Timers of the STR710. The micro controller checks for appropriate conditions, if they are met, it starts the regeneration of the captured Staggered PRI configuring one of the timer in output compare mode. The output from the output compare pin of the ARM microcontroller is given to the digital storage oscilloscope. The tracked waveform can be seen on the digital storage oscilloscope in synchronization with the input waveform.

D. Tracking 8, 16, 64 level Staggered PRI:

When the input to the Arm Microcontroller is 8 level staggered PRI. The output is 8 level staggered PRI as in fig. 8

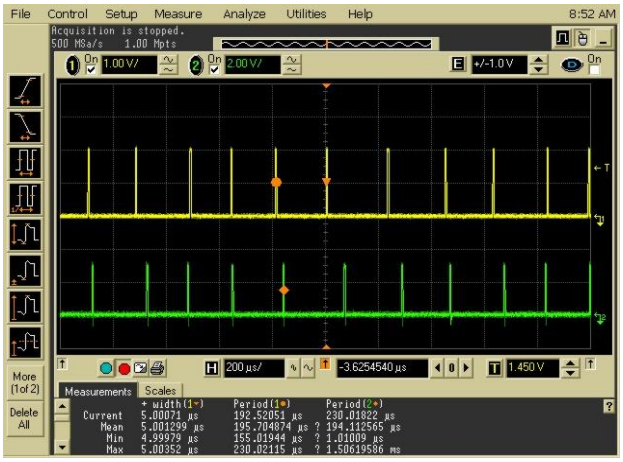

Fig 8. PRI Tracker output for 8 level staggered PRI input

When the input to the Arm Microcontroller is 16 level staggered. The output is 16 level staggered PRI is as in fig. 9.

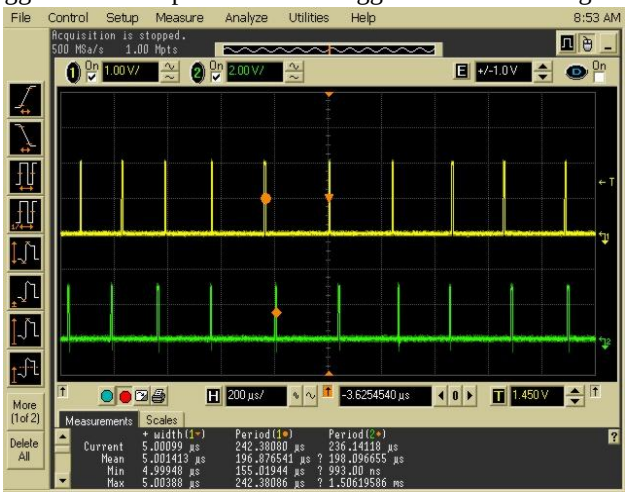

Fig 9. PRI Tracker output for 16 level staggered PRI input

When the input to the arm microcontroller is 64 level staggered PRI. The output is 64 level staggered PRI as in fig. 10.

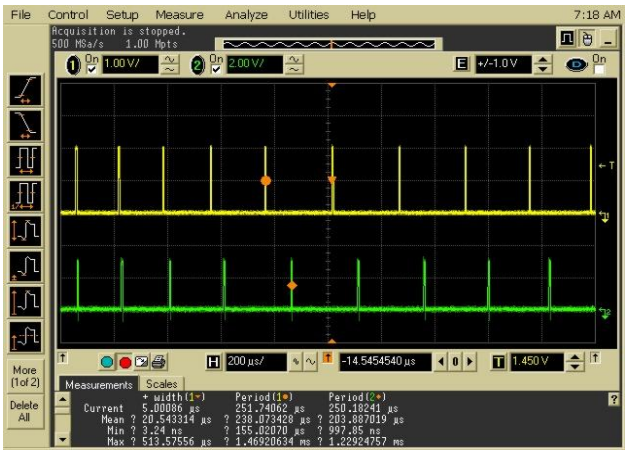

Fig 10. PRI Tracker output for 64 level staggered PRI input

IV. CONCLUSION

PRI Tracker against Staggered PRF using ARM micro controller and Spartan 3E FPGA for tracking multi level staggered Radar signal has been implemented. Design is verified by generating staggered PRI test pattern using Spartan Evaluation Board and results are observed on digital oscilloscope. PRI Tracker algorithm can be extended to multi channel PRI Tracker by using number of additional timers which will enable effective time sharing of Jammer resources under multi threat environment.

REFERENCES

1. J. Appl.Meteor, B.R. and E.J. Dutton., "Optimizing the Radar Detection of Clear Air Turbulance", Vol.5 Pg Nos. 450-460, 1996
2. J. Bhasker., "A VHDL Primer", Pearson Education third Edition, 2005.
3. John F. Wakerly., "Digital Design Principles and Practices", Pearson Education third Edition updated, 2006.
4. Haiqing Jiang, MeiguoGao, Yunjie Li, "Design and Implementation of the Pulse Tracker Based on FPGA", IEEE 2006.
5. RémiGauvin, Dr Ken McRitchie and Scott E. McDonald, "Enabling Technology: Radar PRI and RF Prediction", MC Countermeasures Inc. October, 2005.
6. P.A.HarshaVardhini, M.MadhaviLatha, C.V. Krishna Reddy, "Optimum Decimation and Filtering for Reconfigurable Sigma Delta ADC", Fareast journal of Electronics and communication, pp.101-111, Vol. 11, No.2, Feb 2014.
7. P.A. HarshaVardhini, "Design and Implementation of Adaptive filter on Xilinx FPGA", Journal of Applied Science and Computations. (J-ASC), pp.36-39, Vol.4, Issue 2. July 2017.
8. BinduTushara D., HarshaVardhini P.A. (2017) Performance of Efficient Image Transmission Using Zigbee/I2C/Beagle Board Through FPGA. In: Saini H., Sayal R., Rawat S. (eds) Innovations in Computer Science and Engineering. Lecture Notes in Networks and Systems, vol 8. Springer, Singapore.

AUTHORS PROFILE

Dr. P.A.Harsha Vardhini, professor in the Department of Electronics and Communication, Vignan Institute of Technology and Science, Deshmukhi has 18 years of teaching experience. She pursued her Ph.D in VLSI Design from the department of ECE, JNTUH. Her research interests include Low Power Mixed Signal VLSI Design, FPGA architectures, IoT Embedded Applications & Wireless Communication. She is an IEEE & WIE member and life member of IEI, ISOI, IAENG, IAOE. She has more than 90 publications in various journals and conferences at national and International level including SCI, SCOPUS, IEEE, Springer, Elsevier and UGC.

P.Upender received B.Tech degree from JNTU, Hyderabad, M.Tech degree in RF & Microwave from IIT ROORKEE and pursuing Ph.D. He is currently an Assistant Professor in the department of Electronics and Communication Engineering at Vignan institute of technology and sciences, deshumuki. His research interests are microwave engineering, Antennas, Radar Engineering, RF communication.