Energy Efficient Bandgap Reference Generator for RFID Transponder EEPROM in 130 nm CMOS Process

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Abstract: ***Reducing power dissipation of any circuit can make that circuit more energy-efficient and at the same time promise stability. Recent researchers mainly focus on controlling and monitoring low power designs for different low power applications, wireless systems such as radio frequency identification (RFID) transponder. Therefore, generating an internal reference voltage (VR) for the power management unit is the key challenges for researchers to design such applications. Bandgap reference (BGR) is an essential module that assures temperature and independent VR supply in analog circuits. In this research, an improved BGR is designed with the self-startup circuit, bandgap core and an operational amplifier (OP-AMP) to generate a stable VR. A low-power BGR is simulated using Silterra 130 nm CMOS technology. The designed BGR generates a VR of 1.1 V and consumes only 1.4 µA power form 1.2 V power supply voltage. Moreover, it has a temperature coefficient of 41.6 ppm/℃***

Keywords: CMOS, OP-AMP, RFID, Transponder

I. INTRODUCTION

Currently, microelectronic systems are facing various design challenges, which involves reducing power dissipation, reduced chip area and reliability for the long term. Low power applications such as RFID, smart and wireless sensors meet the above-mentioned design aspects [1-2]. In addition, these systems need powerful batteries that have a long lifetime, fabricated from toxic/hazardous chemicals and slow processing speed, which is eventually failed to meet the challenges. Therefore, recent research on integrated circuits (IC) is concentrating on energy proficient structures, which can control power management, decrease the battery-dumping rate, and escalate the system dependability. Analog circuits such as analog-to-digital converter (ADC), a digital-to-analog converter (DAC), switching voltage regulators, frequency converters, internal high voltage generator (HVG) circuit, power converter circuits, RFID transponder's power management unit etc. required an accurate VR generator or a bias current that is temperature and supply variation independent. Typically, an ideal reference voltage generator should be well defined and output voltage should have temperature independence [3-5]. Moreover, there should have other variations like power supply, load and other operating conditions. As mentioned above, a voltage reference, as its name implies, is a circuit that generates an exact output voltage. In theory, the output of a voltage reference (VR) does not depend on the process, the operating voltage, temperature, load current or the passage of time [6].

According to performances, a reference voltage generator is divided into three categories namely; zero order, first order and second order references or higher-order references [7]. However, among these three types, zero-order references are considered as the basic one, which is mainly suffered from high-temperature variation from 1.5 mv/°c to 5 mv/°c. In addition, this type performs poorly compared to other types. On the other hand, the first-order reference is known as "the first-order term of the polynomial relationship with respect to temperature is effectively canceled" [7], which is better than zero-order in terms of temperature variation only from 50 to 100 ppm/°c. However, these types of vr generators are not compatible with high-performance adcs, sensors, or applications with internal power supply systems. Therefore, second-order reference voltage generators are highly in demand for acquiring high precision data with lower temperature variation of less than 50 ppm/°c [8].

Most of the researchers use bgr for vr circuit in low power applications as the vr does not depend on the temperature, process and supply voltages [9]. Like another circuit, this ic is also made from registers, mosfets and transistors. Gamma irradiation assessment was taken into consideration during the design process that results in less than 3% of variations. Moreover, sub-1 v operations compatibility is shown. However, some trials showed a sluggishly incremental slope even decreasing slope in the output reference voltage due to the mismatch in the base-leakage compensation network [10]. Mattia et al. (2014) proposed a resistor less sub-bgr scheme, where a na dissipated type bgr circuit with a self-biased circuitry is operated under 1 v power supply [11]. Zhu et al. (2016) proposed a low line sensitivity mosfet-only sub-threshold bgr with no amplifiers. The low sensitivity was implemented by the variance of two paired currents and second-order compensation. Therefore, temperature stability was improved. Moreover, by using bulk-driven method

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power dissipation was reduced [12]. However, the temperature coefficient and the distribution (σ/μ) of vr are found large. A 4th-order curvature-compensated cmos bgr is designed by xiaoyun et al. (2011), which used a high-resistive poly register to generate an optimized ratio of the register based on the temperature. However, the ratio of the emitter area of bjt and resistance need to revise properly [13]. Seok et al. (2012) recommended a 2t v_{ref} with several variants that offer sub-nw power dissipation and operation at 0.5 v while sustaining viable temperature coefficient, line sensitivity and psrr [14]. A reference voltage generator consisted of sub-threshold mosfets is proposed by huang et al (2006), where channel length modulation compensation was employed [15]. In this research, optimizing the ration of registers and transistors, the improvement of the effect of temperature was done. However, it produces large temperature coefficient. Another research from magnelli makes the design such as all the existing resistors in the circuit was operated in sub-threshold region [16]. The circuit shows improvement in power dissipation however, the tc still too large. Moreover, the circuit needs two kinds of nmos for the reference voltage, which eventually raises the production costs.

Finally, it is obvious that due to a wide range of drain voltage variation and a stable VR (1.2 V), a BGR based voltage reference circuit is required for high voltage generation process in RFID transponder EEPROM. Therefore, in this research, an improved BGR circuit is designed, which is able to deliver a stable voltage to low power applications.

II. METHODOLOGY

In analog circuit design, a VR is produced from two voltages, which have two opposite sign temperature coefficients and multiplication numbers. Therefore, the output voltage becomes independent of temperature. Conventionally, the voltage drop (VBE) across two base-emitter junctions (BJTs) changes complementary to absolute temperature (CTAT) [17]. On the other hand, if the current densities between these two BJTs are unequal, then the voltage across VBE is found to be proportional to absolute temperature (PTAT). Thus, the PTAT voltage could be added to the CTAT voltage with appropriate measuring numbers to achieve a fixed VR. Figure 1 shows the overall block diagram of the BGR circuit, which is the combination of three fundamental blocks such as start-up circuit, bandgap core, and the op-amp.

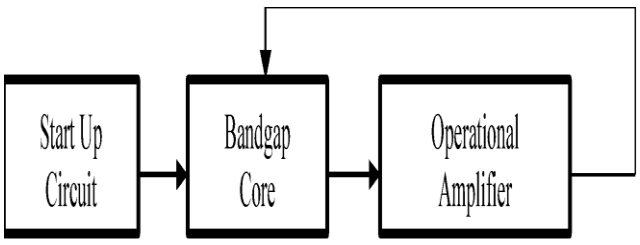

Fig. 1 Block diagram of the BGR circuit

To design the BGR circuit for stable voltage reference, temperature co-efficiency, low power consumption and small chip size play an important role. Therefore, optimized aspect ratios (W/L) of transistors are required for this design. In this design, passive components (such as resistors and capacitors) usage has been minimized to maintain the circuit die area small and compact. During the design process of a BGR circuit, if the entire transistor has zero current when the supply voltage is turned on, the transistors might remain off due to a loop. This loop can hold the zero current for both branches. Consequently, it is essential to inject current in the bandgap core circuit for successful operation, which is done by the startup circuit. At the steady state, this circuit as well turns off. Figure 2 shows the schematic diagram of the designed BGR circuit.

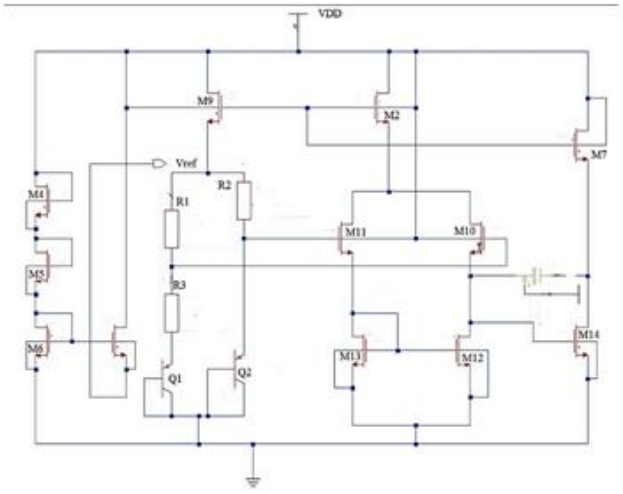

Fig. 2 Schematic diagram of the designed BGR circuit

In this work, a very simple start-up circuit is used, as shown in Figure 2. From the Figure, it is shown that only four transistors (M4. M5, M6, and M8) are required to design this start-up circuit. Figure 2 shows the most significant part known as bandgap core of a BGR circuit, which mainly generates the reference voltage required for the proposed HVG to assist the voltage regulation process. From the figure, it is found that Node A and Node B are operated as the input node of the op-amp circuit, which is of equal voltages. All three resistors (R_1, R_3, and R_2) utilized in this design are sbnp (N+ poly Unsalicide Resistor) resistances, which are vertically inherent of Q1 and Q2 BJTs of CMOS process. From Figure 2, it is clearly shown that this circuit has two branches in this core circuit. Initially, a current of the first branch (R_1 and R_3) is higher than that of the second branch (R_2). In this case, the current through each branch is equal due to steady-state. Therefore, the voltage across Node A and Node B are found equal, so the voltage across resistor R_2 can be written as:

$$V_{R2} = I_2 R_2 = \frac{V_{BE2} - V_{BE1}}{R_3} X\ R_2 = V_T\ ln\ ln\ (n)\ X\ \frac{R_2}{R_3}\ (1)$$

Where n is the no of parallel BJTs. In addition, V_T is the thermal voltage $V_T = K \times Tq$, which is directly proportional to absolute temperature (T). V_{R2} is a positive TC voltage. It is known that BJT is conversely proportional to temperature.

As a result, the output voltage equation can be written as:

$$V_{out} = V_{R2} + V_{BE2} = \left[V_T \; ln \; ln \; (n) \; X \; \frac{R_2}{R_3}\right] + V_{BE2} \quad (2)$$

In this research, the overall BGR needs a simple two-stage op-amp circuit, which is mainly used to drive the bandgap core. In addition, the op-amp is designed in a way that, its output voltage becomes insensate to the supply voltage variation. Because of this, the generated reference voltage also becomes insensitive to supply voltage. The schematic of the op-amp circuit as shown in Figure 2 has a two-stage CMOS differential amplifier, where transistor M10 and M11 are differential pairs and M12 and M13 are acted as a load. The current mirror is formed by M2 and M9, which supplies the bias current to the differential pair. On the other hand, the second stage is the common-source amplifier consists of transistor M14, which is connected with current source transistor M7 with an active load. Moreover, a capacitor C1 is incorporated in the negative feedback path of the second stage, which function is to improve the Miller effect existed in M14 and thus give a dominant pole to the op-amp circuit [18]. The high gain amplifier is required to design the bandgap voltage generator as the output current of the op-amp to drive the bandgap core. Moreover, the transconductance of a MOSFET is not high enough to drive the core. Therefore, the two-stage differential amplifier is chosen for this research work. In addition, this type of op-amp is insensitive to the supply voltage variation VDD. As a result, current mirroring transistors M2 and M9 have been employed in this design, which remains almost constant with respect to voltage variation. Therefore, the proposed op-amp circuit is able to function properly with its own output current. In this circuit, VDD indicates the supply voltage, V_{ref} denotes the output of the circuit, VSS represents the analog ground, and the overall BGR design parameters are listed in Table 1.

Table. 1 Circuit parameter for BGR circuit

Transistor	The aspect ratio (W/L) (µm/ µm)
M2, M9, M4, M5, M6	1/2
M7, M10, M11	1/5
M12, M13	1/4
M8	1/10
R1	5.5 KΩ
R2	5.8 KΩ
R3	10.1 KΩ
C1	0.66 fF
Q1, Q2	2x2 µ

The chip layout of the proposed BGR circuit is shown in Figure 3, where the chip occupies a small area of 101.5 µm × 41.7 µm. During the design process, all transistors and capacitors are placed in a manner that reduces the mismatch and parasitic capacitance. Finally, the microphotograph of the designed chip with I/O pads is shown in Figure 4.

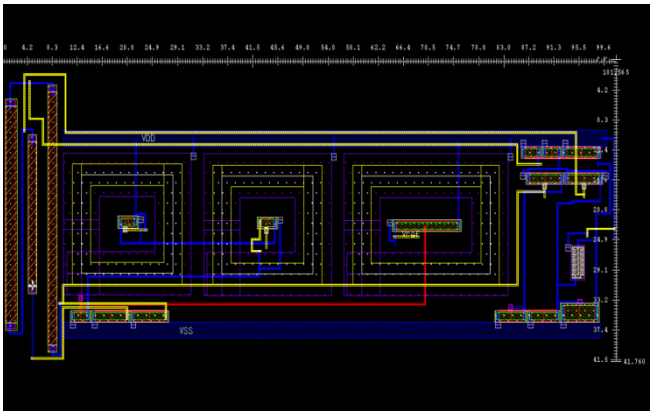

Fig. 3 The layout diagram of the BGR without pads

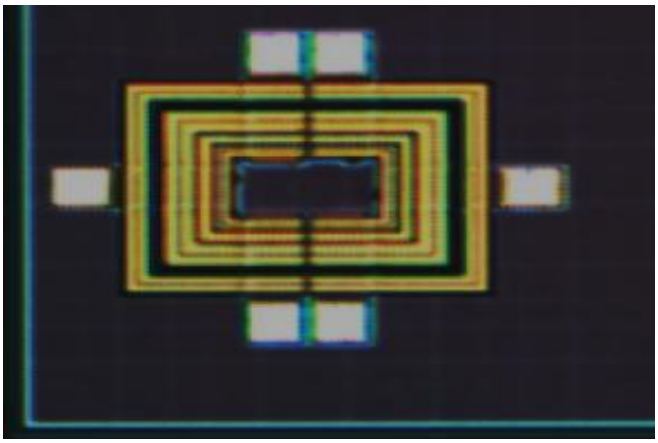

Fig. 4 The microphotographs of the BGR with pads

III. RESULTS AND DISCUSSION

The BGR circuit is simulated using ELDOSPICE simulator (Mentor Graphics) in Silterra 0.13 µm CMOS process. Simulating temperature range is set to -40 ^{0}C to 120 ^{0}C with a supply voltage alternating from 1 V to 2 V. A linear relation is shown in Figure 5, where the generated reference voltage ranges from 0.65 V to 1.15 V. To check the designed BGR circuit for real-life implementation statistical analysis named corner analysis has also been done to check the circuit performance. To determine the reference voltage of the BGR circuit, the post-layout simulation is done and shown in Figure 5.

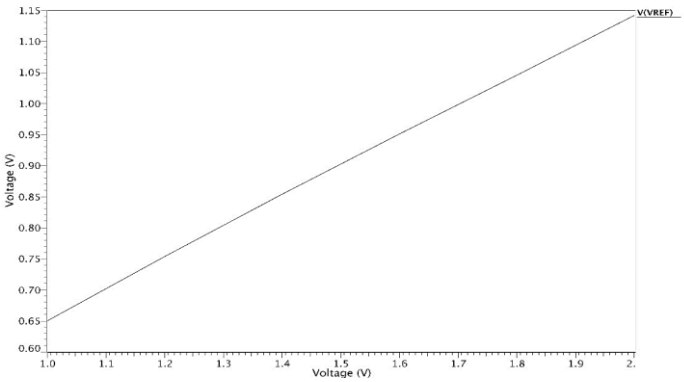

Fig. 5 Variation of the V_{ref} depending on the VDD

In this design, the designed BGR is verified in different power supply voltages at temperature 27 ^{0}C to check the functionality, as shown in Figure 5. According to the characteristics of the curve as shown in Figure 5, until 1.2 V reference voltages output the BGR circuit shows linearity. Therefore, from Figure 5 it is clear that, if the supply voltage is varied from 1 V to 2.1 V than the reference voltage varies only 0.5 V in a linear way. It is also shown in Figure 5 that the designed BGR is able to produce 1.2 V, which meet the specs for the proposed HVG circuit.

In order to validate the circuit in different temperature, the BGR circuit is simulated and the output waveform is shown in Figure 6. According to the figure, the temperature variation from -40 ^{0}C to 120 ^{0}C, while reference voltage V_{REF} varies very only 0.5 V from 80 ^{0}C to 120 ^{0}C and remains steady from -40 ^{0}C to 70 ^{0}C. This is achieved by summing a positive TC voltage and a negative TC voltage.

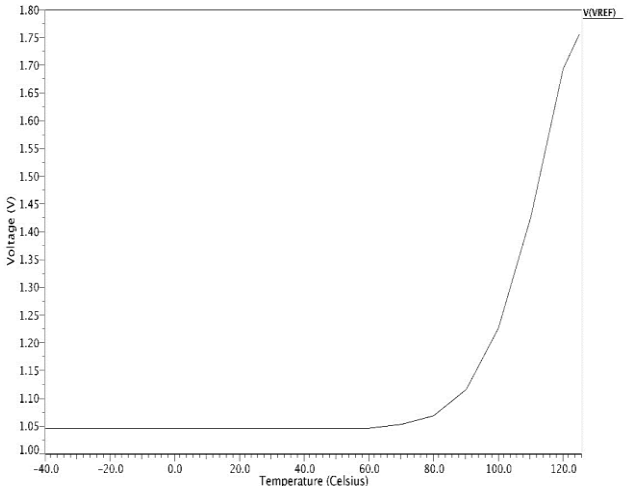

Fig. 6 V_{ref} depending on the temperature of BGR

Like every other circuit, an important measurement is accuracy with respect to temperature. This is known as temperature Coefficient (TC). The parameter also illustrates how the circuit showed accurate results in different frequencies. The calculation of the TC is shown in equation 3.

$$TC = \left[\frac{V_{MAX}-V_{MIN}}{V_{Nominal}\times(T_{MAX}-T_{MIN})}\right] \times 10^6 \quad (3)$$

By observing Equation 3, it is being clear that smaller TC value means an accurate circuit despite the difference in Temperatures or frequencies. In this research, the designed BGR circuit is simulated at room temperature (27 ^{0}C) and TC is found 41.6 ppm/°C.

As the target of this research works is to make the circuit energy efficient, so during the design process, the circuit transistor optimization took an important role to reduce the power dissipation. Therefore, due to successful optimization of the transistors and the other passive elements, the designed BGR consumed only 1.4 µW power undersupply voltage 1.2 V. The brief performance analysis of the designed BGR is illustrated in Table 2.

Table. 2 Performance summary of the designed BGR

Parameter	This Work	[19]	[20]	[21]	[22]
Supply Voltage (V)	1.2 V	0.6	1.2	1.2	3.3
Power consumption (µW)	1.4	NA	36.1	59.5	7.6
Reference voltage (V_{ref}) (V)	1.1	400m V	602m V	850 mV	800 mV
Temperature range(^{0}C)	-40 to 125	-40 to 100	0 to 100	-25 to 85	-40 to 85
Temperature coefficient (TC) (ppm/°C)	41.6	93	2.2	11	20
Library Files(µm)	130	130	130	130	130

Finally, Table 2 shows a detailed performance summary of the designed BGR with recently published research works. According to the table, it is clearly found that the designed BGR consumed the lowest power, which is only 1.4 µW compared to other recent research works [19-22]. Therefore, it is obvious that the designed BGR is more energy efficient for low power designs like RFID transponder. In addition, it is able to generate a higher reference voltage, which can meet the requirement of an RFID system. Moreover, this designed BGR can cover more temperature range, which is found -40 to 120 compared to other works as shown in Table 2. As, to reduce the power dissipation of the designed BGR circuit is the main objective of this research works, so it can easily state that this design is suitable for low power applications. Another important feature of this BGR circuit is that despite dissipating very low power, the results obtained in *TC* is 41.6 ppm/°C which is lower than other researchers.

IV. CONCLUSIONS

In this research, the BGR circuit is designed using EDA tools of Silterra 0.13 µm CMOS process, which is found energy efficient due to low power dissipation. In this work, less number of a transistor with proper size and limited usage of the passive element like capacitor, resistor is helped the BGR circuit to dissipate less power. Simulated output results showed that the optimized BGR is able to generate 1.1 V as the reference voltage with 41.6 ppm/°C as temperature coefficient. In addition, from the simulated outputs, it is clear that the designed BGR is well fit with temperature and process variation, which eventually make it compatible with low power and energy-efficient applications like RFID transponder, sensors, ADCs etc.

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