

A Modified Series Voltage Controller for Power Conditioning



Jeevan J. Inamdar, K. Iywaraya Annapoorani

Abstract : A compensation method for mitigation of voltage related power quality problems with the use of Series Voltage Regulator well known as Series Active Power Filter or Dynamic Voltage Restorer is presented in this paper. The classical control algorithm used for series voltage regulator based on the Park transformation is modified by introducing a Selective Harmonic Filter at detection stage of source current in order to compensate harmonic frequencies which mainly affect power frequency voltages. The significant outcomes are sag restoration, reduction of total harmonic distortion and removal of transients from the supply voltage. Thus it makes possible to improve performance of series voltage controller as power conditioner to mitigate various voltage related power quality issues. The proposed approach is cost effective because same series voltage controller can be used as power conditioner by modifying control strategy used. Also it is possible to eliminate use of PI controller from control circuitry. The usefulness and robustness of the proposed mitigation strategy is confirmed by simulation studies. The presented series voltage controller has ability to mitigate the power quality issues arising due to charging of electric vehicles.

Keywords: Series Active Power Filter, Dynamic Voltage Restorer, Park Transformation, Power Quality.

I. INTRODUCTION

The Power-frequency disturbances are defined as events related to the power frequency caused due to switching operations. As soon as the event producing the disturbance is cleared these disturbances get diminished with time. This helps the power system to come back to its normal operating condition. The acknowledgment of Low-frequency disturbances is very easy. The voltage sag can be recognized by observing dimming of lights and voltage well is observed when lights shine brighter because of rise in the voltage. The detection and measurement of these low-frequency disturbances is easy but restitution is monotonous work. On the other hand both detection and reparation of Transients is less complicated than low-frequency events [2]. There are various measures available to deal with low frequency disturbances like Isolation transformers, Voltage regulators, Static Uninterruptible Power Sources (UPSs), Rotary UPS.

However, these methods have limitation for removal of low frequency variations [2]. To eliminate the distortion the source voltage most common device used is Series Voltage Regulator which is often called as Dynamic Voltage Restorer or Series Active Power filter. The literature shows usefulness of Series APF for mitigation of power frequency voltage variations. In [4], a novel control method for stabilizing power system voltage by operating series voltage controller as an active capacitor to compensate voltage flicker has been reported. The development and testing of a series active power filter functioning as a sinusoidal current source for in phase compensation of mains voltage is reported in [5]. The Line disruptions like voltage changes, sags, dips, noise, flicker and harmonics are reduced by inclusion of a voltage conditioner [6]. A critical analysis of various topologies for power circuits used in power line conditioners designed to attenuate or remove disturbances in the electric power system is presented in [7]. A three-phase three-wire series active power filter based on the generalized p-q theory is proposed in [8]. In [9], the PI control strategy based on low pass to band pass transformation for series hybrid active power filter is discussed. A novel series-shunt hybrid active power filter based on fundamental magnetic potential self-balance is reported by [10]. A series active filter incorporated with a 12-pulse diode rectifier to reduce transients and improve stability based on a recurrent discrete Fourier transform control is elaborated in [11]. The authors in [12] have carried out an investigation of a series-connected pulse width modulated inverter for high-power applications by incorporating open-loop control. A new system design for a series hybrid power filter is executed for the all kinds of harmonic loads is proposed by [13]. The control strategy based on the vectorial theory dual formulation of instantaneous reactive power is used for control of hybrid series active filter is proposed in [14]. A series hybrid active power filter based on controllable harmonic impedance to minimize inverter capacity and improve system reliability, is deliberated [15]. The compensation of current harmonics arising because of high-power rectifiers is presented and analyzed [16]. A mathematical representation of the Series Hybrid Active Power Filter is established in [17] to improve the filtering capacity. A new control algorithm for a Series Hybrid Active Power Filter (SHAPF) based on the generalized instantaneous power theory is proposed by [18]. An enhancement of power quality with critical loads for single phase system is carried out by a Transformerless Hybrid Series Active Filter in [19]. A single-phase half-bridge active power filter with series-parallel-resonant LCL filter at output side is proposed to improve power quality [20].

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A Transformerless Hybrid Series Active Filter with a sliding mode control algorithm along with notch harmonic detection method is executed on a Single-phase distribution feeder by [21]. A series active power filter based on a single-phase matrix converter is proposed in [22].

The reduction of the magnetizing impedance is achieved through a hybrid control of fundamental and harmonics magnetic flux to guarantee improved performance of series APF is discussed in [23]. The power quality has been improved by using dynamic voltage restorer in [24, 25] for different load conditions.

The Series Voltage Regulator (SeAPF/ DVR) comprises of a Voltage-Source Inverter (VSI) with a storage element on the DC side [3]. The VSI connected in series to the network through an isolation transformer. The regulator acts as a controllable source of reactive power to attain desired voltage regulation. The ability of the SeAPF/ DVR to mitigate low frequency events is solely because of the control algorithm used to extract components of reference voltage. There are two major theories [3] established for implementing these control algorithms. First is the Instantaneous Reactive Power Theory (IRPT) and second one is the Synchronous Reference Frame Theory (SRFT). This paper considers SRFT for control of DVR with an additional feature of the Selective Harmonic Compensation to enable DVR as power conditioning device.

A modification in classical control algorithms based on the Park transform in the framework of SRFT is carried out by adding Selective Harmonic Filter at detection stage of source current. This modification helps to achieve the goal of mitigation low frequency events within the IEEE standard limits [1]. Also with proposed approach, it is possible to eliminate the use of bulky filters at output terminals of voltage source inverter. The relevant effect would be reduction of Total Harmonic Distortion (THD) of the load voltage at Point of Common Coupling (PCC). Thus it makes possible to improve performance of series voltage controller as power conditioner. The Matlab simulation studies confirmed the usefulness of the proposed mitigation strategy.

The paper is organized as follows. Section II reports operation of DVR with classical algorithms based on the Park transform. In Section III, the proposed modified algorithm is described. Section IV discusses a simulation study by incorporating two control algorithms in DVR to show the effectiveness of the proposed approach. Finally, Section V presents the conclusions of the paper.

II. SERIES VOLTAGE CONTROLLER: SeAPF/ DVR

The Series Voltage Controller is often used to eliminate the distortion of source voltage quality. This also called as Dynamic Voltage Restorer (DVR) or Series Active Power Filter (SeAPF). Hereafter, in this paper the analysis is done by considering Series Voltage Controller as Dynamic Voltage Restorer (DVR). Fig. 1 shows block diagram of DVR. As shown in block diagram a voltage V_f is generated to complete the source voltage to ideal sinusoidal voltage by following the waveform of the load voltage V_L or the source voltage V_s . Thus DVR maintains the (distortion free) load voltage at PCC for protecting other connected sensitive loads.

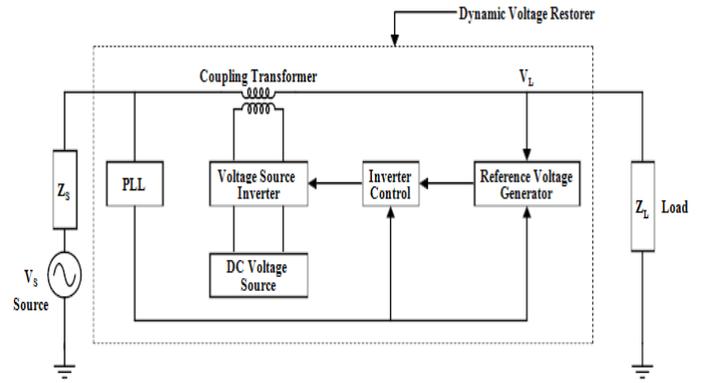


Fig. 1 Block diagram of Dynamic Voltage Restorer [3]

As shown in Fig. 1 the DVR is connected in series with both source and load through a coupling transformer. For eliminating high-frequency components occurring due to the switching of power electronic devices a LC filter is connected at the inverter output. The controller is heart of the DVR. It provides control signal to Voltage Source Inverter (VSI) by using three main strategies which are used to determine the reference signal, first control strategy is to detect the source current which is used to generate a voltage proportional to source current harmonics at the output of DVR. In second control strategy the controller detects the load voltage and DVR generates the voltage with the same harmonic content but with opposite phase as that of the load voltage. The third approach is Hybrid of first and second in which detects source current as well as load voltage and DVR generates a voltage.

A. Mathematical Model and Control Configuration of DVR

The mathematical model used is developed by using well-known dq0 transformation (Park's transformation) given in (1), where ω is the angular frequency in radians per second. Fig. 2 shows block diagram of control algorithm based on Park transformation (CA_{PT}). The controller design is based on hybrid approach discussed earlier. The desired value of load voltage is obtained at output of VSI by employing this control algorithm.

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} 2\sin\omega t & 2\sin(\omega t - \frac{2\pi}{3}) & 2\sin(\omega t + \frac{2\pi}{3}) \\ 2\cos\omega t & 2\cos(\omega t - \frac{2\pi}{3}) & 2\cos(\omega t + \frac{2\pi}{3}) \\ 1 & 1 & 1 \end{bmatrix} * \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

For generating a unit sinusoidal wave in phase with the main voltage the Phase Locked Loop (PLL) circuit is used. The d-q transformation and the phase information of load voltages is used to convert three phase source currents (I_{sa}, I_{sb}, I_{sc}) to d-q domain currents I_{sd} and I_{sq} . These currents are further passed through a low pass filter to generate reference control signals I_{sd}^* and I_{sq}^* given by (2) and (3).

$$I_{sed} = I_{sLPPFd} - I_{sd} \quad (2)$$

$$I_{seq} = I_{sLPPFq} - I_{sq} \quad (3)$$

The control signals I_{sed} and I_{seq} along with I_{s0} are converted back to stationary frame by Inverse Park Transformation. These stationary control signals are then passed through unit delay block to PWM generator for generating switching signals for voltage source inverter.

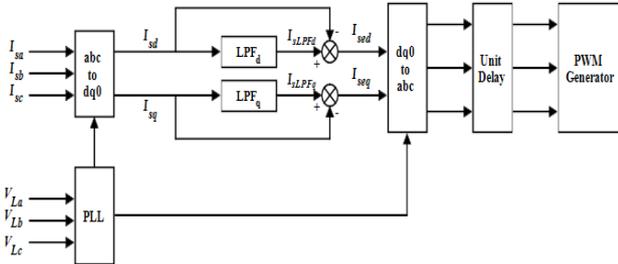


Fig. 2. Block scheme of control algorithm based on Park transformation (CApt)

III. PROPOSED CONTROLLER DESIGN FOR SERIES VOLTAGE CONTROLLER

The proposed modified controller design with modified algorithm (CA_{mod}) is shown in Fig. 3. A block “Selective Harmonic Filter” (SHF) is added to controller design scheme of Fig. 2 before Park transformation block. Each phase current is passed through a band pass filter before applying converting to d-q domain. Thus three phase source currents (I_{sa} , I_{sb} , I_{sc}) are passed through band passed currents to obtain new set of three phase source currents (I_{sa}^* , I_{sb}^* , I_{sc}^*) which are further converted to d-q domain as I_{sd}^* and I_{sq}^* . These currents are passed through a low pass filter having cut-off frequency equal to fundamental frequency. The direct and quadrature components of source reference current I_{sed}^* and I_{seq}^* are obtained using (4) and (5) respectively.

$$I_{sed}^* = I_{sLPPFd}^* - I_{sd}^* \quad (4)$$

$$I_{seq}^* = I_{sLPPFq}^* - I_{sq}^* \quad (5)$$

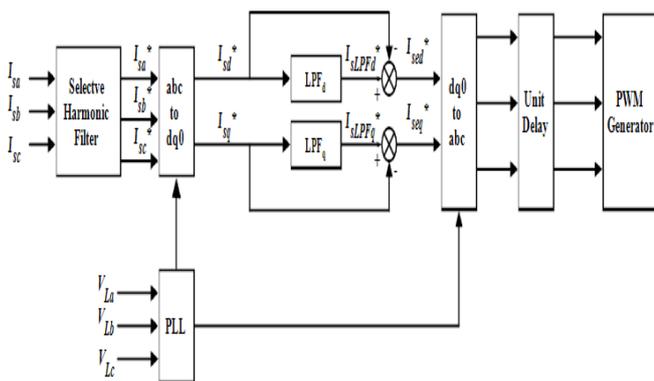


Fig. 3. Block scheme of proposed modified control algorithm (CA_{mod}).

A. Selective Harmonic Filter Design

A second order Butterworth band pass filter is selected and designed because it has no ripple in the pass band or the stop band and has best time domain response. The transfer function of filter is given by (6)

$$H(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (6)$$

where, Q is the quality factor of filter and given by (7) as:

$$Q = \frac{F_0}{F_H - F_L} \quad (7)$$

F_H and F_L is higher (upper) and lower cut off frequency respectively. The resonant frequency F_0 is the geometric mean of F_L and F_H . $F_0 = \sqrt{F_H F_L}$ (8)

The damping ratio ξ is sometimes used where $\xi = 2\alpha$ and $\alpha = \frac{1}{Q}$

The range for cutoff frequencies is chosen by simulating the uncompensated system described in section IV and observing THD analysis of load voltage. The lower cutoff frequency (F_H) selected is 250 rad/s and Higher (Upper) cutoff frequency (F_L) is 600 rad/s. The bode diagram of the filter is shown in Fig. 4.

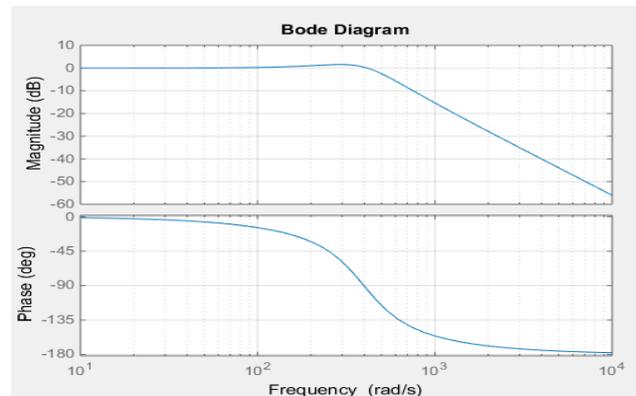


Fig. 4 Bode plot of Selective Harmonic Filter

IV. SIMULATION CASE STUDY

This simulation study shows comparative analysis for operation of series voltage regulator when two control strategies mentioned earlier are implemented. The comparison is carried out by observing reduction of source voltage harmonics and Voltage Sag/Swell restoration capability. The simulation parameters are given Table 1.

Table-I Simulation Parameters

Sr. No.	Parameter	Rating
1	Source Voltage (line to line)	11 kV
2	Source Impedance (X/R) ratio	7
3	Fundamental Frequency	50 Hz
4	Short Circuit Power	100 MVA
5	Three Phase Fault Resistance	1 Ω

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6	Linear Load	5 kVA
7	Non Linear Load (Controllable load)	10 kVA, power factor = 0.9
8	Rectifier with R-C parallel load	R= 100 Ω , C=100mF
9	Passive Filter Inductance	7mH
10	Carrier Switching Frequency	2kHz

A MATLAB/ Simulink model is designed with above mentioned parameters as shown in Fig. 5. The simulation is carried out in discrete mode with Tustin type solver having sample time of 50μs and variable step solver ode45 (Dormand-Prince) with tolerance of 1ms and using non nadaptive algorithm.

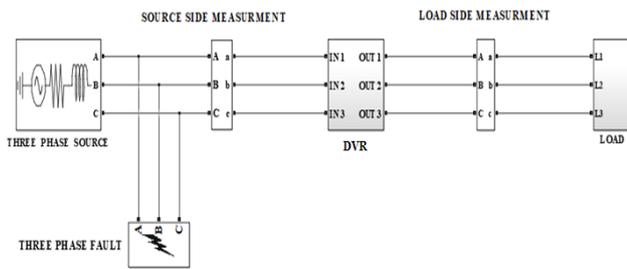


Fig. 5. Overall Simulink Scheme.

A. Simulation Results and Discussions

For accomplishing analysis various load conditions considered. Among various types of sags three phase unbalanced sags [2] are selected for investigation tabulated in Table 2. The effectiveness of proposed algorithm is verified through operation of DVR to compensate these six types of unbalanced sags under nonlinear load environment.

Table-II. Types of Three Phase Unbalanced Sags [2]

Case	Fault Type	a) Star Connected Load	b) Delta Connected Load
1	Three Phase	Type A	Type A
2	Two phase to Ground	Type E	Type F
3	Phase to Phase	Type C	Type D
4	Single Phase	Type B	Type C*

Further, results are interpreted by considering both algorithms. The simulation time selected is 0.5 seconds. The change in per unit RMS value (about 0.35 pu) due to fault is shown in Fig. 6.

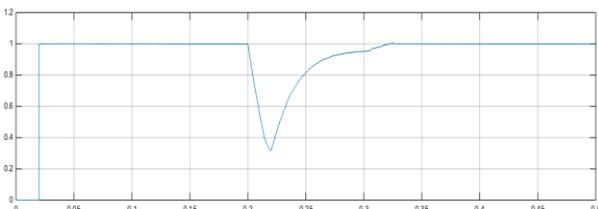


Fig. 6 P.U. change in RMS value due to fault.

The simulation results with control algorithm CA_{pt} for case 1 with star connected load (Type-sag) are shown in subsequent figures. The load voltage, injected voltage by controller and supply voltage restored are shown in Fig. 7a, Fig. 7b & Fig. 7c respectively. The THD plot for load voltage during sag period is shown Fig. 8 and Fig. 9 shows

THD plot of supply voltage with controller operation respectively.

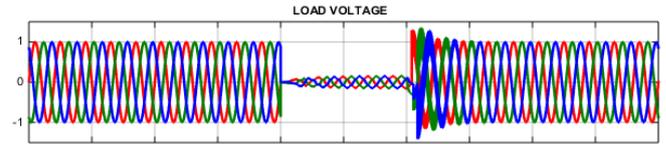


Fig. 7a) Load voltage with CA_{pt} for three phase fault, Star connected load (Type A sag)

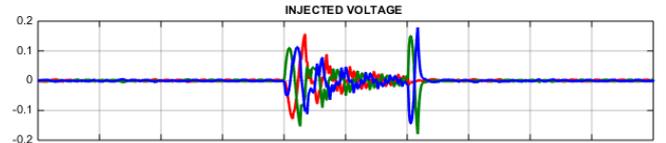


Fig. 7b) Injected voltage with CA_{pt} for three phase fault, Star connected load (Type A sag)

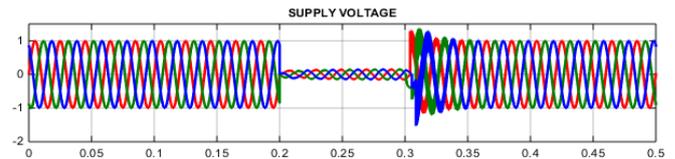


Fig. 7c) Supply voltage with CA_{pt} for three phase fault, Star connected load (Type A sag)

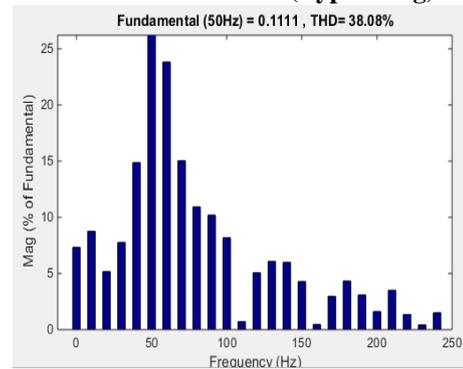


Fig. 8 THD of load voltage during sag period

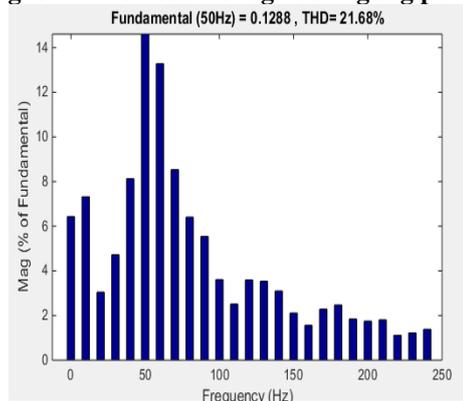


Fig. 9 THD of supply voltage with DVR- CA_{pt}

Fig. 7a to Fig. 7c show that, though there is injection of an antiphase component to load voltage in order to restore it during fault condition, the sag is not getting restored completely because of fact that there is loss of energy during restoration. Also the voltage harmonics along with transients are also present in supply voltage which shows that operation of series voltage controller is not satisfactory.

As shown in Fig. 8 the Total Harmonic Distortion (THD) is 38.08 % before operation of SeAPF while Fig. 9 shows that THD is reduced to 21.68 % when series voltage regulator is operated. The comparison of two values shows that voltage THD with control algorithm 1 is above IEEE level for restoring region. In order to reduce this THD further, a new scheme is simulated using modified control algorithm CA_{mod} . The supply voltage restored with modified control algorithm CA_{mod} for Type-sag is shown in Fig. 10 and Fig. 11 shows THD plot of supply voltage with controller (DVR) operation.

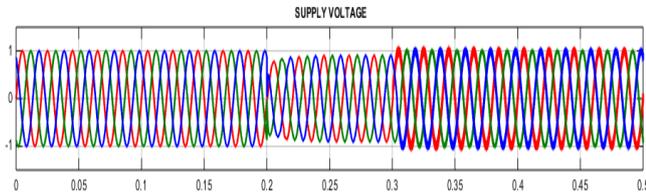


Fig. 10 Supply voltage with CA_{mod} for three phase fault, Star connected load (Type A sag)

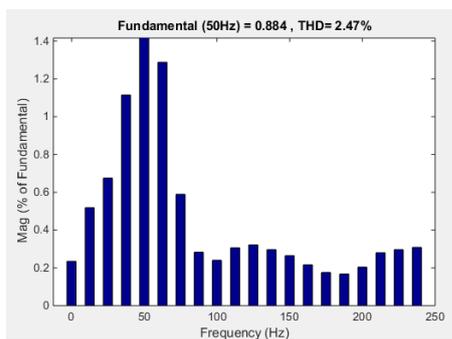


Fig. 11 THD of supply voltage with DVR- CA_{mod}

Fig. 10, clarifies that, the voltage sag is restored with improved magnitude and with fewer distortions. As shown in Fig. 11, the Total Harmonic Distortion is reduced to 2.47% which is within limits of IEEE [1]. Thus, operation of series voltage controller is satisfactory because it is able to restore voltage magnitude as well as to eliminate voltage harmonics within prescribed limits. The results obtained by scheme with CA_{mod} are more reliable as compared to that with CA_{pt} . In order to investigate the effectiveness of proposed control algorithm, all cases of Table 2 have been simulated using CA_{pt} and CA_{mod} and comparison based on various voltage sag indices is presented in subsequent discussions.

B. Result Analysis

In order to check the goodness of the system quality after compensation various indices are taken into consideration.

▪ Voltage Total Harmonic Distortion (THDV)

Harmonic distortion is a good indication of the quality of the system output voltage. According to IEEE 519-1992 [1] the expression of the THDV measured at the point of common coupling is given by (9) follows,

$$THDV = \frac{THDV_a + THDV_b + THDV_c}{3} \quad (9)$$

In order to study robustness of proposed system Harmonic Compensation Ratio (HCR) is calculated. The HCR factor is calculated by (10)

$$HCR = \frac{THD \% \text{ after Compensation}}{THD \% \text{ before Compensation}} * 100 \quad (10)$$

▪ Voltage Sag Indices

The voltage sag indices are symbols of the recovery of voltage quality. These indices are able to give correct feedback of the system performance because of their sensitivity to any kind of disturbance. There are various sag indices given in [2]. Among these Detroit Edison Sag Score (SS), Voltage sag lost energy index (VSLEI) are taken into consideration for checking effectiveness of system.

▪ Detroit Edison Sag Score (SS):

The first voltage sag index which is useful for commitments between utilities and consumers is Sag Score [2]. This is defined by (11) [23]

$$SS = 1 - \frac{V_a + V_b + V_c}{3} \quad (11)$$

where V_a , V_b , and V_c are per unit rms values of load voltages during sag period. The recovered voltage after compensation should have SS value close to 0.

▪ Voltage Sag Lost Energy Index (VSLEI):

For the sag period the load voltage is below normal. This causes reduction of the energy delivered to the loads. The Voltage Sag Lost Energy Index gives this lost energy (W_{loss}) defined by (12) [2].

$$VSLEI = \sum_{p=a,b,c} T_p * \left(1 - \frac{V_{ph}}{V_{nom}}\right)^{3.14} \quad (12)$$

where V_{ph} is a phase voltage and V_{nom} is nominal voltage for the sag event, and T_p is the sag duration in milliseconds for each phase.

Each fault is applied for duration of 0.2–0.3 second i.e. 100 ms (5 cycles). Table-III shows the uncompensated system results to be defined and compared with the compensated system results after using the CA_{pt} and CA_{mod} respectively as depicted in Table-IV and Table -V. From Table 5, it is evident that the THDV percentages are within IEEE limits [1], for all cases under study. Besides, it is notable, as shown in Table 5, that the Sag Score level and Sag Lost Energy have met the IEEE recommendations [1]. Hence the DVR with modified control algorithm is able to achieve the required goals of minimizing voltage harmonic distortion, sag score level and sag lost energy. For sag type A(Y), the sag score is as high as 84.67% for uncompensated system and 79 % for system with CA_{pt} ; the proposed modified control algorithm achieves better result with 10% sag score. The significant outcome of proposed modified control algorithm is that sag lost energy is reduced from 177.90 Joules for uncompensated system and from 143.16 Joules for compensated system with CA_{pt} to 0.22 Joules.

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The harmonic compensation ratio (HCR) for compensated system with CA_{pt} is varying from 83.14 % to 63.73 % for A to F type of sags respectively whereas the with proposed modified control the HCR has come down to 8.94 % to 5.68 % for A to F type of sags respectively. Fig. 12, Fig.13 and Fig. 14 shows comparison of THDV, % SS and VSLEI for three cases viz. uncompensated system, compensated with CA_{pt} and compensated system with CA_{mod} for various sag types. Fig. 15 shows HCR variation in order to show robustness of proposed approach.

Table -III Uncompensated system results

Parameter	A (Y)	A (Δ)	B	C	C*	D	E	F
THDVa	25.89	25.89	45.1	63.8	45.1	63.8	41.53	41.54
THDVb	30.43	30.43	55.2	74.0	55.2	74.0	41.18	41.18
THDVc	32.27	33.27	76.5	72.0	76.5	72.0	71.85	71.86
THDV	29.53	29.86	59.0	69.9	59.0	69.9	51.52	51.53
SS(%)	84.67	85.00	52.3	69.0	53.6	68.6	77.67	77.67
VSLEI (J)	177.9	180.0	70.4	97.4	73.9	95.8	149.9	149.9

Table -IV Compensated system results with CA_{pt}

Parameter	A (Y)	A (Δ)	B	C	C*	D	E	F
THDVa	21.68	21.69	32.0	44.1	32.0	44.1	24.07	24.0
THDVb	25.08	25.08	37.5	51.9	37.5	51.8	25.62	25.6
THDVc	26.89	26.89	51.7	51.5	51.7	51.5	48.82	48.8
THDV	24.55	24.55	40.4	49.2	40.4	49.2	32.84	32.8
SS(%)	79.00	78.67	38.3	65.0	35.0	65.0	70.67	57.6
VSLEI (J)	143.16	141.2	17.3	79.5	11.4	79.0	108.0	53.4
HCR	83.14	82.22	68.5	70.3	68.5	70.3	63.74	63.7

Table-V Compensated system results with CA_{mod}

Parameter	A (Y)	A (Δ)	B	C	C*	D	E	F
THDVa	2.47	2.47	2.72	2.76	2.71	2.77	2.71	2.71
THDVb	2.73	2.73	3.63	3.14	3.63	3.16	2.74	2.74
THDVc	2.72	2.72	3.52	3.27	3.52	3.15	3.33	3.33
THDV	2.64	2.64	3.29	3.06	3.29	3.03	2.93	2.93
SS(%)	10.00	10.00	3.33	4.00	3.33	4.67	6.00	6.33
VSLEI (J)	0.22	0.22	0.07	0.02	0.07	0.10	0.10	0.12
HCR	8.94	8.84	5.58	4.37	5.57	4.33	5.68	5.68

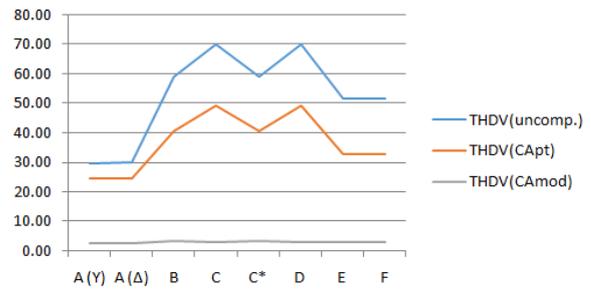


Fig. 12 Plot of %THDV comparison

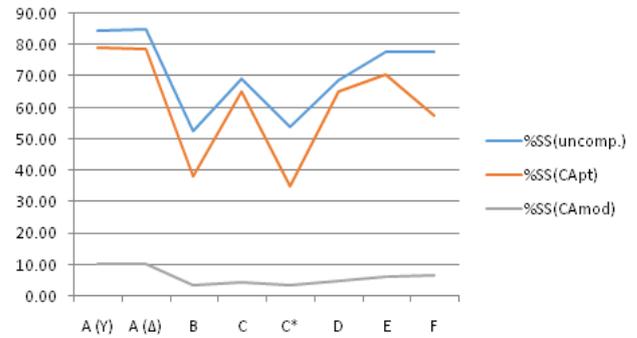


Fig. 13 Plot of % SS comparison.

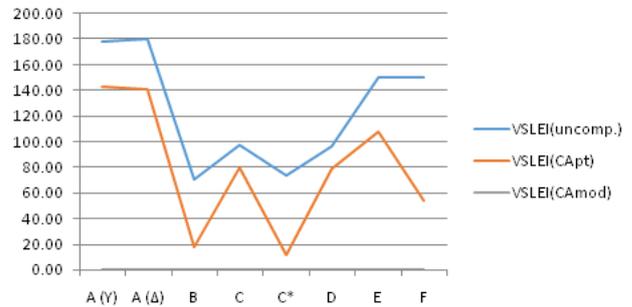


Fig. 14 Plot of VSLEI comparisons.

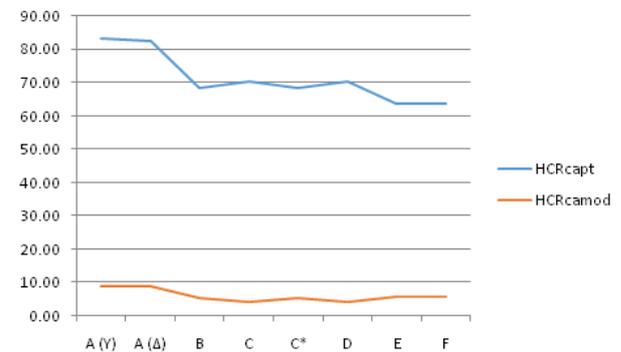


Fig. 15 HCR comparisons with two algorithms.

VI. CONCLUSION

This paper has proposed a modified Series Voltage Controller with Selective Harmonic Compensation for mitigation of power quality issues. The methodology implemented has modified classical control algorithm based on the Park Transformation to generate control signals for inverter part of series voltage controller.



The modified control algorithm improves quality of system voltage by compensating a variety of power quality issues like Voltage Sag, Harmonics and Transients effectively as compared to traditional approach. This facilitates proposed series voltage controller as multi-functional compensator or power conditioner. Simulation case study confirmed the usefulness of the proposed mitigation strategy and gave a quantitative idea in terms of Total Voltage Harmonic Distortion and per unit change in supply voltage. Further a comparative study has been carried out by considering various types of voltage sags. The goodness of the system quality is demonstrated by investigating various sag indices. The Harmonic Compensation Ratio comparison illustrates the robustness of proposed method. It is evident that proposed algorithm proves much better than established algorithm. The proposed Series Voltage Controller can be incorporated in power distribution system to compensate power quality issues arising due to charging of Electric Vehicles.

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