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Design and Development of A Modified AXI Based BIST Technique for Memory Architectures

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Abstract:Memory testing and fault detection is an important phase in testing the hardware devices. This improves the overall performance of the system and prevents runtime failures in the devices. Built In Self Test (BIST) is a hardware memory test architecture deployed in many System on Chip devices to enable fault detection. This technique reduces the cost and time needed to test the memory systems. Different BIST modules need to be used to detect faults in different memories. As a result, design complexity increases. In order to overcome these above shortcomings, it is essential to develop advanced extensible Interface (AXI) with Block Random Access Memory (BRAM) and Design and Develop AXI based self-test memory architecture (March Algorithms) to achieve parallel read and write capability. The proposed model reduced the dynamic power and the clock cycles needed for simulation when compared to existing techniques.

Keyword: As a result, design complexity increases.

I. INTRODUCTION

Memory testing is very essential in many crucial applications like military and aviation. Runtime Faults in memories may lead to catastrophic failures in the entire system. To prevent such disasters, researchers developed techniques like Built in Self-Test (BIST), which can detect faults in memories. These BIST techniques require large number of read write operations to be performed on the memory locations. Thus the conventional BIST techniques consume more power and the sequential read write operations increase the latency of the system. These techniques use automatic test pattern generators to generate inputs with high rate patterns which in turn consume high dynamic power. Figure 1 shows the block diagram of the conventional BIST technique. The major blocks present in the Conventional BIST procedure are:

- Test Pattern Generator (TPG)
- Output Response Analyzer (ORA)
- Test Controller

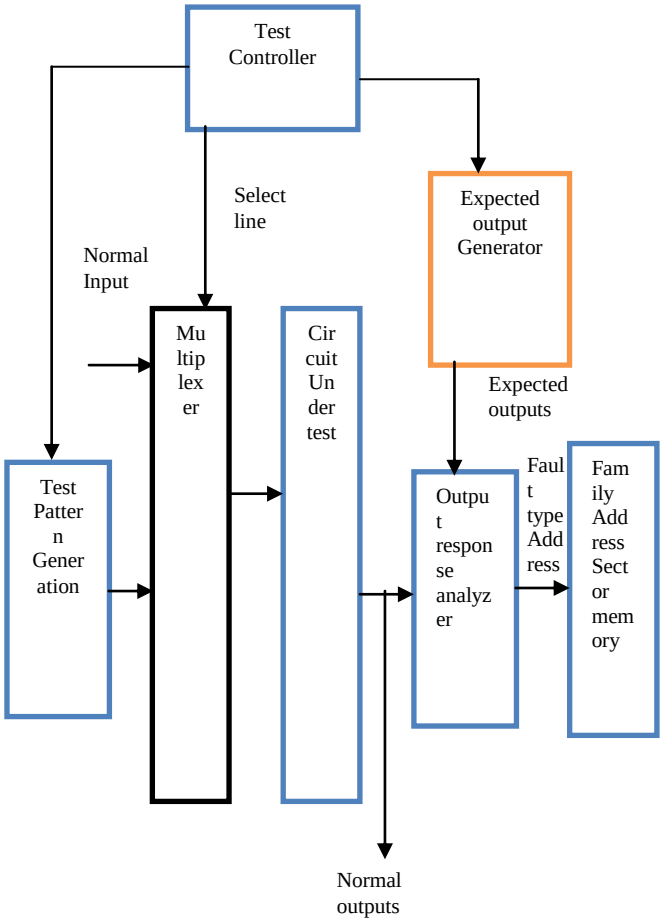

Figure 1: Conventional BIST Block Diagram

The test pattern generator generates the test inputs to simulate the system. This block acts on the instructions of Test controller which instructs on the range and nature of the inputs. The outputs of the TPG are selected using the multiplexer and given to the Circuit under test. The resultant simulation is matched with expected output in the ORA. The block analyses the faults present in the memory if any. TPG consists of several test patterns stored in the RAM, a Linear Feedback Shift Registor (LFSR) and a counter. ORA compares the produces output with the expected once to ensure whether the system is functioning properly or not.

BIST techniques based on Sequential memory operations require large amount of time to complete the diagnosis.

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Further, the task becomes more complicated when systems with multiple memory modules of different types are involved. Such cases require multiple BIST algorithms to identify specific faults.

These shortcoming can be eliminated by using Advanced Extensible Interface (AXI) with Block Random Access Memory (BRAM) and Design and Develop AXI based self-test memory architecture (March Algorithms) to achieve parallel read and write capability.

AXI, is part of ARM's Advanced Microcontroller Bus Architecture specifications. AXI is a one to one interconnection designed for high speed and high performance microcontroller systems. AXI protocol defines how two devices can communicate with each other inside a microcontroller system. It makes sure that the communication is clear and continuous. That way, multiple devices can establish communications parallel without crossing one another. The steps involved in an AXI protocol are:

- Master & slave must "handshake" to confirm valid signals
- Transmission of control signal must be in separate phases
- Separate channels for transmission of signals
- Continuous transfer may be accomplished through burst-type communication

Figures 2 and 3 show the read write procedure in AXI protocol. In figure 2, a 32 bit write address is transmitted from master to slave in a single phase. The write data channel is used to write the data in multiphase. The write response channel is used by the slave in acceptance to the write request. WDATA is a signal which is responsible for multiple data to be written.

The complete write operation has the following steps in order:

- Write address
- Write data
- Write response

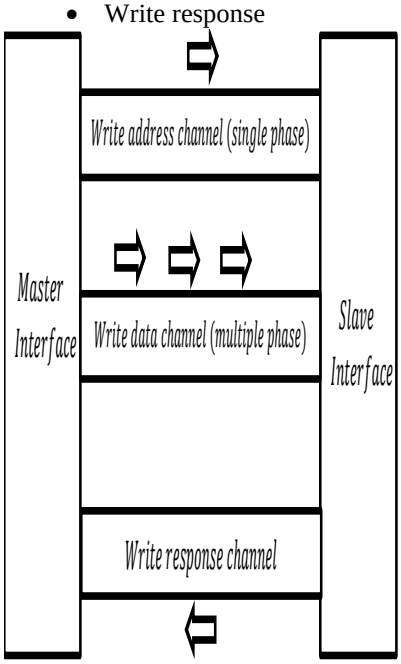


Figure 2. Write Architecture

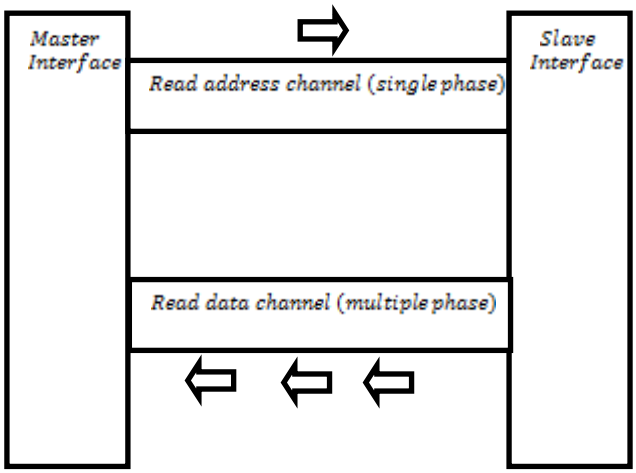


Figure 3. Read Architecture

The read architecture shown in figure 3 shows that read address channel in single phase mode. The read data channel is a multiphase operating mode so that the data can be accessed in parallel. The data reading can be initiated with the address location being transmitted using read address channel and the data transmission is done using the read data channel. The read operation consists of the following steps in order:

- Read address
- Read response

The user can create multiple test cases following these rules to verify the faults in the memory devices. The results have to be checked with the known values to identify the faults. The available BIST architectures are of two types

- Centralized BIST
- Distributed BIST

In any type, the TPG plays a major role by generating the test cases for testing the address and memory locations. In conventional BIST circuits, Linear Feedback Shift Registers are used for test pattern generations. The test patterns generated are categorized as:

- Deterministic
- Algorithmic
- Exhaustive
- Pseudo-exhaustive

Figure 4 represent the general block diagram of centralized and distributed BIST architectures. The BIST controller has to be shared when multiple processors are to be tested [2].

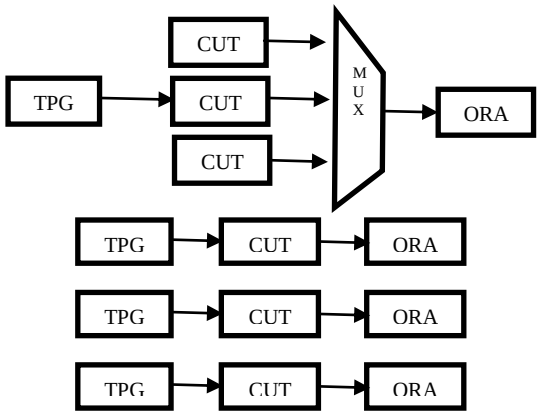


Figure 4: (a) Centralized BIST; (b) Distributed BIST [3].

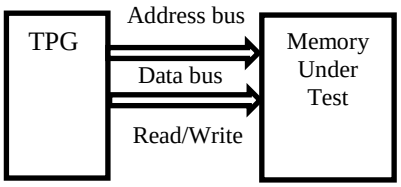


Figure 5: General scheme for testing Memory [4].

Fault models

The faults commonly occurring in the memories are classified into the following types [5, 1, 6]:

- Stuck at Faults (SF): The memory bits are always stuck at a logic 0 or 1.
- Transition Faults (TF): This faults occur when the memory bit fails to transit from one logic to another at the clock cycle.
- Coupling Fault (CF): This fault is said to have exists when writing a cell changes the value of an adjacent cell.
- Address Decoder Fault (ADF): This fault arises when the cell accessing becomes corrupted. Passing an address line with an address sometimes accesses no memory or sometimes accesses multiple locations.
- Neighbourhood Pattern Sensitive Faults (NPSF): This is a kind of coupling fault that acts on multiple memory cells at a time.

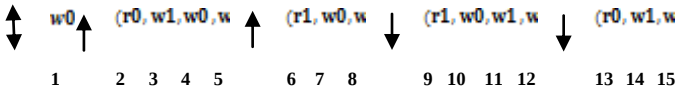
March Test Algorithms

March Test algorithms are used for testing the memory devices. These algorithms consists of a fixed sequence of march elements which are used to perform specific read write operation sequences, to detect the faults in memories [2, 1]. For example,

↑ (**r0,w1**) - March element where r0 and w1 are March primitives.

The ordering of the primitives can be either increasing (↑) or decreasing (↓) or both (↕). r0 represents reading 0 from cell. r1 represents reading 1 from cell. w0 represents writing 0 to a cell. w1 represents writing 1 to a cell.

Existing March-A algorithm



Total Clock pulses (Time=n*15)

In the existing March-A algorithm, initially the Write-0 operation will execute from top to down or down to top. In the next step read-0, write-1, write-0, write-1 and read-1 operations are executed. Similarly in each task the each operation requires each clock pulse and total number of operations requires 15n clock pulses to complete the task.

ReinaldoSilveira et al, [7] has suggested a flexible BIST architecture memory to optimize the existing basic architecture and reduce the area of circuit. The hierarchical FSMs nature would allocate the latest characteristics such as tests of address-decoder to be rapidly included. Any unnecessary test case could be easily eliminated in the proposed method. The implementation doesn't include the repair logic in the speed path. Thus high speed cache memories can also be tested though the proposed technique.

A latest approach suggested by Ryan Pennucci et al [8] has outlined the traditional memory testing drawbacks. The development time have been decreased and by replacing conventional memory testers along with low-cost, instruments of general-purpose, costs of testing are considerably reduced by evading the need for comprehensive BIST circuitry. Unique test cases can be generated and the memory testing can be achieved through them.

Dong Xiang et al, [9] has proposed a pseudorandom generator based Test Pattern Generator (TPG) with weighted single test. The paper also explains Low Power (LP) deterministic BIST & reseeding. The proposed process consists of the following two stages: 1) LP weighted pseudorandom TPG 2) LP deterministic BIST with reseeding. The first stage generates the weights needed for the TPG in generating the test cases. The polynomial selection for the TPG and the insertion of new inputs has been performed thought a novel procedure. The LP capability over all the clock cycles is assured though a reseeding scheme. G. Harutyunyan, et al, [10] researched on the concepts of periodicity and regularity in TPG based on several existing memory fault types. The authors defined rules for achieving these properties in the circuits. A table named Fault Periodicity Table (FPT) is created to store all the types of memory faults that occur in the circuits. The framed rules are tested using Test Algorithm Template (TAT) and verified whether all the faults in the FTP are covered or not.

Preethy K John et al, [11] proposed a fault detection algorithm for memory cores using March – C algorithm. A Configurable Linear Feedback Shift Register (CLFSR) is used to generate the addresses to achieve maximum coverage. The proposed method uses the same n bit CLFSR circuit to generate both the address sequences and the test patterns for detecting the faults. This technique improved the performance of the system in terms of hardware complexity and area of the circuit. The March – C algorithm successfully identifies the stuck at faults present in the memory.

Tan Li et al [12], presented a BIST algorithm based on March algorithm on FPGA to verify the SRAM chip. The proposed March operation consists of 6 stages. In each stage, the initialization parameters are first configured. This process is followed by a series of read write operations in active mode. The time required for the read write operations is very less when compared to the initialization phase.

Mahesh Kumar et al [13], proposed a novel BIST technique for FPGA memory fault detection. The coverage of the proposed algorithm is high and the stuck at 0 and 1 faults are detected. In addition to this CLB faults, bridge faults, wire open and delay faults have been identified uniquely. The technique detects the faults present in the interconnected devices and the CLB's simultaneously. This optimized the circuit in terms of area overhead and testing time.

II. IMPLEMENTATION

High Speed testing architecture using AXI based implementation which will aid

in parallel read and write. This will reduce the testing time significantly.

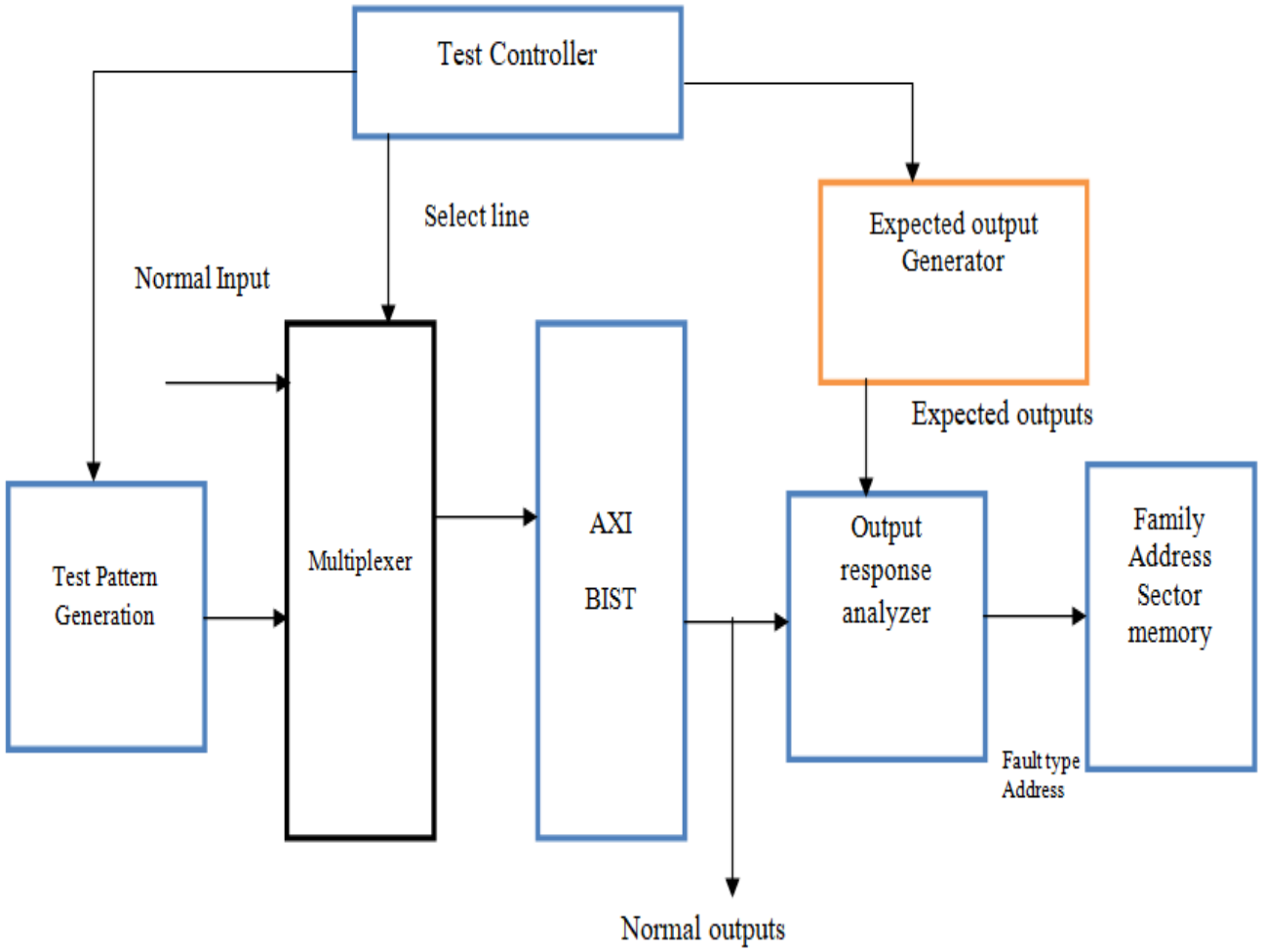


Figure 4: Proposed BIST Block Diagram

Proposed Architecture of AXI with MARCH Algorithm

Proposed MARCH A with AXI

$$(w0,r\uparrow(w1,r1,w0\uparrow(w0,r0,w\downarrow(w0,w1,w\downarrow(w1,w$$

n+1 2n 2n 3n 2n

Total Clock pulses (Time=9n+1)

Flow-Chart

As shown in figure 5, the proposed AXI based March-A algorithm, initially write-0 and read-0 operation executes either top to bottom or bottom to top and it requires n+1 clock pulses. In the proposed algorithm the write and read operations executes in parallel manner. In the second step write1 and read-1 operations requires only one clock pulse, which means in asingle clock pulse write and read operations parallelly executed. The proposed method covers the two types models which are Stuck at faults and Transition faults. The proposed algorithm verifies whether read or write instructions performed or not. Based on the condition it detects the fault model. For example if write '0' or write '1' instruction should perform in all memory locations, the condition will checks the all memory locations. If this conditions fails it comes under stuck at fault model. If the write instruction changes from one state to another state (like initially write '0' instruction and immediately write '1' instruction), the condition should check these sudden transitions. If these condition fails then it will treated as transition faults. In the proposed algorithm requires 9n+1 clock pulses requires in order to complete the algorithm. From this calculations, the proposed algorithm is faster than the existing algorithm and also it uses less number of resources compared to existing algorithm

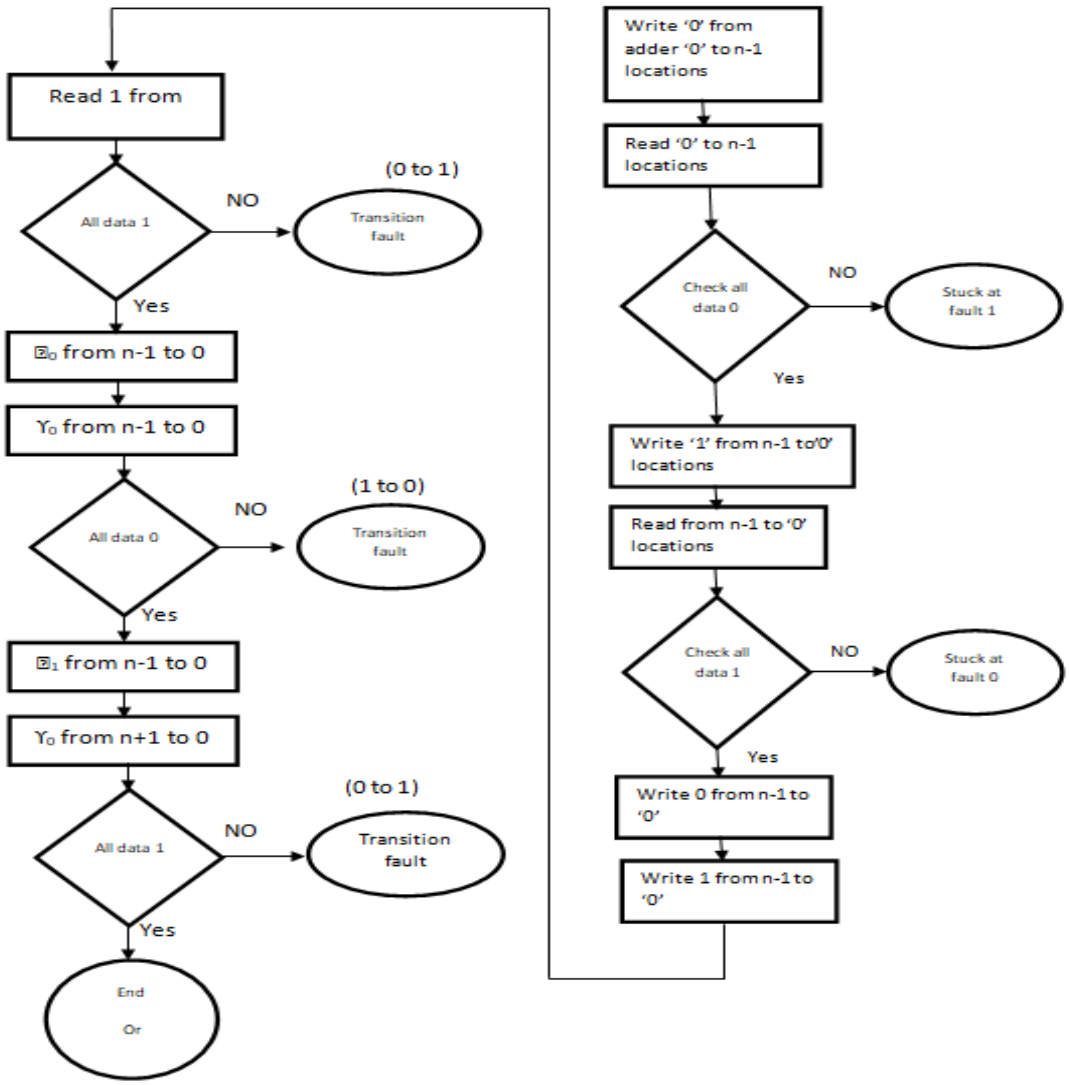


Figure 5: Flow chart

III. RESULTS

This section presents the simulation results of the proposed technique. The simulations are carried out in Vivado 2017. Figure 6 represents the Register transfer level schematic of proposed algorithm.

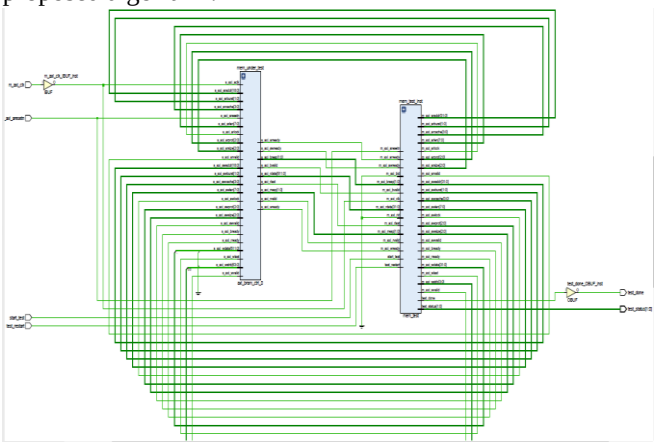


Figure 6 RTL Schematic

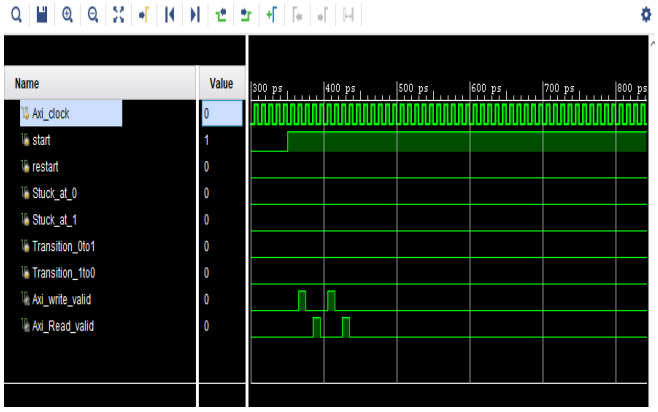


Figure 7: Parallel Write and Read

In figure 7, the Axi_write_valid signal represents the address valid signal for write instruction and Axi_Read_valid represents the address valid for read instruction. In earlier approach after completion of write instruction for all memory locations then only read instruction performs.

In this proposed method two clock pulses is required to enable the read instruction.

Figure 8: Serial Write and Read

In figure 8, the conventional memory BIST technique is used. The *'wea'* signal responsible for write and read instructions. In the conventional BIST technique, when *'wea'* signal becomes '1' the write operation is performed. When 'wea' signal becomes '0' the read operation is performed. In this results the write and read operations performed in serial manner.

Table 1: Comparative results

S. No.		[11]	[12]	[13]	Proposed BIST
1	LUT count	1050	1176	1366	965
2	Dynamic Power (w)	0.58	0.61	0.96	0.32
3	Number of clock cycles (per one instruction)	10	19	27	7

Table 1 shows the comparative results of the simulations carried out. The comparison is carried out with respect to LU count, Dynamic Power and number of clock cycles. The proposed technique consumes less number of LUTs and the Dynamic power is also reduced. The clock cycles required for the operation is reduced to 7.

IV. CONCLUSION

March C based algorithms are used for memory testing and fault detection in SoC devices. Different BIST modules need to be used to detect faults in different memories. As a result, design complexity increases. In order to overcome these above shortcomings, it is essential to develop advanced extensible Interface (AXI) with Block Random Access Memory (BRAM) and Design and Develop AXI based self-test memory architecture (March Algorithms) to achieve parallel read and write capability.

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Second Author profile which contains their education details, their publications, research work, membership, achievements, with photo that will be maximum 200-400 words.

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