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Execution of Median Filter Built on FPGA for Trimming Noise Meeting the Real Time Requirements

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Abstract—As images plays a vital in all aspects, there is a need to met the real time requirements in processing the image. Major challenges raised in processing the image is noise. The utmost typical difficult is effective denoising creation as well as quick functioning in the processing of digital image noise suppression process for the need of real time consequences to afford image with high quality this project was introduced. Generally filters plays a major role to remove the impulse noise in acquired images. The filter named sliding window spatial filter which is familiar as median filter is effective technique to eradicate impulse noise from the devoleped image. But in real time, it is very difficult to execute. To overcome this, FPGA methodology is introduced to fulfills the support besides the optimization of major constraints like area, speed, power. In addition to this, it assures technical sustenance of eradicating noise in image as per requirements in real time. Regarding the design and structure appearances in FPGA, Xilinx software is used for simulation and code has been written in Verilog language.

,Keywords-- FPGA, Median Filter, Image Processing, Verilog, Real Time Filtering, Impulse noise, Xilinx.

I. INTRODUCTION

Effective usage of images in most of the real time applications In an image organizing algorithms by concerning typical features to improve the image .[1].Primarily spatial domain and frequency which are two major domains used in digital image processing. There is exploit of pixels directly in spatial domain and frequency domain can be implemented by altering the Fourier transform.[2] A widespread technique which is used for trimming impulse noise is by applying non linear filters as non linear filters may fails to reduce impulse noise exhaustively. By comparing linear filters with non linear, digital accomplishment of nonlinear filters can be sluggish and immense .[3]. Sliding window spatial filter named as median filter which are categorized under nonlinear filters and has employs in spatial domain. Median filters were make known to industry by in the year of 1971 by Tukey [4]

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which has been implementing in numerous presentations in the field of image processing. Pointing at fixed value impulse noise for eradication from spoiled image, different filters are picked equivalent to pattern of noise existed in acquired image. By inspecting and evaluating on different types of algorithms which are discussed on various filtering techniques has been used formerly, limited literatures are employed.[5]. Here it is very complex to implement in hardware .To prevail over this, there is a need to change the way of implementing or change the algorithm used. For this FPGA technique is presented to minimize the complexity and optimizing parameters like area , power ,speed along with them it furnishes the real time requirements by eliminating impulse noise with furnished technical support.

II. MEDIAN FILTER

Filters are the operative tools to eradicate the noise. Filters afford an aid to visual clarification of images and can also be used as a precursor to further processing. Linear and nonlinear are the two types of filters in image processing. A non-linear filter is one that cannot be done with convolution or Fourier multiplication. Filters re-evaluate the value of every pixel in an image . For a particular pixel ,the new value is founded on pixel values in a local region a window centered on that pixel in order to reduce noise or augment edges. Filters may either be applied directly to recorded images or after transformation of pixel values.

Median filter is non linear filter which is also known as rank selection filter.[4] and sliding window spatial filter because as it works in spatial domain. To minimize the noise it endeavors value of spike of the noise by luminance of center pixel with median of that window. The mathematical expression of median filter is as follows.

S={s(i,j), where S is considered as filtering image.

$$S(i,j) = \text{median}\ (k, l)\ \epsilon\ W_{m,n}\{D(i+k, j+l)\}$$

Where $W_{m,n}$ is a sliding window of size m×n pixels centered at coordinates (i, j) and ns=m×n samples.

Sorting techniques such as bubble sort and quick sort has been using to sort out the pixels to organize the pixel samples in the order of upwards or downwards in algorithms which is used for sorting where n_s has high value. To obtain the N×N value of the median , the number of operations implemented in conventional algorithm is $3/8(n^4-1)$comparison.

The processing time and speed of the data is not good when the number of operations encompassed in FPGA. So the sorting technique , merged insertion sort is proposed which is faster then other sorting techniques. Minimization of comparisons can be achieved by using this sorting and also there is a chance to extend the number of comparisons. It reduces the complexity too.

III. ALGORITHM

A linear array LA having 'N' elements and 'K' is a positive integer. Such that K≤N, this algorithm in to the k^{th} positive in LA.
LA is linear array with 'N' elements and 'K' is a positive integer. Such that K≤N, this algorithm in to the k^{th} positive in LA.

1. [Initialize counter]set J=N

2. Repeat step 3 and 4 while J≥K.

3. [Move the J^{th} element downward] set LA [J+1]=LA[J].

4. [Decrease counter]set J=J-1

5. [Insert element]set LA[k]=ITEM

6. [Reset N] set N=N+1;

7. Exit.

IV. IMPLANTATION OF HARDWARE

To implement the system technically in hardware it must have filters for noise eradication like median filter, UART, PC, memory, control unit

A.FPGA

FPGAs, as illustrated in Figure given below consist of an array of programmable logic blocks of potentially dissimilar types, including general logic, memory and multiplier blocks, surrounded by a programmable routing fabric that allows blocks to be programmable interconnected. The array is surrounded by programmable input/output blocks, labeled I/O in the figure, that connect the chip to the outside world.

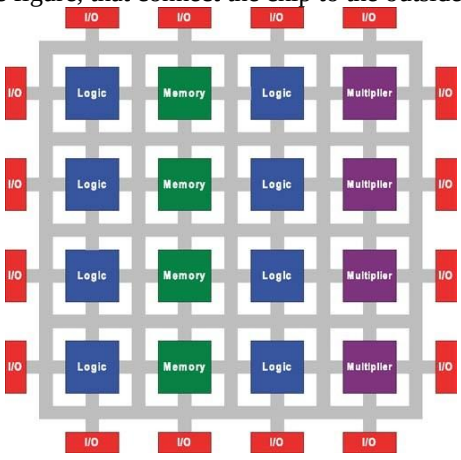

Fig:1 Basic structure of FPGA

B. MEMORY

The data of the image processed straightly, it may gets changed by pixel misplacement. This is because of the inequality time of writing and reading. A asynchronous FIFO is inserted amongst FPGA and FIFO for data buffering. To arrange the cached data, FIFO is taken to organize the structure of pipeline by ping pong operation. To attain the image data which consisting 8bit and sequential stream of display SDRAM is inserted which is having dual ports for reading and writing the operation. To accumulate the data of the image write port is used. By forming a skilled frame buffer with acceptable timing signal for VGA display read port is employed.

C. GENERATION OF MATRIX

In the module of the system, for simulating pipeline processing algorithm it is mandatory to swear the range of 25 pixels in the window to accomplish instantaneously. There is a need of 4 shift registers and 25 registers for designing hardware technically of 5×5 sampling window.

D. UART

The device which transforms the data parallel to serial is universal asynchronous transmitter receiver (UART). It transmits the data in the form of bytes successively a bit at a time from source but it receives the data in bytes at the end. It decodes the data which is sequential having control bit at the destination. In whole process it does not requires clock at the input. Therefore it labeled as asynchronous communication. The speed of the transmission can be calculated in the form of baud rate.

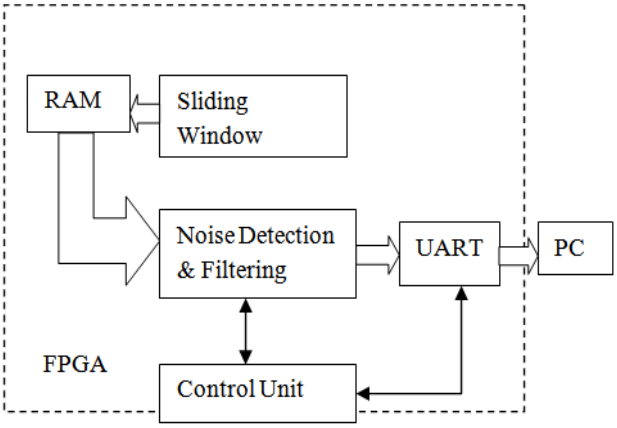

Fig.1. Hardware Architecture

E. CONTROL UNIT

To ensure better performance and ease implementation, there is a requirement of control unit , to regulate the data between source and destination for transforming.

V. SIMULATION RESULTS

Hence, in this project the impulse noise has been suppressed by using median filter which is implemented in hardware based on FPGA Spartan 3 Kit in the package of TQ400 with enriched accurate results.

Here also included the practical results of simulation by using ISE(VHDL/Verilog) and also enhanced images. In this project, Xilinx software is used and code has been written in Verilog language.

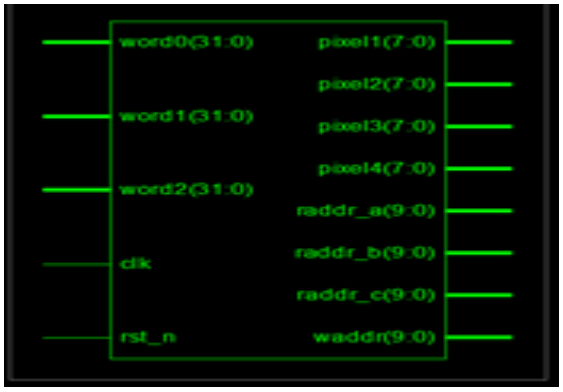

Fig.2. Median filter RTL schematic

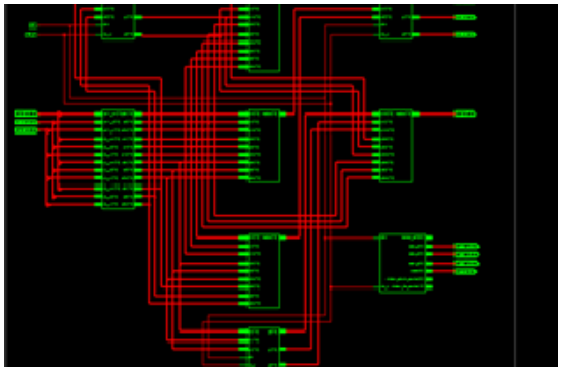

Fig.3.Interior outlook of filter

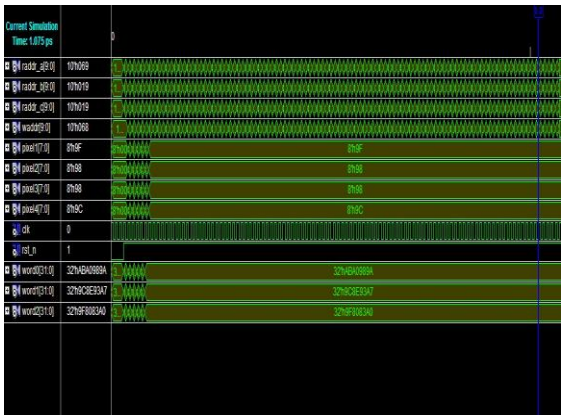

Fig.4. Test bench waveform o

Fig.6. Image with noise

Fig.7. Image with suppressed noise 1

Fig.7 Image with suppressed noise 2

Fig.9. Enhanced output image

VI. CONCLUSION

By analyzing the former experimental outcomes, concludes that this project has been diminishes the area and optimizes the constraints like power ,speed. It fulfills the hardware implementation technically and eradicates the noise to attain the real time requirements. By using novel sorting approach it minimizes time consumption and increases the processing speed. Performance has improved when compare to previous approaches and computational complexity has been reduced.

VII. FUTURE SCOPE

There are several approaches in future work like by implementing other filters to suppress noise in RGB images in advanced version of FPGA and by using SDRAM for memory for better way of optimization.

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