Design of 8T CNTFET SRAM for Ultra-Low Power Microelectronic Applications

K. Sarath Chandra, K. Hari Kishore, Pushpa Giri, E. Santhosh Reddy

Abstract*: At around 10nm, direct source to drain tunneling in COS-MOS technology constituting fundamental limitations that in turn hold back their suitability for modern electronic appliances chiefly as far as area, energy competency and performance. In advanced electronic appliances, memory constituents play a crucial part. Almost in every digital appliance, memory component is mostly preferred due to its unique potentiality to withhold information. Due to rapid technology advancements, architecture of SRAM is truly tested as far as delay, energy efficiency and stability. Traditional 6T memory unit experiences passage transistor conflict arises the contrast among read balance and write competence. The paper that proposed here contrasts the performance of distinctive CNTFET based 8T memory unit architectures like Traditional and Dual-Port with respect to write delay, read delay and power efficiency like static and dynamic. 8T SRAM bit cell is designed with 32nm CNTFET technology using HSPICE Tool. From the HSPICE simulation results, Dual-Port CNTFET SRAM has provide better read and write delays were reduced by ~8.8% and ~16.3%, static power and dynamic power by ~12.5% and ~42.2% respectively than conventional one.

Keywords*: Complementary-Symmetry Metal-Oxide Semiconductor (COS-MOS), Carbon Nanotube FET (CNTFET), Static RAM (SRAM), Six-Transistors (6T), Eight-Transistors (8T), Traditional and Dual-Port.

I. INTRODUCTION

As a result of advancements in VLSI manufacturing process, there will be invariably rise in the mode of chip integration. It has been brought about a consistently expanding exchange for bulkier on-chip information storage with enhanced stability, reliability and competency [1]. The portable silicon chip gadgets consist of integrated memory, which substitutes an extensive portion of the system-on-chip (SoC). The low-power highlight for on-chip SRAMs is getting increasingly significant, particularly for battery-dependent applications. These systems need lesser energy exceptional circuits put to use power handled device with an expanded period. The energy usage has its own priority to run down to increase the lifetime by adopting unorthodox appliance architectures, cutting-edge structures, and shape up the architecture [2].

Even though, potential scaling has gone before to circuit process in sublimit region with almost negligible energy usage, however performance issue is a major consideration. In the sublimit territory of circuit procedure prompts ultra-low power installed memories, chiefly static RAMs (SRAMs) [2], [3]. Regardless, in sublimit province, the input idea of Static-RAM cell is an unforgiving concern and degrades with the decrease of silicon-based transistors to sub-nanometer progression.

In recent times, semiconductor dependent field effect transistors (FETs) were examined as pervasive appliance component for silicon-based enterprises. At whatever point, the transistor size can be decreased to nanometer system, semiconductor FET's detaches to many complications like formidable energy competency in idle mode due to huge drop, gate loses his supremacy over tunnel, toughness in selecting best oxide material, incompetence to decrease oxide density respectively, and further more short tunnel effects (STEs).

Explicitly, under 10nm complementary-symmetry metal–oxide–semiconductor (COS-MOS) constitutes the voltage issue, i.e., reducing of KT/q and henceforth non-scalability of threshold voltage Vth and supply voltage Vdd. Also, at these specific innovation hubs, crystalline silicon separates into nebulous silicon wafers providing it to them to be utilized as a reasonable substance to manufacture advanced gadgets. Along with these, to make future electronic gadgets littler, more astute, and computationally productive, it has gotten critical to settle on substitute appliance substances or substitute application approaches. Fin Field Effect Transistor (FinFET), graphene Field Effect Transistor (GFET) [4-6], graphene nanoribbon Field Effect Transistor (GNRFET), carbon nanotube (CNT) [7,8] and Si-nanowire Field Effect Transistor are the substituent segments which have been completely well-considered as an imminent substitute for COS-MOS innovation. In this paper, CNT technology is used because of their utmost small unit area (about 2nm), extreme accomplishment in terms of speed, and energy competency.

Static-RAM (SRAM) is the major component in system-on-chip (SoC) deployed in computerized circuits and that possesses nearly 90-percent based on the chip cutting-edge area.

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With the innovation and at the same time supply voltage drop off, the design of SRAM is a tough task because of lesser noise and results in poor stability. In this way, along with nm scaled innovation, area, stability and energy efficiency are the three tough requirements that SRAM has to provide. In a similar fashion, decrease in transistor size results in memory size scaling cannot be reduced to extent when contrasted with other chip constituents. To think about using CNTFET for SRAM, in [11, 12] the writers have examined the contrast between CNTFET and COS-MOS memory cell. In [13], the novelists were analyzed various structures of CNTFET dependent SRAM, however haven't been inspected the impact of CNT imperfection in the memory execution. From [14], novelists thought that about the thickness impact deviations and metalloid cylinders effects the exhibition of Six-Transistors Static-RAM. Novelists were thought about graphene nanoribbon FET (GNRFET) occupied memory and semiconductor FET occupied memory and also indicated the energy utilization of GNRFET with semiconductor occupied Static-RAM, in [15]. The writers were presented the impact of metalloid Carbon Nanotube on write and read delays. At any rate CNTs can totally dismisses the impact of energy and noise margin in both read and write activities. So also, the novelists promoted the advanced metalloid based 6T CNTFET for an ultra-low energy structure. At any rate noise margin, delay, and furthermore the impact of diameter in consideration of alternate conceivable memory structures hadn't been analyzed. Along these, the investigation of CNTFET occupied 8T memory for different designs like traditional and Dual-Port cells with some innovative deadlocks are observed while fabricating of CNTFET, for example, metalloid CNTFETs, difference in doping-level, deviation in tube breadth, and deviation in thickness of cylinders. In this paper prefers the impact of all these contradistinctions mainly for parameters like read- write delays, and energy competencies like static and dynamic.

The rest of the paper is systematized to such an extent that, the conventional data concerning CNTFET innovation is illustrated in Section II. Modified 8T CNTFET Static-RAM memory structures like conventional and Dual-Port are discussed in Section III. In Section IV and Section V, simulation outcomes and Comparisons were conferred it. In Section VI, the journal paper is done up finally with concluded.

II. CNTFET TECHNOLOGY

Carbon nanotubes are consecrate smoothly continuous circular solids bring into existence by circumrotary graphite foil as shown in figure1. Based on the circumrotary motif of the graphite foil, CNTs interprets the Pair of metalloid and semiconducting properties. In like manner, it is possible to construct all CNT subordinate electronic contraptions utilizing metalloid CNTs as a joining curl and semiconducting CNTs as a FET.

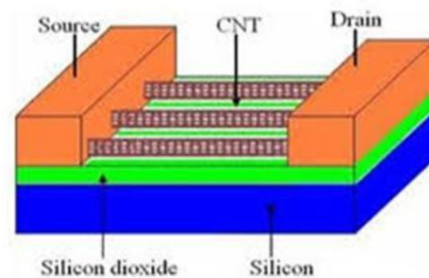

Fig. 1. CNTFET Structure.

1-D structure of CNT is the liberal fundamental perspective and the substance of solid quantum hypothesis of electron and gap state in only 1-D part of a band. Thus, the dynamism increases by decaying the rearmost scattering (i.e., tremendous current holding limits even at low supply voltage) and better direction over FET in off-area (and consequently low spillage current). It has capable to use ballistic advancement (i.e., the normal rail is broad than the rail) which decreases transporter charge assault and recommends endless impedance. Likewise, the speed of a FET will be in the scope of THz (Terahertz). Extreme-comparability, strength, smaller imperativeness competency, and STE are some of the distinctive characteristics exhibited by the CNTFET technology at below 10nm. In this way, the properties of CNTFET make it one of the strong probabilities for present day equipment.

III. 8T CNTFET SRAM CELLS

So as to enhance the functioning of the Static-RAM, a couple of Eight-Transistors Static-RAM cells are presented here. Figure 2 exhibits customary 8T CNTFET Static-RAM [9]. It incorporates a standard 6T SRAM cell as within it. Bit line (BLb) and control signal (Read) are utilized to cell isolation from the output by using two extra n-type transistors. The write activity of Static-RAM can be finished by using bit lines BL and BLb by means of access path transistors (M1 and M4). The read activity is fulfilled by means of R1 and R2 and the information that put away shows up on the read bit line BLb. M4 and M1 are made more strengthened than P1 and P2 for effective write activity.

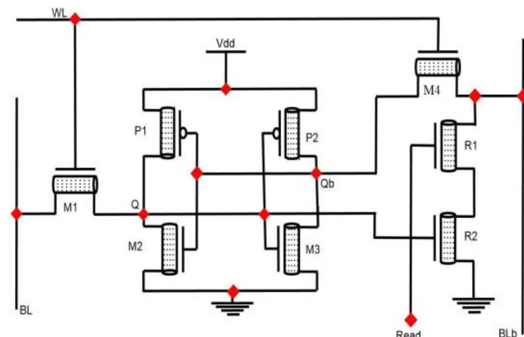

Fig. 2. Conventional 8T CNTFET SRAM Structure

Read activity of the cell begins with pre-charging the bit lines. From that point onward, reading is begun by setting Read signal to HIGH. Whenever bit one is put away to the cell, Q is at Vdd and Qb is at GND. While read activity, pre-charged bit line (BLb) begins to release through R2 and R1. Releasing stage ought to be quick enough contrasted with the rate that bit line (BLb) spills through all the access ones, Static-RAM cells associated with it. Along these lines, the write circuit can distinguish the information effectively. Whenever bit zero is put away in the cell, bit line (BLb) ought not release, and at any rate it remains at or close to Vdd. For this situation, the write circuit ought to identify the value of bit line (BLb) before spillage makes it drop excessively.

The write activity begins with pre-charging of bit lines both BL & BLb. After that writing is started by setting WL to HIGH. Whenever bit one is to write in the cell, bit line (BL) ought to be one and bit line (BLb) ought to be zero. Such that transistors M1 & M4 are ON. Then Q charges to one and Qb to zero. Similarly bit zero can be written into the cell by making bit line (BL) to zero and bit line (BLb) to one.

The Suggested Eight-transistors Static-RAM unit is appeared in Figure 2, which experiences the problem of read disturbance. The value of read bit line (BLb) relies on Qb esteem such that when Qb esteem alters the whole condition of the cell alters because of this the reading activity is got disturbed, in essential 8T SRAM. To overcome this in Static-RAM, a modified Eight-Transistors Static-RAM unit has been created as appeared in Figure 3.

SRAM cell with Dual-Port has structure contemplations are significant for various reasons. Initially, the design of a Dual-Port SRAM cell has ability to give steady and powerful SRAM activity. Also, to increase On-chip memory storage due to continuous changes in the technology advancements, SRAM designers were mostly concentrated on thickness of the transistor. In this way, a SRAM cell should be as small as could be expected under the circumstances while meeting the steadiness, speed, potentiality and demand imperatives. Dual-Port Static-RAM unit is the segment to reserve binary data. Both read and write abilities are provided by the cell. Functional activities are characterized by the word line.

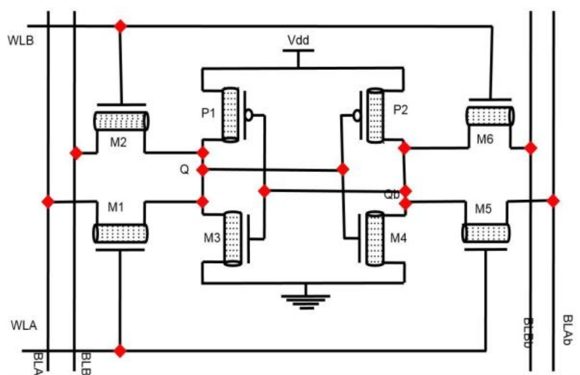

Fig. 3. Dual-Port 8T CNTFET SRAM Structure.

Similarly, likewise fundamental 8T SRAM cell, Dual-Port one can be written using either WLA &WLB and can be read from the cell. Here we can write data into the cell with word line WLA and read data from the cell with word line WLB and vice versa.

Usage in Embedded systems: Numerous classes of mechanical and logical subsystems, car hardware, and comparable, contain static RAM.

Usage in PCs: For rapidly performing activities, the speed and effectiveness of Static RAM make it perfect for CPU reserve. Balancing of cost and area for Static-RAM are generally done by the little amounts of usage in present day PCs.

IV. SIMULATION RESULTS

Illustration of simulations and results of Static-RAM cell structures using 32nm CNTFET technology using HSPICE Tool are presented here.

Fig. 4. Writing information into 8T traditional CNTFET Static-RAM Structure.

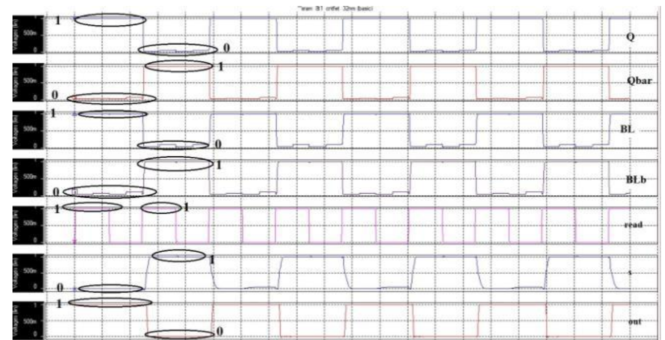

Fig. 5. Reading data from conventional 8T CNTFET SRAM Cell Structure.

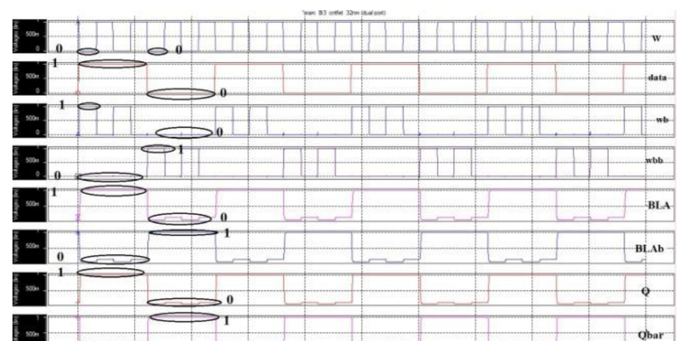

Fig. 6. Writing data into Dual-Port 8T CNTFET SRAM Cell Structure using bit lines (BLA & BLAb).

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Fig. 7. Reading data from Dual-Port 8T CNTFET SRAM Cell Structure using bit lines (BLA & BLAb).

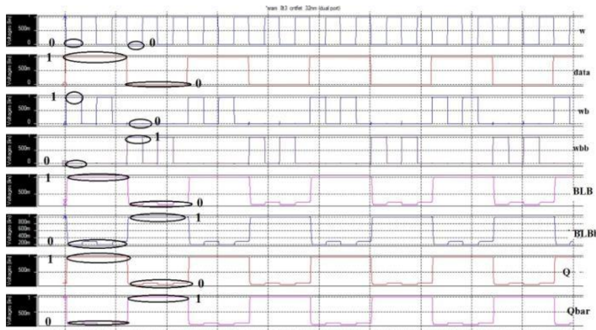

Fig. 8. Writing data into Dual-Port 8T CNTFET SRAM Cell Structure using bit lines (BLB & BLBb).

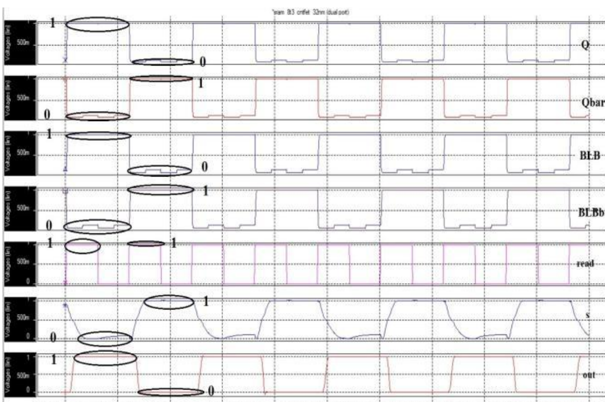

Fig. 9. Reading data from Dual-Port 8T CNTFET SRAM Cell Structure using bit lines (BLB & BLBb).

V. COMPARISON SUMMARY

Therefore, distinctive 8T memory cells are designed utilizing 32 nm CNTFET Technology at a supply voltage of 0.9 V using HSPICE Tool. Read-Write delays, static and dynamic powers are major performance metrics for analyzing SRAM cell stability. Because of assistance of the independent write and read word lines, the Fundamental Eight-Transistors SRAM shows an unintended difference in put away condition that is overwhelmed by the Dual-Port one. From the Fundamental 8T SRAM, it has observed that a write delay time of 9.1ns and read disturbance of 12.9ns respectively. While in case of dual-port 8.3ns of write delay and 10.8ns of read disturbance are observed. The static and dynamic power consumption of conventional 8T and Dual-Port 8T cells is found to be 0.008pW and 0.007pW, 38pW and 22pW individually. It tends to be seen that there is a negligible variance in static however medium in dynamic power utilization esteems and henceforth, the operational advantage is the prime factor. HSPICE simulation results states that dual- port CNTFET SRAM has provide better read and write delays were reduced by 8.8% and 16.3%, static power and dynamic power by 12.5% and 42.2% respectively than conventional CNTFET SRAM. The comparison of the 8T SRAM memory structures are classified in TABLE I.

TABLE I
COMPARATIVE ANALYSIS OF 8T CNTFET MEMORY CELL STRUCTURES

8T CNTFET Structure	Write delay (ns)	Read delay (ns)	Static power (pW)	Dynamic power (pW)
Conventional	9.1	12.9	0.008	38
Dual-port	8.3	10.8	0.007	22

VI. CONCLUSION

From the HSPICE Simulations, we know that the 8T Dual-Port CNTFET memory cell has decreased read disturbance, increased data stability and better control over the cell. In addition of extra transistors in traditional architecture, enhances the read and write mechanisms of the cell. Moreover, of additional FETs shapes the region of the suggested 8T SRAM practically Dual-Port with its functional capacity and smaller delay provides it exceptionally appropriate for extreme use than that of Fundamental 8T SRAM. Design in most of the battery-operated system-on-chip (SoC) is dependent on memories like Static-RAMs because of its low energy utilization. Performance and structure are a major concern in developing array of memory. Use of this cell can discover mostly in low or ultra-low voltage and average recurrence activities like neuroscience machines, sub limit computing and low power cache memories.

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