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Design and Selection of Power Circuit and Control Parameters for DSTATCOM

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Abstract*: This paper presents the proper design and selection of power circuit and control parameters of VSI based DSTATCOM for compensation of reactive power in a radial distribution systems, feeding power to crucial loads of an industrial, commercial and residential systems. The study of radial distribution system is analyzed in terms of electrical power system of institute, power consumption pattern and tariff related issues. Some conclusions were made to improve the system performance in terms of power factor and reduction in tariff. The DSTATCOM performance depends on the calculation of the reference source currents that generate the gating pulses of the VSI.

Keywords : DSTATCOM, Hall Sensors, Point of Common Coupling, Pre-Charge Circuit, 3S-2P.

I. INTRODUCTION

In today's scenario, to maintain good power quality in a power system is very important, and thus it is very essential to design appropriate compensators. The quality of the power is poor due to the increase in a wide variety of loads that pollute the power system. Improper design results in compensators with either over-capacity or under-capacity. Under-capacity leads to interruption of operation while over-capacity increases the cost. Hence, each component is to be designed very carefully. For better quality of power the general method of designing a DSTATCOM is described elaborately. Proper control and functioning of any system requires a correct or accurate design and analysis is an essential component. Specially for reactive power supervision in a power distribution system of a power utility or industry plays a key role in i) reducing distribution loss, ii) maintaining constant distribution voltage and iii) improving power factor. The perfection of power factor enables the reduction of current demand from the utility resulting in efficient utilization of distribution transformer and reduced electricity bills. The performance of conventional switched capacitors used for reactive power compensation would only give step control and results in over compensation or under compensation for varying loads and changeable reactive power demand. To overcome these problems, it is proposed to develop a prototype 30 kVAr DSTATCOM for reactive power compensation which would provide instantaneous correction of power factor and always maintains the set power factor. The prototype consists of a power panel with IGBT based voltage source inverter, DC filter capacitor [1] and a DSP based controller along with necessary power supply units, protection cards and firing pulse generating units. By suitable control strategy [2-3], the STATCOM would generate leading or lagging reactive volt-amp (VAR) at the PCC (Point of Common Coupling) and avoid problems connected with lag and lead power factor. The power factor can be maintained at the desired level irrespective of system voltage [4-6].

A. Objective

The main objective of this design is

a) To Design, simulate and fabricate a ±30 kVAr prototype DSTATCOM

b) To develop control hardware and software for reactive power compensation

c) To evolve novel testing strategies

B. Project significance

DSTATCOM is an acronym for Distribution STATic synchronous COMpensator, and forms a member of the family, widely known as FACTS (Flexible AC Transmission System) or Custom Power devices.

Development of DSTATCOM and knowledge of practical aspects of advanced power electronics enables the research centre in Electrical Engineering Department (EED) to be a unique one with in-house capability to design and develop a FACTS device. The idea of combining capabilities of IGBT-based voltage source converter, DSP based controller and allied power electronics as proposed in the project ushers in an original generation of FACTS controllers. The present development would open up a path for further studies in the region of other FACTS or custom power devices. The know-how gained in the present development will result in tools and techniques for design of other FACTS devices such as, high power STATCOM, Static Synchronous Series Compensator (SSSC), Interline Power Flow Controller (IPFC) and Unified Power Flow Controller (UPFC), Dynamic Voltage Restorer (DVR), active power harmonic filter, active power line conditioner etc. The basic building control block diagram of DSTATCOM shown in Fig. 1. The complete electrical substation layout of Sultan Ul-Uloom Education Society is shown in Fig. 2. The incoming supply is 11 kV/440 V is divided in to two parallel feeders; one feeder is connected to 500 kVA transformer and the other feeder is connected to 250 kVA transformer.

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The output power of these two transformers feeding to different loads in the society. In this system, to control reactive power it is connected to two automatic capacitor panels, one capacitor bank of 150 kVAr to feeder 1 and the other capacitor bank of 125 kVAr to feeder 2. To compensate no load reactive power of transformers, a fixed capacitor of 25 kVAr is directly connected to 500 kVA transformer and 15 kVAr to 250 kVA transformer at their secondary terminals.

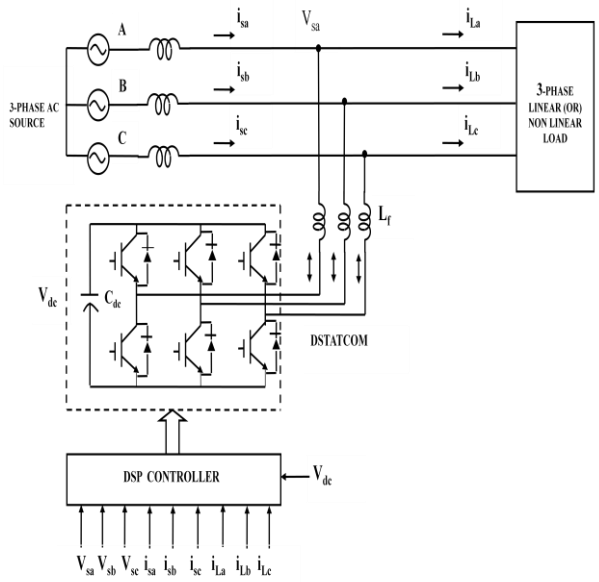

Fig. 1.Basic Building Control Block Diagram Of DSTATCOM.

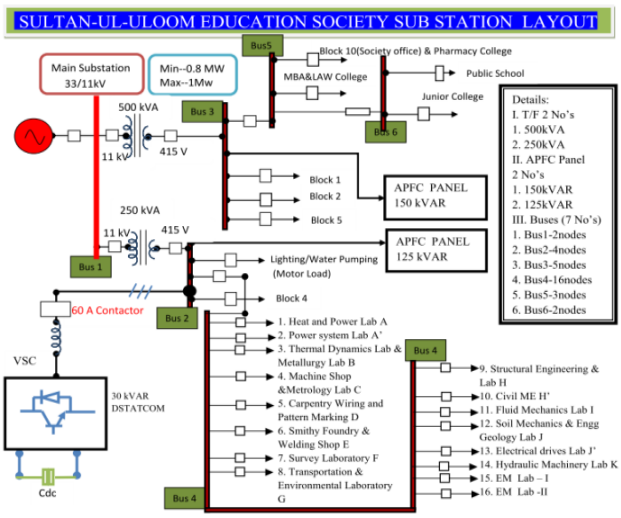

Fig. 2.Power Distribution of Sultan Ul- Uloom Educational Society.

II. PROBLEM FORMULATION

A Distribution STATCOM (DSTATCOM) is a shunt compensation device used for reactive power compensation. It can be used either in the power factor correction mode or in the voltage regulation mode. The major problem associated with the design of the controller for the DSTATCOM is the selection of appropriate circuit components. The second major problem is to understand the proper working of the controller and control algorithms. It is necessary to understand the design of hardware components and the controller so that the DSTATCOM is effectively used for power quality improvement applications.

III. DESIGN PARAMETERS OF DSTATCOM

The Design parameters are considered based on the design of 30 kVAr DSTATCOM. It consists design of the choke (interphase inductor), voltage rating, selection of DC link capacitor, equalizing resistances, pre-charging circuit parameters, realization of Phased Lock Loops (PLL), power supply modules, DC filter capacitor bank module [7-8], signal conditioning cards, protection cards, IGBT power modules, processor and their interlocks [4].

A. *Design of DSTATCOM*

It is a shunt connected flexible AC transmission system (FACTS) controller used for improving the power quality in the distribution level or at the medium voltage level. Fig. 3. shows a DSTATCOM configuration which consists of a Voltage Source Converter (VSC) or an inverter, a DC-link capacitor and a coupling inductor. The design of the DSTATCOM means the selection of appropriate values of coupling inductor or choke, determining the capacitor value and its operating voltage level and selecting the appropriate operating voltage and current ratings for the power electronic switches. In general, for medium voltage applications, Insulated Gate Bipolar Junction Transistors (IGBTs) are used as power electronic switches.

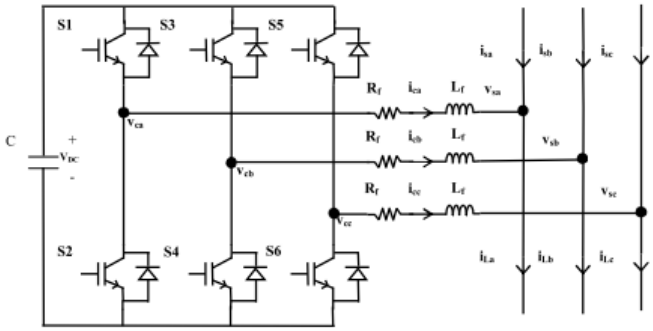

Fig. 3.Dstatcom Configuration

B. *Design of the Choke*

Let us consider a three-phase system with a line voltage V_{LL} of 415 V. The design procedure is explained with respect to a 30 kVAr DSTATCOM connected in shunt with the power system through a coupling inductor. Thus the rated rms line current is given as in equation (1).

$$Rated\ RMS\ line\ current = \frac{kVAr \times 10^3}{\sqrt{3} \times V_{LL}} = 42\,A \qquad (1)$$

Peak value of the line current Ip = 42×1.414= 59.39 A
Assuming the ripple current ΔI through the choke to be 20 % of the rated peak current so, ΔI = Ip × 0.2 = 60 × 0.2 = 12A, Impedance per phase is calculated as $Z_{ph} = V_{ph}/I_{ph}$ = 5.7142 Ω. Generally we will consider either 15% Impedance or 20% Impedance for 15% impedance = 5.7142*0.15=0.8571Ω and for 20% impedance = 5.7142*0.2=1.1428Ω.

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Coupling inductor value for 15% Impedance = 2. 7296 mH, Coupling inductor value for 20% Impedance=3.6395 mH. Hence, a 3.6395 mH, of 42 A choke can be used for this application with a tap of 2.7296 mH and it is shown in Fig. 4.

However, this choke has to filter out currents containing the switching frequency components. Hence, the core losses in the choke will be more than that when it is used to pass the fundamental component of the current. While constructing the choke, this factor should also be taken into consideration. In addition, the core should not be saturated at peak values of current due to the harmonics. In addition, it is necessary to provide enough ventilation between the conductor and the core of the choke.

Fig. 4.Reactors Of 30 Kvar DSTATCOM

The coupling reactors connect the voltage source converter to the mains. The design of coupling reactor depends on several factors described in this section. The current flowing into the ac supply and its waveform depend on the link inductance. This link or coupling inductance can be provided by the leakage reactance of the coupling transformer and, if necessary, through an additional reactor placed in series with the transformer winding. This coupling reactance helps in limiting harmonic currents as well as fault current into the DSTATCOM. It also helps in softening the transient current response from the DSTATCOM when there is fault on the supply system which collapses the voltage, or when there is a large magnitude of dynamic over voltage. The selection of the coupling reactor should take into accent the above factors.

C. *Design of capacitors*

The DC-bus capacitor for a DSTATCOM is selected based on the following maximum ratings.

- The working voltage of the capacitor, which specifies the maximum DC voltage that the capacitor can withstand for a sustained period.
- Ripple current of the capacitor, which specifies the maximum AC current that can flow through the capacitor without exceeding its internal temperature.

1) Voltage rating

The voltage rating of the DC capacitor is obtained from the maximum DC-bus voltage that the capacitor can withstand for a sustained period. The maximum DC-bus voltage depends on the grid voltage, the voltage drop across the series inductor and the type of PWM strategy employed in the VSC. If the sine PWM (SPWM) technique is employed for switching the IGBTs equation (2) gives the line-to-line RMS voltage $V_{LL}(RMS)$ obtained at the output of the VSC.

$$V_{LL}(RMS) = 0.707 \times m \times V_{dc} \quad (2)$$

where, m ($0 \leq m \leq 1$) is the modulation index and V_{dc} is the DC bus voltage. Taking the series choke voltage drop as 10% of the grid voltage, as considered in the case of choke design.

Series Choke drop = $0.1 \times 415 = 41.5 \cong 42\ V$

the minimum line-line RMS voltage required at the VSC output V_{LL} min is the sum of the grid voltage (Vg) and voltage drop across the choke and is given by

$V_{LL} = V_g$ + Series choke drop = 415+42 = 457 V, according to equation (2), the DC bus voltage required to produce this line to line rms voltage at the VSC output at the maximum modulation index (m=0.8), is given by

V_{DC} = 457/0.707 = 650V

However, in the practical case, the grid voltage attainable will be lesser than the estimated one due to the dead-band and the transition times of the switching device. In addition, as per the grid-code specifications, the grid voltage can have a maximum value of 457 V (415 V+10%). Considering all these factors, the operating voltage of the DC bus is chosen to be more than 850 V. By taking the margin of safety into consideration, the voltage rating of the DC bus is selected as 900 V [9]. However, the commonly available capacitors have a maximum rating of 500 V. Hence, two identical capacitors of voltage rating 500 V are connected in series.

2) Selection of DC Link Capacitor

The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. Let us assume that the compensator is connected to a system with the rating of X kilovolt amperes. The energy of the system is given by X×100 J/s. Let us further assume that the compensator deals with half (i.e., X/2) and twice (i.e., 2X) capacity under the transient conditions for cycles with the system voltage period of T (sec.). Then, the change in energy to be dealt with by the dc capacitor is given in equation (3).

$$\Delta E = \left(2X - \frac{X}{2}\right) nT \quad (3)$$

Now this change in energy should be supported by the energy stored in the dc capacitor. Let us allow the dc capacitor to change its total dc-link voltage from $1.4V_m$ to $1.8V_m$ during the transient conditions where V_m is the peak value of phase voltage. Hence, the stored energy in a capacitor E can be written as

$$\text{The energy stored in a capacitor} = \frac{1}{2} C V^2$$

$$\frac{1}{2} C_{Dc}[(1.8V_m)^2 - (1.4V_m)^2] = \Delta E$$

$$\frac{1}{2} C_{Dc}[(1.8V_m)^2 - (1.4V_m)^2] = (2X - \frac{X}{2}) nT$$

This implies that

$$C_{Dc} = \frac{3XnT}{[(1.8V_m)^2 - (1.4V_m)^2]} \quad (4)$$

For example, consider a 30-kVA system (i.e., X = 30 kVA), system peak voltage V_m = 340V, n = 0.4, and T = 0.02 s. The value of C_{Dc} computed using equation (4) is 4622 µF Practically, 4700µF is readily available and the same value has been taken for simulation and experimental studies.

3) Design of the Equalizing Resistances

When electrolytic capacitors are connected in series, their voltage distribution may not be uniform due to the differences in the dielectric insulation resistance of the individual capacitors. This may cause the voltage of the individual capacitors to exceed the maximum permissible voltage rating, which is quite undesirable. Forced balancing of the voltage distribution can be achieved by connecting balancing resistors across the individual capacitors.

As a rule of thumb, the balancing resistance values are chosen such that approximately 10 times the leakage current of the capacitor flows through the resistors. In other words, the selected resistance value should be substantially lower than the leakage resistance of the capacitor. Equation (5) gives the expression for estimating the equalizing resistance.

$$R = 100M\Omega * 1\mu F * (1/C_{Dc}) \quad (5)$$

Since the capacitance value selected is 4700 µF, the practical value of the equalizing resistor is 22 kΩ.

The power loss in the balancing resistance, assuming a working voltage of 425 V, is given by

$$P = \frac{V^2}{R} = \frac{415 \times 415}{22\,k\Omega} = 7.8\ W$$

Hence, 22 kΩ , 8 W resistors are chosen as balancing resistors in the capacitor bank.

The capacitor bank was fabricated using ALCON make electrolytic capacitor of rating 4700 uF/ 450 V [10]. To achieve the required capacitance and voltage rating, three capacitors are connected in series and two such parallel combinations (3S-2P) The capacitor bank is divided into single modules and connected to one numbers of IGBT phase modules. The connection diagram of capacitor is as shown in Fig. 5

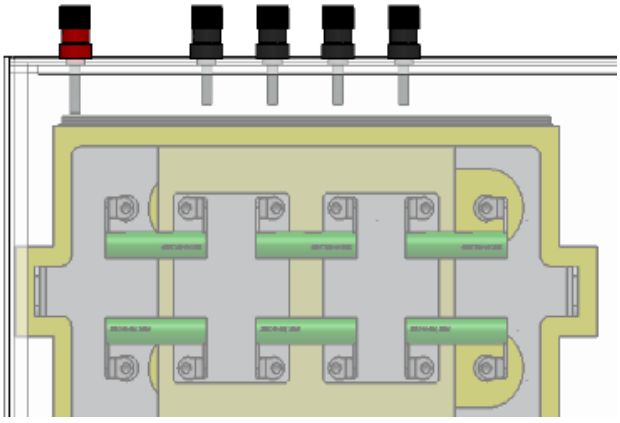

Fig. 5.Capacitor Bank Connections In An Inverter Stack

D. *Pre -charging circuit*

The pre charging circuit resistor value, current value and resistor wattage calculations are given below. DC link capacitor voltage (V_{dc}) = 594.2 V ~= 595 V. Normally D.C. link capacitor charge to a full value of 90%. i.e., C_{Dc} = 0.9*595=535.5~= 536 V. Each resistor wattage is 10 W; each resistor current is 2.27 A; each resistor value is 200 Ω [10-12]. Without and with delay of pre-charging [4] simulation wave forms are as shown in Fig. 6 & Fig. 7.

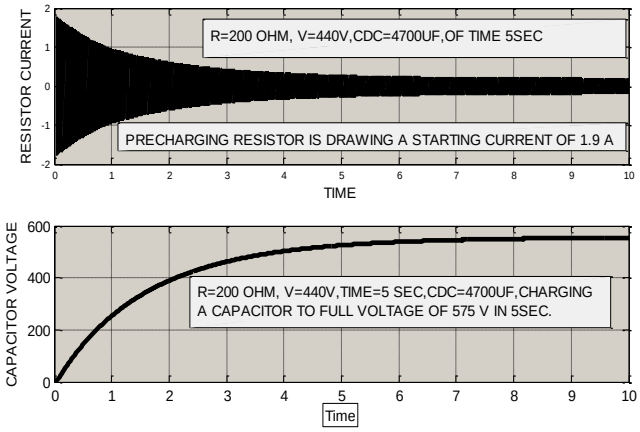

Fig. 6.Charging Of Capacitor With Out Delay.

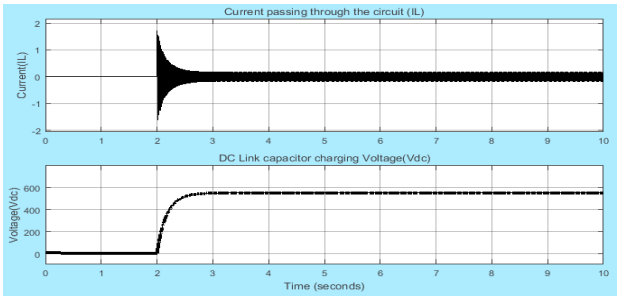

Fig. 7.Charging Of Capacitor With A Delay Of 2 Sec.

The hardware model of pre-charge circuit as shown in Fig. 8. It consists of 220 Ω , 10 W three resistors in each phase and a pre-charge contactor of 9 A capacity. When the operation starts first the main contactor (63 A) is in bypass mode, pre-charge contactor of 9 A is in supply.

When inverter stack dc link capacitor is fully charged it bypasses the contactor form pre-charge (9 A) to main contactor (63 A), the main switch will be ON continuously. Only the action will be taken in between pre-charge and main contactor. If any problem occurs in the control, the DSP timer will give trip signal to main contactor, so the entire system will be in OFF state.

Fig. 8.Hardware model of pre-charge circuit.

E. *Hardware implementation of Signal conditioning circuit*

The block diagram of the fabricated signal-processing unit or signal conditioning circuit is shown in Fig. 9, which consists of the quad low power JFET input operational amplifier (LF444) based signal conditioning circuit and the sensor circuits that are designed and fabricated in a PCB. The voltage source type of signal condition card is simulated in Matlab/Simulink is shown in Fig. 10. Fig. 11 shows the current source type of signal condition card and the simulated results of voltage and current source type are shown in Fig. 12 & Fig. 13. The same circuit is fabricated and tested using 3-Φ input signals with the function generator and then used in the 30 kVAr DSTATCOM hardware prototype implementation. The above design is based on the Texas instrument design using op-amps [11].

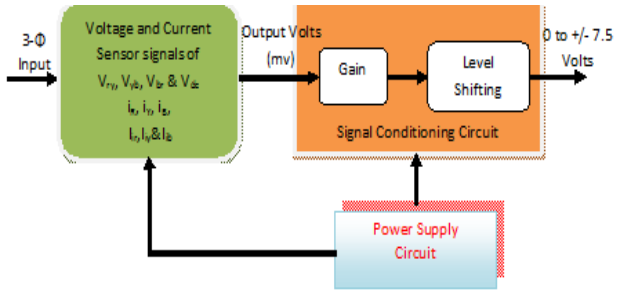

Fig. 9.Block Diagram Of The Signal Processing Unit

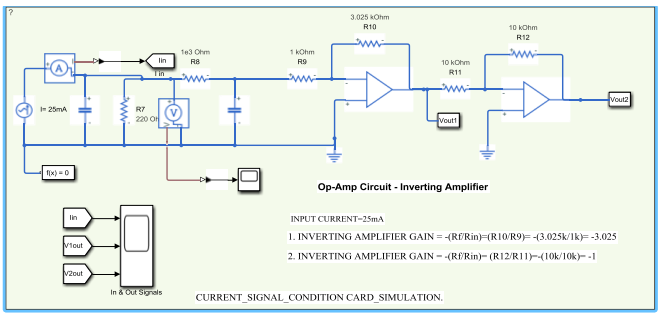

Fig. 10. Matlab Simulation model of the current signal conditioning card

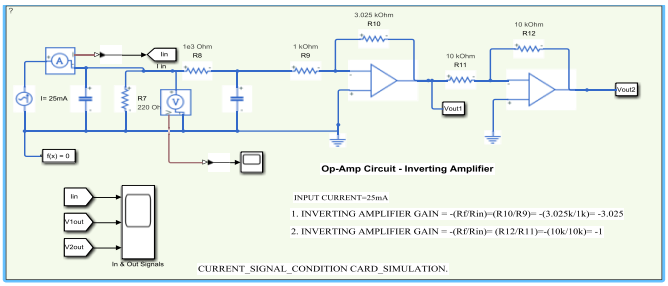

Fig. 11. Matlab Simulation Model Of The Current Signal Conditioning Card

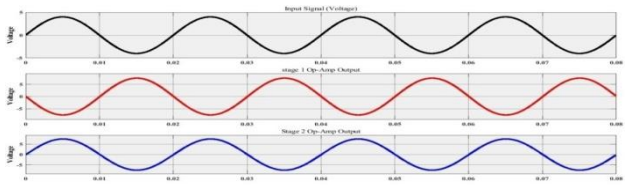

Fig. 12. Matlab Simulation output of the voltage signal conditioning card

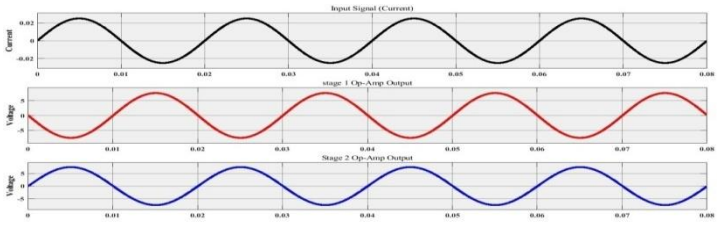

Fig. 13. Matlab Simulation output of the current signal conditioning card

F. *Protection Logic*

The following protections are provided for the DSTATCOM system.

- Over voltage / Under voltage at converter AC terminals
- Over voltage / Under voltage at converter DC terminals
- Over current at converter AC terminals
- Shoot-through protection
- Power supply under voltage
- V_{CEC}(sat.) Function (Back up for shoot-through)

In case of any fault, the trip sequence is initiated for opening the main contactor and charging contactor.

IV. DETAILS OF CONTROL CIRCUIT HARDWARE

The control panel consists of DSP (digital signal processor) boards, PC (Personal computer), power supply units, signal conditioning cards, protection cards and firing pulse generation card. This table top setup consists of all the hardware required for controlling the PWM converter, operating sequence and protection functions shown in Fig. 14. How DSTATCOM control system interfaces with its power circuit and substation PCC equipment.

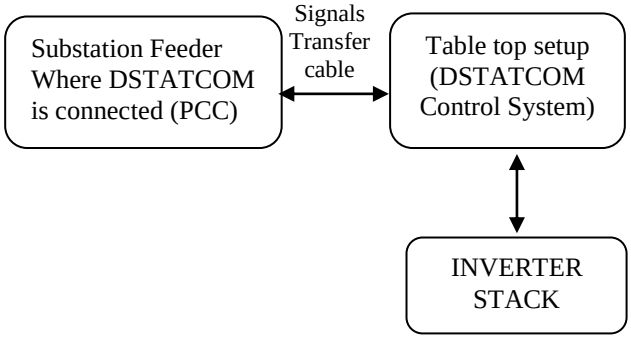

Fig. 14. Interface of DSTATCOM Power and Control Hardware with PCC Equipment.

A. *Description of Control Circuit*

The DSTATCOM can be used for radial distribution systems and industrial application. The present project envisages reactive power compensation in an educational institution of radial distribution network. Fixed or switched capacitor banks are normally used in industries or in distribution utilities to maintain power-factor to near unity. The reactive power demand depends on the magnitude and type of load. Hence, to maintain power-factor near to unity, the capacitor banks have to be manually or automatically switched through circuit breakers or thyristor switches.

Thus, step-less control of reactive power compensation is not possible with fixed or switched capacitor banks. Thyristor control reactor in conjunction with capacitor bank can be used for step-less control of reactive power drawn from the source. The reactive power compensation with such scheme involves phase angle control and thus, generates a lot of unwanted harmonics. The DSTATCOM can be used to avoid problems associated with fixed or switched capacitor bank or conventional SVC based reactive power compensators. The present DSTATCOM project envisages maintenance of near unity power-factor at the incoming substation. Hence, the incoming three-phase voltages and currents are monitored and PWM switching pattern for the converter is generated such that the reactive power drawn through the incoming feeder is almost zero.

For complete design of power circuit and control parameters for DSTATCOM researchers can use this link [12]. The input data required for design of DSTATCOM is shown in Table I and their corresponding parameters values are shown in Table II

TABLE I. DSTATCOM DESIGN INPUT DATA

Parameters	Corresponding values
Preliminary data required for design	
Rating of DSTATCOM in kVA	30 kVA
System rms line voltage (V_{LL})	415 V
Modulation index (m) 0<=m<=1	0.8
Switching frequency (fsw) in kHZ	2.5 kHz
Ripple current (Iripple)	0.85
System operating frequency in HZ	50 Hz
Capacitor charging time in seconds	20 seconds

TABLE II. POWER CIRCUIT DESIGN PARAMETERS OF DSTATCOM

Parameters	Design values*
Main line current	42 A
Precharging contactor rating	2.196 A
Main contactor rating	59 A
Precharging resistor values	680 Ω
Precharging resistor wattage	8 W
Precharging steady state voltage	504.41 V
Precharging time to steady state voltage	20 seconds
DC link capacitor value	4.90e-3 uf
DC link voltage/ bus voltage	808 V
Inverter currents maximum	63 A
Main cable size	25 sq mm
Rating of coupling reactor/ inductor value 15%	2.73 mH
Rating of coupling reactor/ inductor value 20%	3.63 mH

* Rating of the devices can be choose next higher available values in the market

V. CONCLUSION

The Design and selection of power circuit and control parameters for DSTATCOM are analyzed in terms of their performance and quantity level. Some of the components are simulated in Matlab/ Simulink environment and for the satisfactory results, the obtained power circuit parameter values are embedded in this paper, the equivalent components are used for 30 kVAr DSTATCOM for controlling of reactive power compensation in an 800 kW radial distribution system of an educational institute. The results that are achieved are satisfactory in terms of their performance and quantity.

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