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Design of Low Power Memory Architecture using 10t Sram Array

M. Madhumalini, B. Saranraj

Abstract *:**The main aim of electronics is to design low power devices due to the prevalent usage of powered gadget. Ultra low voltage operation of memory cells has become a subject of a lot of interest because of its applications in terribly low energy computing. The stable operation of static random access memory (SRAM) is important for the success of low voltage SRAM and it is achieved by parameter variations of scaled technologies. The power consumption and access time of the SRAM is also a complex parameter due to the unavoidable switching activities of the number of transistors used for different blocks like, SRAM cell, access transistors, pre-charge circuit, sense amplifier and decoders. It has been shown that conventional 6T SRAM fail to achieve low power and delay operation. The proposed 10T SRAM design gives an approach towards the hold power dissipation. The designed circuit has 10 transistors out of that 2 transistors are used as sleep transistor. The sleep transistors are used as switches. Such as header and footer switches and the switches are turned on during active mode of operations and turned off during idle or standby mode of operations. The designed SRAM cell also has conducting pMOS circuit, which can reduces the total power dissipation. The SRAM cell is simulated by using Cadence tool. A supply voltage of 1.8V is used which makes it enough for low power applications. The power obtained as 761.7mW, which reduces 15% of conventional 6T SRAM design. The delay obtained as 125.6ns, which reduces 45% of conventional 6T SRAM.***

Keywords *: **SRAM, Conducting pmos, Sleep Transistor, decoder, pre-charge ,sense amplifier.***

I. INTRODUCTION

Memories are the most important block of electronic components. Memories are classified into two types i) Random Access Memory(RAM) and ii) Read Only Memory(ROM). Read only memory is a simple transistor memory, which stores data under no power situation too with structure of transistors. Random access memory is entirely different from Read only memory. RAM is further classified into two types i) Static Random Access Memory(SRAM) ii) Dynamic Random Access Memory(DRAM). Dynamic RAM uses capacitor to store data, charge stored in capacitor can hold up to a small period of time after that it starts discharging [2,21]. After a particular time period the voltage value become less than the threshold value of the transistor. So, DRAM needs refreshing circuit, which periodically refreshes the stored value in capacitor until that value is taken for the operation and another data is stored. Static RAM uses only transistors to store data (as cross coupled inverter pair) so, SRAM don't need any refreshing circuit[6].

There are three major problems associated with the power dissipation in SRAM memory. First one is single word line for both read and write operations, which wasted the power when only one operation takes place[26]. Second one is unwanted switching activity of every transistors when the operations, which dissipates more dynamic power. The last major issue is short circuit power dissipation, which occurs when V_{dd} is shorted to ground for a small amount of time due to both pMOS and nMOS are switched ON during transition. Power dissipation of the SRAM memory can be reduced by reducing these three issues. A conventional 6T SRAM cell is shown in figure 1 and it consist of two cross coupled inverters and access or pass transistors.

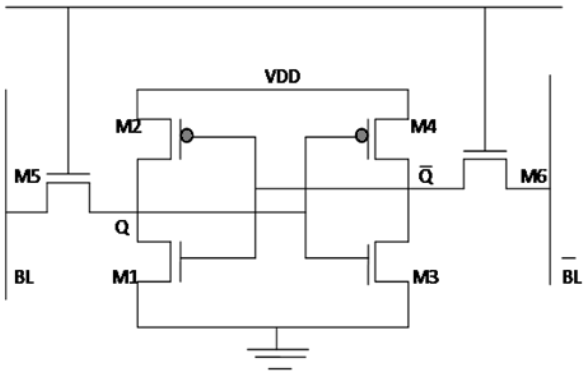

Figure 1: Conventional SRAM cell

Basic SRAM operation is tabulated in the table (Table 1). It can be done by different design techniques, out of which one technique or more than one can be employed in a design and the power dissipation amount is reduced.

Table I : SRAM Operation

Operation	Input		Output	
	BL	BL_bar	Q	Q_bar
Write 0	0	1	1	0
Write 1	1	0	0	1

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II. EXISTING METHOD – 10T SRAM CELL

An SRAM cell design is differentiated by 3 major parameters, number of transistors used, design technology and technique employed. Every design consists of a particular method in order to reduce the parameters area, power and delay and these techniques also varies the number of transistors.

The transistor count not varies when modification in conventional SRAM cell method is employed.

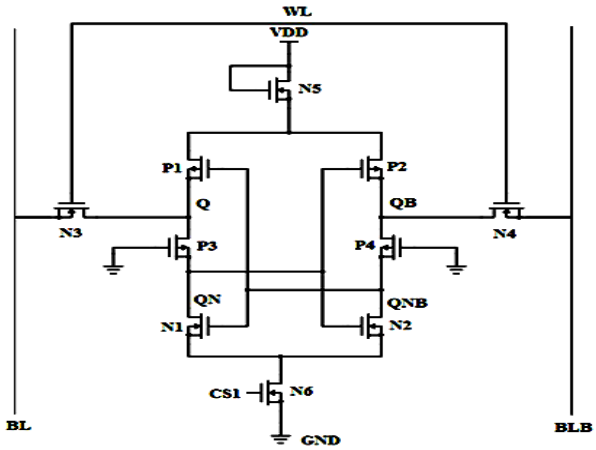

Figure 2: Existing 10T SRAM cell

In this method 10T SRAM cell there is a Vdd connected nMOS (N5) as shown in figure 2. The transistor N6 is controlled with the control signal. In write and hold mode the CS1 is set to '0'. So that the N6 transistor is in OFF state and disconnects the path from the ground. Thus the leakage power is reduced to large amount in hold and write mode. When CS1 is set to '1' during read mode so that the N6 is ON and makes to ground path. The stability of the cell is reduced due to scaling of Vdd because there is probability of flipping due to pre-charged bit lines the contents of storage nodes.

The stability is reduced due to scaling of Vdd is compensated due to the extra pMOS transistors P3 and P4. Which are always ON and they are added in between driver and access transistors. This design increases the read stability. When WL is enabled the voltage in the circuit are divided in series along N4 of access transistor, P4 of conducting pMOS and N2 of driver transistor. So that the suppressed voltage does not flip the contents of cell.

While writing the data if node is at '1' and another node will be at '0' to write '0' , BL is connected to ground and BL_bar is raised to Vdd and the WL line is enabled. The node Q charge from Vdd to '0' and node is discharged from '1' to '0' state. The node QN cannot be dropped below because pMOS does not pass '0'. But the falling of QN produces inverter to trigger and cross coupled inverters provides flip of state. The static power dissipation is to be reduced due to stacking of MOSFET.

The working modes of proposed SRAM are

A. Write mode: In this mode WL line is enabled by providing '1' and CS1 is set to be '0'. In order to write '1' and the BL is given with '1' and BLB is provided with '0'. In order to write '0' BL and BLB are provided with '0' and '1' respectively.

B. Hold mode: In this mode WL line is disabled by giving '0' and then the CS1 is connected to '0'.

C. Read mode: In read mode WL line is enabled by providing '1' and then the CS1 is connected to '0'. The BL and BLB are precharged to '1'.

III. PROPOSED METHOD – 10T SRAM CELL USING SLEEP TRANSISTOR & CONDUCTING pMOS

In this technique an additional nMOS sleep transistor is used between pull down network and ground and an additional pMOS sleep transistor is used between pull up network and V_{dd} [15]. The inverter is constructed from an nMOS and pMOS transistor connected in series between power and ground. Sleep transistor is added between actual ground and circuit ground called virtual ground. This device is turned-off during sleep mode to cut-off the leakage path mode[22]. Inserting the sleep transistors splits the chip power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

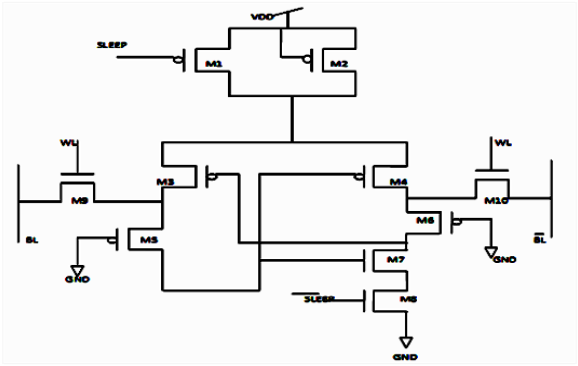

Figure 3: Proposed 10T SRAM cell

Conducting pMOS are used to provide the strong 1 or strong 0 values to the circuit. They are used to reduce the read failure that occurs in the circuit. They are maintained to be in active mode by connecting them with the ground to produce strong 0. The proposed 10T SRAM cell design is shown in the figure 3 and it consist of two sleep transistors, two conducting pMOS, two access or pass transistors, inverting circuit.

A. SRAM Array

SRAM is used to store and retrieve data, consists of number of bits in it for a particular time period. One SRAM cell of 2 inverters and 2 access transistor (6 transistors) can store only one bit of data inside it. As much number of bits need to store that much amount of SRAM cell is used [18]. These SRAM cells are placed as an array set as much needed because accessing array is an easy process. Representation of a bit cell is done by 2D method as column and row, which is shown in the figure 4 consist of precharge circuits, row decoder, column decoder, 4*4 SRAM array, sense amplifier.

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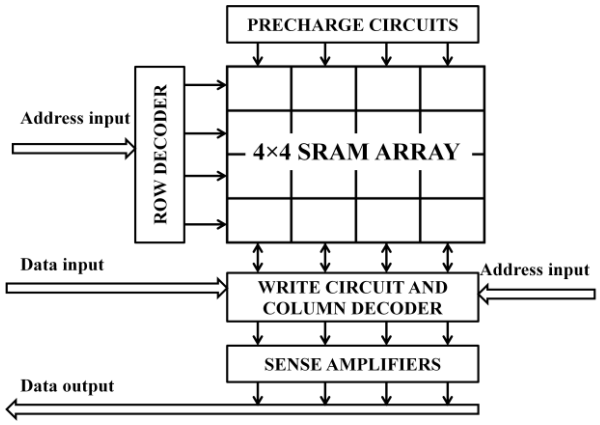

Figure 4: 4×4 SRAM Array

B. Schematic in Cadence

The schematic of 4×4 SRAM array is created by using the symbol representation of different blocks. A 4×4 SRAM array consists of 16 SRAM cells accessed by a 2:4 row decoder, a 2:4 column decoder, a column multiplexer, four precharge circuits and four sense amplifiers as one precharge circuit and one sense amplifier for each column.

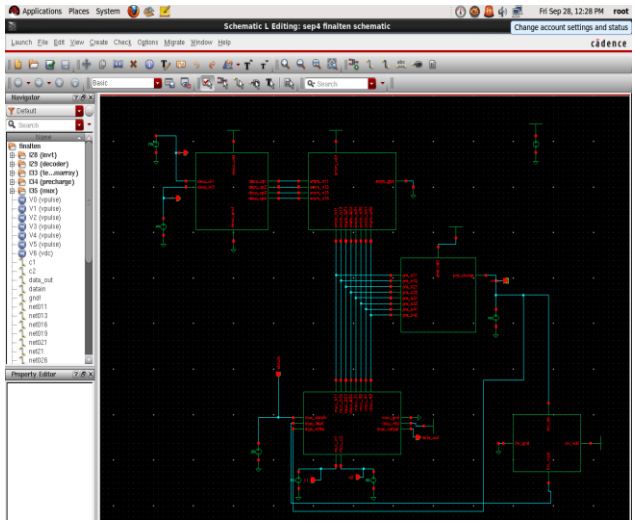

Figure 5: 4×4 SRAM array Schematic

Their performance strongly affects both memory access time, and overall memory power dissipation. CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. The final schematic of the 4×4 SRAM array is shown in the figure 5. Precharge circuit is used to load the supply voltage in BL and BL_ bar lines, which is used in the read operation only. In read operation, the read bit is done by using the voltage difference values between node and bit lines. Sense amplifier is a simple differential amplifier, which is used to read the data bit in the SRAM cell. It is also used in the read operation of the SRAM. Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. Their performance strongly affects both memory access time, and overall memory power dissipation. CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. Decoders are constructed using inverters and AND gates for using as row and column decoders in an array circuit like SRAM and DRAM memory arrays. Row decoder is directly employed and column decoder is used in the array circuit with the help of column MUX, a column MUX is a simple NMOS transistor with gate is controlled by the column decoder.

IV. RESULT AND DISCUSSION

When write/read_bar is enable, write data input is written in the SRAM cell at the allocated memory cell chosen by row and column decoders. The write and read operations are done successively in a single memory address. When read operation, the data write in the previous step is read and held that same value until the next read operation. The final output of the memory array is shown in the figure 6, which shows the waveforms write enable, Data in, row decoder inputs (r0, r1), column decoder inputs (c0, c1) and Data out.

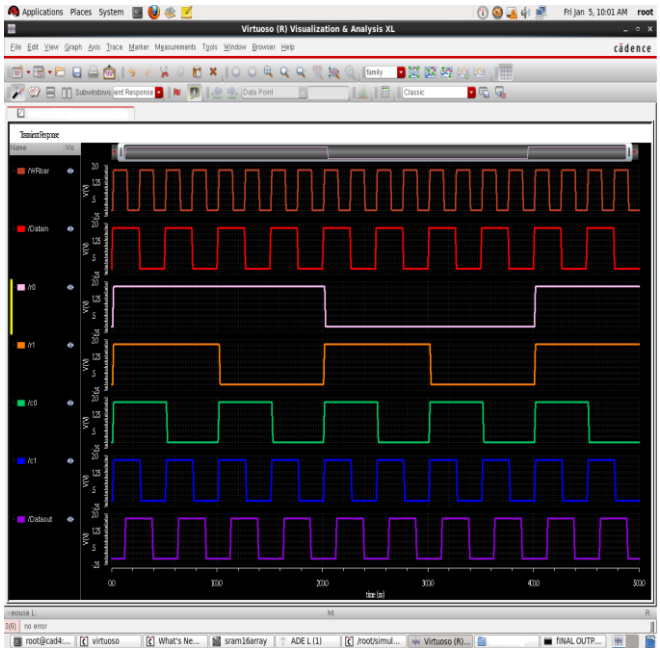

Figure 6: Result of 4×4 SRAM array

Power of the array design is done by CADENCE as the average power consumed by the various transistors available in the design for each cycle of the input, row and column decoder inputs and outputs. The output of the 4×4 SRAM array is shown in the figure 6. Delay is calculated between the data input and data output is tabulated between existing 10T SRAM and designed 10T SRAM.

Power and delay comparison of both designs are shown in the table 2.

Table 2
Power and Delay using Cadence

Design	Power	Delay
Conventional 6T SRAM Array	901.3mW	321.2µs
Existing 10T SRAM Array	899.8mW	229.3ns
Designed 10T SRAM Array	761.7mW	125.6ns

The table shows that the power consumption is reduced by 15% and delay is reduced by 45% when compared with conventional 6T SRAM.

V. CONCLUSION

This design provides a low power SRAM memory architecture design without any variation in area by using the 10T SRAM array design. A 4×4 memory array also created using the modified 10T SRAM cell. Thus the proposed memory architecture reduces the power by 15% and delay by 45% when compared with existing memory architecture.

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