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Contention Current Problem in Level Shifter

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Abstract*: This paper presents a comparative study for conventional and contention mitigated level shifter during shifting of level, occurs contention problem in current in the conventional level shifter during the transition. Level shifter control block control and minimize the power of the voltage converter DC circuits. The Multi VDD hopping in the huge circuit for power management is suffering from huge delay and power due to the current contention problem in Level shifter.

Keywords: Contention mitigated Level shifter, conventional Level shifter, DC to DC converter.

I. INTRODUCTION

The Designing of DC to DC (boost) converter at chip-level for a small portable electronic application which is the primary concern dual supply voltage management in sub-circuits level, as shown in Fig 1, the various application unit, which is a requirement of Level shifter unit. ASIC designing becomes complicated because of the scaling down technology in low power domain at the full-chip level [1,2]. / O blocks perform the same VDD, so the designer needs a level shifter for power management at the block level, as we know, to construct a DC to DC circuit, we have to attach multiple circuits to better results such as minimal power outages to minimize unwanted effects and for efficiency improvements, as shown in Fig 2. [14], So Block of the level shifter is used to one supply level to another voltage level in between I/O circuits and core circuitry for shifting the voltage level, now some of these circuit blocks operate at a lower voltage and some higher voltage, and the designer needs a shifter circuit to manage these voltages, that circuit needs to be a shifter of a voltage level is called level shifter [3]. Vdd hopping scheme in a system level to minimize the power up to four time than conventional single V_{DD} method and an important key in dynamic voltage scaling at system level. The novel DVS is called VDD hopping Generally, a problem has found that leakage current increases at high voltage gate, even when a low voltage gate is running a high voltage gate. In this paper, the contention current is explained which is generated during high to low and low to high transition, which has been compared to the CLS Shifter and CMLS [4].

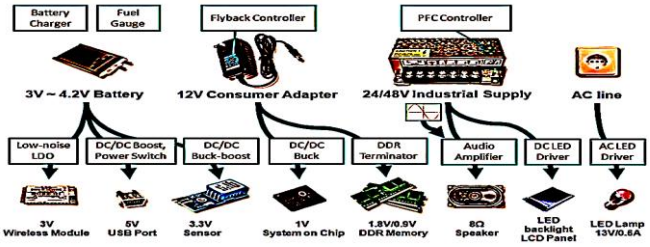

Fig 1Application of Level Shifter used in voltage Shifting[2]

II. CONVENTIONAL LEVEL SHIFTER

The contention problem comes during the shifting of voltage, the larger delay gives contention problem between the pull-up (P1 and P2) and pull-down (N1 and N2) transistor. This is disadvantage of conventional level shifter. As shown in Fig 3, At High Frequencies, Problem arises in Conventional Shifter-Contention comes in the circuit, contention emersion among P1 and N1, and during the transition low to high emersion high to low P2 and N2. So conventional level shifter

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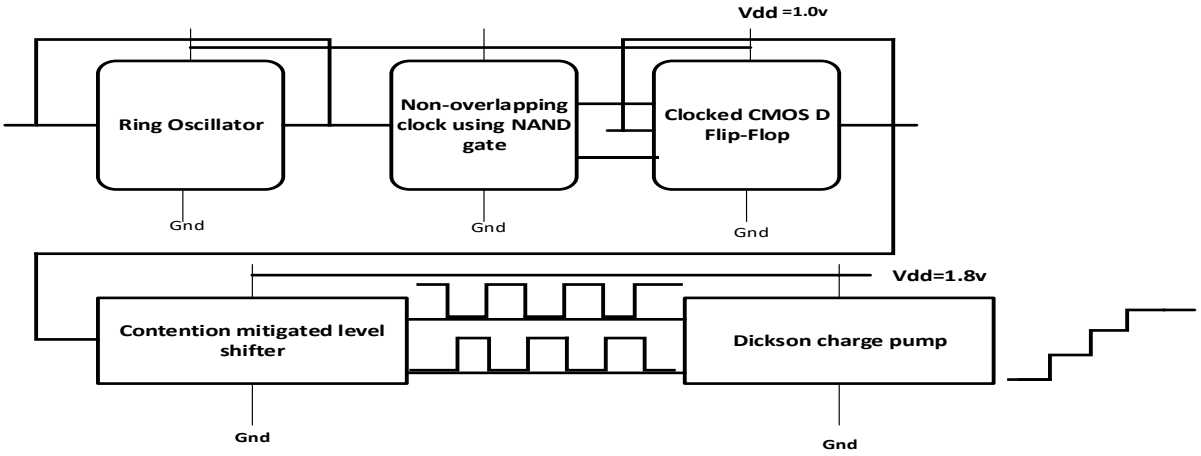

Fig 2 Use of Level shifter between the I/O system Level circuit.

cannot be used at high frequency, due to this reason, required high-speed level shifter [5]. This problem overcome through namely Contention Mitigated Level Shifter. It is a significant design challenge dynamic power dissipation management in scaling-down technology, leakage problem found in low power circuit design [6]. A crowbar current used to prevent an overvoltage condition.

The current contention problem generating between pull-up and pull-down transistor which is describing in detail as shown in Fig 4. Since these level shifters have a contention issue found in delay as well as power at low V_{DD} become higher and then not fitted with V_{DDL}. Thus It can be said conventional level shifter is not suitable for Low V_{DDL}. However Additional buffer circuit is reduced to loading effect from input to output help to transfer input /output voltage. To transfer a voltage from a first circuit with a high output impedance level to a second circuit with a low input impedance, a voltage buffer amplifier is used. level [7]. The interposed buffer amplifier prevents the second circuit from loading the first circuit unacceptably and interfering with its desired operation and buffer output which provides high noise immunity and stable output.

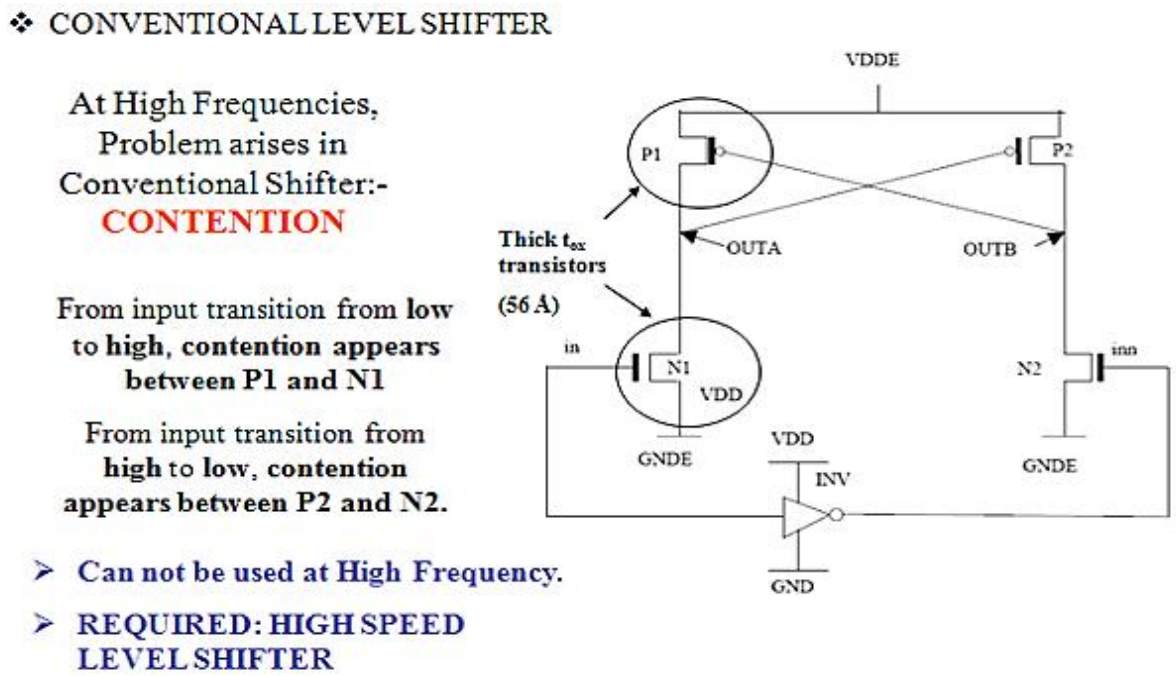

Fig 3Conventional Level Shifter

III. OUTPUT ROADMAP OF LEVEL SHIFTER

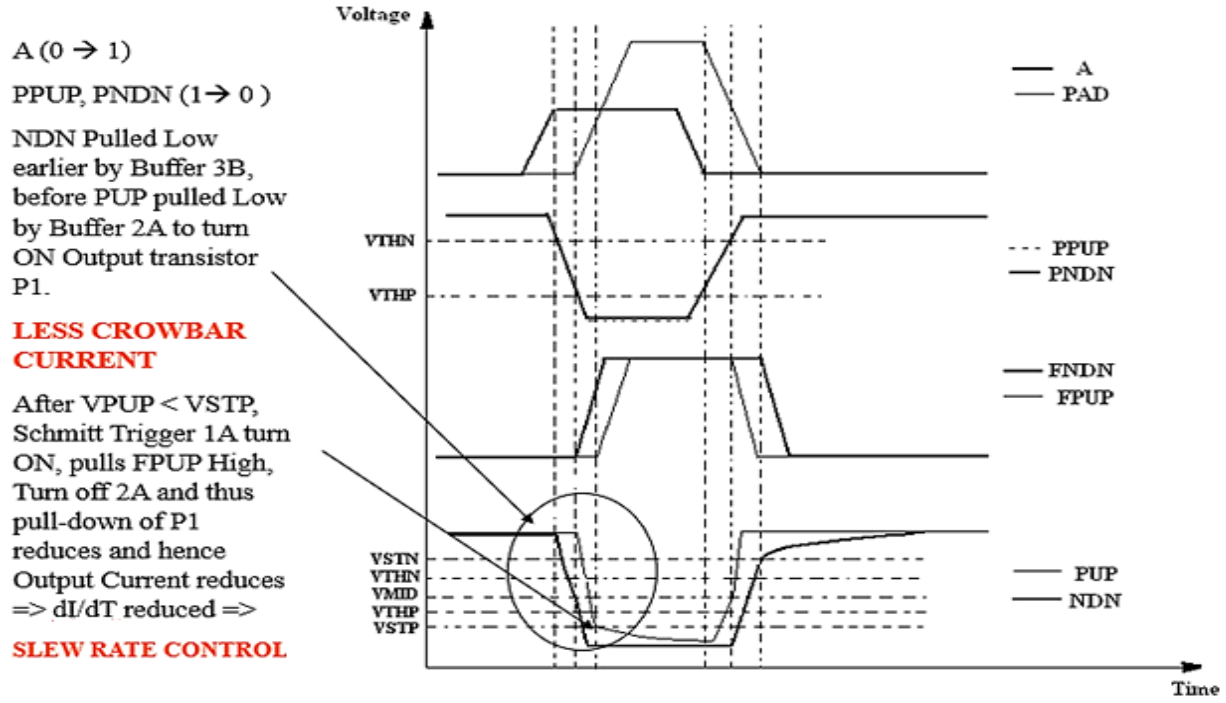

Fig 4 Current contention Problem in Conventional Level Shifter

IV CONTENTION MITIGATED LEVEL SHIFTER (CMLS)

The CMLS Level shifter circuit architecture are using two additional pull-up PMOS transistor which can be reduced contention current as shown in Fig 5 The When attaching two additional PMOS transistor among the Pull-up and Pull-down because of delay is an increase, because of this contention time become small, so process time margin decreases which improvement in delay and power. When the input voltage V_{DDL} is 0 V, the delay and power consumption of the CMLS are reduced by 43 % and 20% respectively, compared with the conventional level shifter as shown in Fig 6 and Fig 7. Area increases 4%, and leakage current increases in CMLS 72% from CLS. The Key benefit of CMLS shifter is avoiding crowbar current lowering. MOS transistor Positioning of MN1-MP3 & MN2-MP4 works as a partial inverter. So, the working point of A and B are speedy than conventional shifter. Hence, transition delay and switching power can be

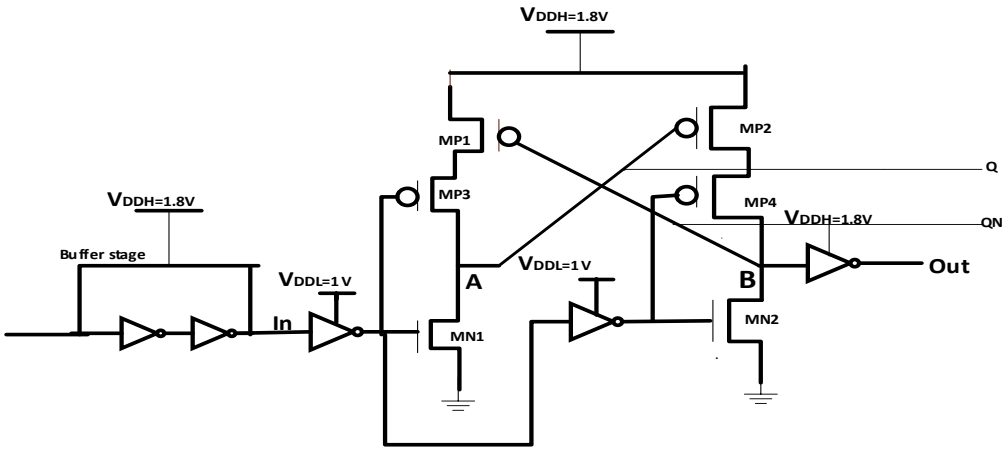

Fig 5 Contention Mitigated Level Shifter

reduced to a large extent in contention current due to contention also reduces the current tide. The Simulation result of CMLS Shifter is done by Tanner EDA Tools by 180nm (BSIM Technology model file) as shown in Fig 8. The use of shifter in boost DC circuit, change the position of dual supply voltage 1.8 to 0 V or 0 to 1.8 during the transition. The traditional level shifter and CMLS simulated power consumption when VDDL is varied and VDDH is set.

The prototype of the BSIM 180 nm CMOS is used. The region at the top of the CMLS is measured at 5%. Because MP1 and MP3, or MP2 and MP4, are in off states, the CMLS ' leakage current is lower than that of the conventional level shifter. The leakage current of the CMLS is 79nA at V_{DDH}=1.8 V and V_{DDL}=0 V, which is 72% of the leakage current of the traditional 109 nA level shifter. [7]

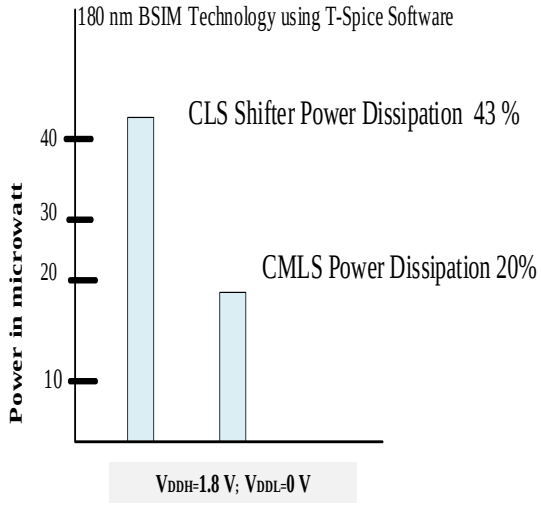

Fig 6 Simulation Result of Power

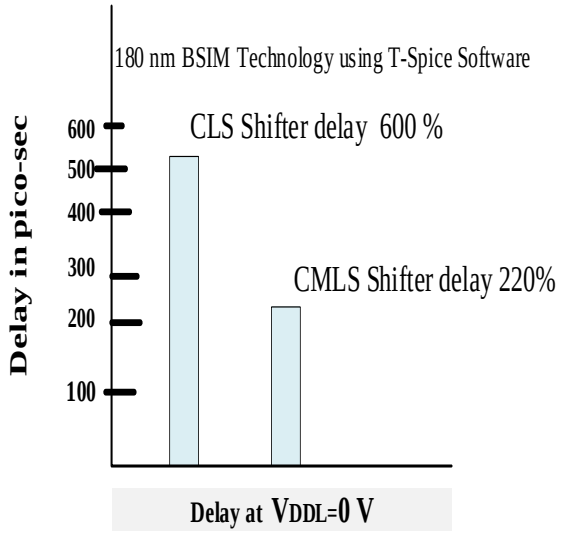

Fig 7 Simulation Result of Delay

VSIMULATION RESULT OF POWER, CURRENT, RISE-FALL TIME AND DELAY USING 180 NM TECHNOLOGY IN T-SPICE

TABLE - I

Table 1 Simulation Result of Level shifter (CMLS) Vdd =1.8V

Power	Current	Rise/Fall Time (output)_ V(Q)	Rise/Fall Time (output)_V(QN)
325 µw (max) 22 µw (Avg)	180 µw (max) 12.2 µw (Avg)	2.60 ns/1.23 ns	1.36 ns/1.65 ns

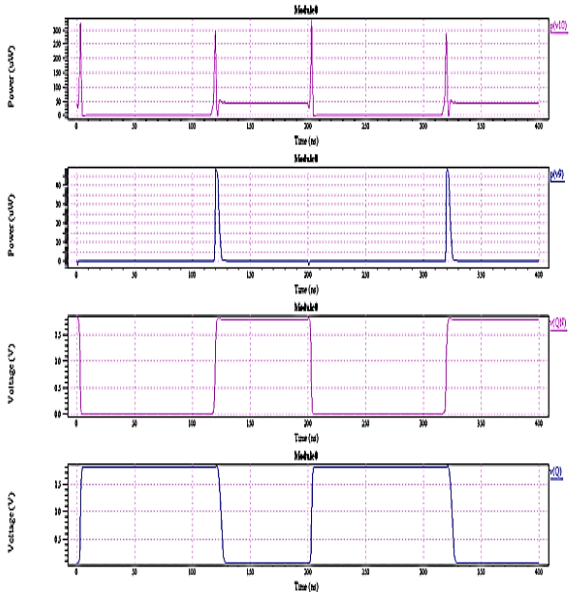

Fig 8 Simulation result of Contention Mitigated Level Shifter

VI. CONCLUSION

The shifter is shifting the supply of DC converter circuits (V_{DDH} to least V_{DDL}) that is a need for the control circuit to function correctly. The converting voltage phase low to high to provide minimum switch losses. The contention mitigated level shifter (CMLS) is better than conventional level shifter from power dissipation, preferable in high frequency and delay point of view, along with this, the crowbar current can also be reduced contention with the help of CMLS level shifter. The conventional level shifter cannot be used in high frequency. Reduce the crowbar current (V_{DDH} to V_{DDL}), which, due to increasing the switching speed as well as energy per switching according to minimum operating voltage, has been chosen. When the input voltage is V_{DDL} =0V, Delay and Power dissipation can be reduced by 43 % and 20 % in CMLS shifter as a comparison to CLS Shifter.

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