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Design of Low Power, High Gain Fully Differential Folded Cascode Operational Amplifier for Front End Read Out Circuits

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Abstract: ***The Front end read out circuits are major block in the implementation of Capacitive MEMS accelerometer. Front end read-out circuits comprises of preamplifier block containing folded cascode fully differential operational amplifier which are required for the signal conditioning of the signals received from the MEMS sensors. The op-amps are prime elements in design and implementation of mixed signal integrated circuits. The high gain and low power of the designed circuits helps in the designing of high precision IC's for numerous application. Amongst the available topologies folded cascode topology plays vital role in the design and development of low power, high gain read out circuits. This paper illustrates the design and analysis of low power, high gain fully differential Folded Cascode Operational Amplifier for front end read out circuits. The designed op-amp exhibits a power consumption or dissipation of 92.14 µW and relatively higher open loop DC gain value with a value calculated at 81.33 dB by employing folded cascode topology. The UGB and Phase Margin for the selected design are 35 MHz and 83.6^0 respectively. The design operates at 5V power supply with the bias current of 12.11 µA. The circuit design and simulations have been implemented using 0.18 µm CMOS technology.***

Keywords : Folded Cascode, Operational amplifier, Gain, PM, UGB, Front end Read out circuits and MEMS accelerometer.

I. INTRODUCTION

The Micro-electrical and Mechanical Systems (MEMS) are the combination of both electrical and the mechanical systems, collaborated in order to append the design aspects and properties of both the mechanical as well as the electrical systems so as to realize the enhanced functionality of the system[1]. MEMS is basically a technological process used to create miniature sized IC's.

The resultant IC's manufactured using the MEMS process technology comprises of the numerous abilities which are mainly Micro Scale Sensing, Micro Scale Actuating and Micro Scale Controlling [2-4].

The combined effect of these can be experienced at a macro-scale level.

The IC fabricated by implementing the MEMS processing technologies are majorly in the size range of µm to mm. The alluring ability of this field is its multifaceted characteristics, wide range applicability and comparatively dramatic impact on the society [5,6].

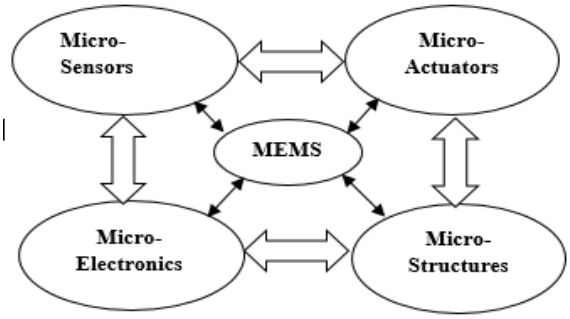

Fig 1: Widely used MEMS Components

Fig 1 exhibits the MEMS devices in a broader scenario comprising of Micro-Sensors , Actuators ,Micro-Electronics and Micro-Structures. MEMS (Micro electrical and mechanical systems) symbolize a technology used in the gyroscopes and accelerometer [7]. The various advantages which has led to the increased interest in the MEMS technology are:

- Versatile nature of the field led to collaborative work of different fields.
- New fabrication techniques led to increased reliability
- Reduced physical size, volume, weight & cost.
- MEMS techniques provide root cause for manufacturing of various products.

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The major goal in the designing of the readout circuits is to improve the minute changes which are sensed in the input sensors. These minute change occurred in the input sensor are having low driving capability and are mostly limited by their signal power level and the unwanted noise component. The read-out circuits are usually designed to improve the sensitivity of the system.

Section II depicts the system model as well as the boundary conditions employed for the implementation of the op-amp.

This section also shows the comparative analysis for several topologies in terms of power dissipation, open loop gain and output swing. Section III shows the proposed architecture along with the design steps and parameter specification. The section IV comprises of description of results and also discuss the AC gain phase response of the op-amp. The (W/L) ratio of the all the transistors in op-amp is also illustrated in that section. Comparative study of the proposed op-amp and in the various literature surveys is shown in Table VI, followed by the most significant points which are conclusion and acknowledgement in the corresponding sections.

II. OPERATIONAL AMPLIFIER FOR READ OUT CIRCUITS

The read out circuit is important component of MEMS. The output which is emitted from the MEMS Sensor portion of the system is usually having number of limitations like Low power level of Output Signal, More Noise interference, Low Sensitivity, Low Fidelity, Usually output is analog in nature and thus can't be fed to Digital blocks like Filters and different nature of output signal like capacitive change, frequency variation, optical variations etc.

The read-out circuits are usually implemented after the Sensor block of the MEMS system so that the signal conditioning can be easily accomplished. The front end read-out circuit or the interface unit comprises of amplifiers, ADC's, Modulator & Demodulator and the Filter's (Low Pass Filter's) as shown in Fig 2.

Operational Amplifiers from the time immemorial is a major element in design and development of the front end read out circuits. There utilization is well known in both analog as well as in mixed signal VLSI circuits [8]. There are several topologies available that can be used in the implementation of operational amplifier that includes 2-stage differential amplifier [9], telescopic topology, class AB topology, folded cascode topology and two stage differential amplifier with miller compensation technique [10]. Out of all the stated topologies, the topology used for the implementation of operational amplifier in this research paper is the single stage folded cascode topology along with the implementations of the bias reference voltages.

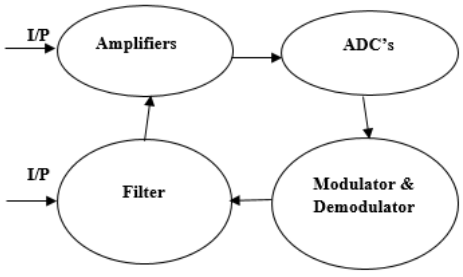

Fig 3: Block Diagram of Read out Circuit

It is well known phenomenon that the design of the structure, exhibiting low power dissipation and an excellent value of open loop DC gain is itself a challenging task as there is a tradeoff between open loop DC gain, power and other performance parameter [10]. However, these challenges have been studied by the various circuits. The various performance parameter which are majorly concerned are analyzed by taking various electrical characteristics into consideration namely: load capacitance, power supply voltage, open loop gain, ICMR, UGB, PM, output swing etc. [11]. Moreover, as operational amplifiers are fundamental constructional element of most of the mixed signal devices, they are majorly implemented in voltage regulators, LPF's, signal processing units and also in Analog-to-Digital Convertors as well as the Digital-to-Analog convertors (ADC's and DAC's) [12].

Majorly op-amps are concerned with the task of amplification, buffering and filtering. A well-known phenomenon about the operational amplifier is that they when implemented in the single stage mode, are faster & have extraordinary frequency response compared to the multi stage topology [13]. Since single stage op-amp doesn't satisfy the nominal values of the small signal voltage circuit thus they might not be able to curb the effects of non-linearity in the open loop scenario. This all leads to the mismatch in certain results which were intended [14]. Thus op-amps must exhibit wide range of phase margin in order to achieve high stability. For the achievement of better stability either frequency compensation technique or the single stage op-amps are used without compensating or compromising on the open loop dc gain aspect. All this is achieved with the help of folded cascode structure topology. In this topology, even single stage is capable to provide excellent stability and higher value of open loop dc gain. This topology is used in dual differential output mode. For various applications the architecture is used in the dual differential output mode. This architecture provide better rail to rail to output swing.

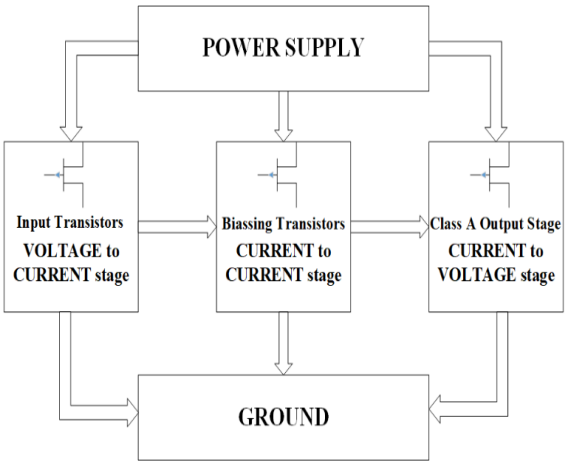

Fig 3: System Model for the general Folded Cascode Topology

Another major constituent in the design are the voltage reference circuits or the bias circuits along with the current mirror circuit configurations. Being a significant parameter in the circuit design, they in the present day's scenario are one of the configurationally major constituent of the electronic circuit.

The trimmed value of voltage cascode current mirror exemplifies a much higher voltage fluctuation during minimal proposed voltage specifications besides some of the basic conventional cascode current mirror circuits [16].

TABLE 1: Comparison of different topologies

Topology	Power Dissipation	Open Loop gain	Output Swing
Telescopic Cascode Opamp [14]	Average	Average	Average
Miller Opamp [10]	Low	High	Avergae
Folded Cascode Opamp [12]	Lower	Highest	Good

III.PROPOSED ARCHITECTURE AND STEPS

The system model utilized for the implementation of folded cascode operational amplifier is depicted in the Fig.3 which exemplifies the three stage implementation of the op-amp. The folded cascode architecture of the op-amp design the first stage in the topology is the input symmetrical transistors which are majorly exhibiting the voltage to current conversion process. After the V-I conversion the next stage comprising of the biasing transistors is the current to current conversion stage. Lastly, after the I-I stage the output stage implements Class A structure for the current to voltage conversion. This current to voltage conversion leads to the amplified version of the input voltage thereby giving the required amplification with low noise interference. The whole of the system would be working at +5 V of the power supply leading to less effect of the subthreshold conditions and also attaining low power dissipation.

In Table 1, three major topologies are being compared. Based on the comparison table the most suited topology for the op-amp design is the folded cascode topology for the readout circuits design. The boundary conditions that are utilized for designing the system model of the op-amp are listed in the table II.

As per the Table I, single stage fully differential folded cascode topology has been selected for low power dissipation circuit as well as for achieving higher value of open loop DC gain. The designed op-amp is a single stage opamp as I stage provides excellent stability and relatively good speed. The input is given to the PMOS in order to reduce the flicker noise components. The folded cascode op-amp are applied with bias current of 12.11 µA. The bias current or the reference current is given to the biasing circuits as well as to the current mirror circuit as well. The folded cascode topology is selected in implementing the operational amplifier the system is stable because the folded cascode topology is a first order system with the pole completely on the left half of the jω axis. In this topology there are basically two current sources are implemented which are fighting for the domination. This topology applies the folded cascode architecture at the differential input arms with a class A structure at the outputs for the peculiar implementation of the differential amplifier in order to achieve the good input and output common mode range along with self-frequency compensation and the higher gain in comparison with the two stage op-amps [14][15]. As we are well familiar with the fact that in order to make differential amplifier dual ended output the voltage gain of the op-amp has to be reduced to half. But this problem is rectified in the folded cascode structure.

The necessary preliminary assumptions of the various electrical parameters made, based on which the op-amp would be designed are illustrated in the Table II.

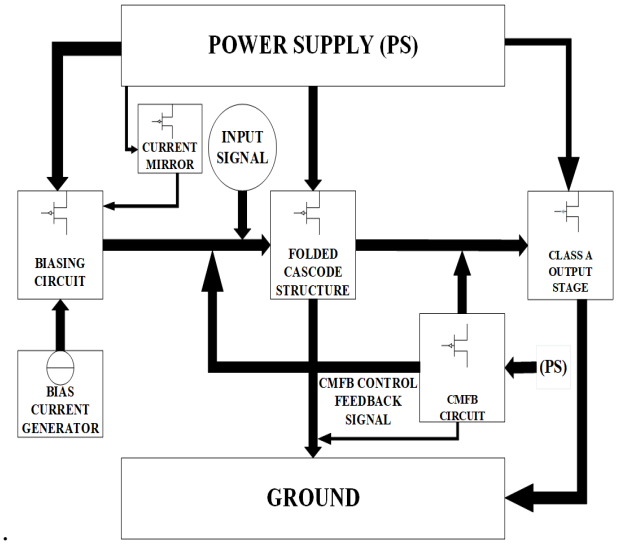

Fig 4: Proposed Architecture

TABLE II: Electrical Parameter under analysis [13]

Parameters	Values
Open Loop DC gain (dB)	≥65
Phase Margin (PM in degree)	≥45
UGB (in MHz)	≥10
Power Dissipation (µW)	≤200
Power Supply Voltage (V)	+5
CMRR (in dB)	≥20
PSRR (in dB)	≥30
ICMR (in V)	≥2.5

Pseudo Algorithm for the Designing of op-amp:

Step 1: Calculate the current value with the help of load capacitance and slew rate values:

$$I_3 = SR * C_L \qquad (1)$$

Step 2: Calculate the Bias currents in the output cascode while avoiding the process of zero current in the different cascodes:

$$I_4 = I_5 = 1.2I_3 \text{ to } 1.5I_3 \qquad (2)$$

Step 3: Calculate the Scalability or the Size of the MOSFET M_5 and MOSFET M_7 based on the maximum output voltage, V_{out} (max):

$$S_3 = \frac{8I_5}{(K'_p)*V_{DS5}^2} \qquad (3)$$

$$S_7 = \frac{2I_7}{(K_P')*V_{DS7}^2} \quad (4)$$

Let S_4=S_5 =S_{14} and S_7 =S_6 = S_{13}

$$V_{DS5}(sat) = V_{DS7}(sat) = \frac{V_{DD} - V_{out}(min)}{2} \quad (5)$$

Step 4: Calculate the Scalability or the Size of the MOSFET M_9 and MOSFET M_{11} based ssson the maximum output voltage, V_{out} (min):

$$S_{11} = \frac{2I_{11}}{(K_P')*V_{DS11}^2} \quad (6)$$

$$S_9 = \frac{2I_9}{(K_P')*V_{DS9}^2} \quad (7)$$

Let S_{10}=S_{11} and S_8=S_9

$$V_{DS9}(sat) = V_{DS11}(sat) = \frac{V_{out}(min) - |V_{SS}|}{2} \quad (8)$$

Step 5: Calculate the value of the self-bias resistors in the cascode topology based on the self-bias cascode features:

$$R_1 = {V_{DS14}(sat)}/{I_{14}} \quad (9)$$

$$R_2 = {V_{DS6}(sat)}/{I_6} \quad (10)$$

Step 6: Calculate the Scalability or the Size of the MOSFET M_9 and MOSFET M_{11} based on the Gain Bandwidth product:

$$GB = \frac{g_{m1}}{C_L} \quad (11)$$

Step 8: Calculate the Scalability or the Size of the MOSFET M_4 and MOSFET M_{11} from the Maximum ICMR such that the S_4 and S_3 must meet or exceed the requirement of STEP3:

$$S_4 = S_5 = \frac{2I_4}{k_p'*(V_{DD} - V_{in}(max) + V_{T1})} \quad (14)$$

Step 9: The typical value for the Differential Voltage gain is given as:

$$\frac{V_{out}}{V_{in}} = A_V = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right) * R_{out}$$

$$= \left(\frac{2+k}{2+2k}\right) * g_{m1} * R_{out} \quad (15)$$

Where the value of k and R_{out} are:

$$k = \frac{R_9(g_{ds2} + g_{ds4})}{g_{m7} * r_{ds7}} \quad (16)$$

$$R_{out} = (g_{m9} * r_{ds9} * r_{ds11}) \| [g_{m7} * r_{ds7} * (r_{ds2} \| r_{ds5})] \quad (17)$$

Step 10: Lastly calculate the power dissipation in the circuit as:

$$P_{diss} = (V_{DD} - V_{SS}) * (I_3 + I_{12} + I_{10} + I_{11}) \quad (18)$$

Table III: Transistors (W/L) Ratios

(Width/Length) Ratio	Value
$(\beta)_0$=$(\beta)_1$	1.8/1
$(\beta)_2$=$(\beta)_3$	3.75/10
$(\beta)_6$=$(\beta)_7$	25/2.5, M=10
$(\beta)_4$=$(\beta)_5$	12/1
$(\beta)_8$=$(\beta)_9$	35/1
$(\beta)_{11}$=$(\beta)_{12}$	2.5/1
$(\beta)_{10}$=$(\beta)_{24}$=$(\beta)_{25}$=$(\beta)_{26}$=$(\beta)_{27}$=$(\beta)_{34}$	3.5/1
$(\beta)_{13}$=$(\beta)_{14}$=$(\beta)_{16}$=$(\beta)_{19}$=$(\beta)_{32}$	1.75/1
$(\beta)_{15}$	1.625/1
$(\beta)_{17}$	4.5/1
$(\beta)_{18}$=$(\beta)_{20}$	3/1
$(\beta)_{21}$	4.4/2
$(\beta)_{22}$	2/1, M=4
$(\beta)_{23}$	12/2.31
$(\beta)_{28}$=$(\beta)_{31}$	3/7.31
$(\beta)_{29}$	3/2
$(\beta)_{30}$	1.405/3
$(\beta)_{33}$	1.25/1

Fig 5: Flow chart for the Low power dissipation Op-amp

Operational amplifier using folded cascode topology has been implemented by undergoing the above steps. The phase margin is calculated by applying the following equation:

$$Phase\ Margin = \Phi_M = Argument\ [-A(j\omega_{0dB})F(j\omega_{0dB})] \quad (19)$$

$$= Argument\ [L(j\omega_{0dB})] \quad (20)$$

As it is a well-known fact that the phase margin is calculated when there is addition of the phase i.e. the minimum amount or quantity of the phase that can be added to the system so that it reaches the edge of instability. PM can be calculated at ω_{gc} also known as the gain cross over frequency, derived by putting the gain of the system equal to 0 dB. Further this value is then applied to the phase calculation from which the PM can be derived as:

$$PM = 180^0 + \phi_0 \quad (21)$$

Where, ϕ_0 = Phase of the system

The Fig 5 represents the flow diagram representation of the design. Before implementing the design architecture the various steps are involved for the design purposes. All the design considerations are carried out based on the design parameters as well as by taking the boundary conditions into picture.

Based on the steps discussed for the design and implementation, the dimension of the transistors is given in the Table IV.

Fig 6 illustrates the circuit diagram of folded cascode op-amp with the installation of the CMFB circuit. In order to achieve the proper biases, various bias voltages are generated from the bias or reference voltage generation circuit in Fig 7. Various current mirror configurations are used to increase the current driving capacity of the circuit.

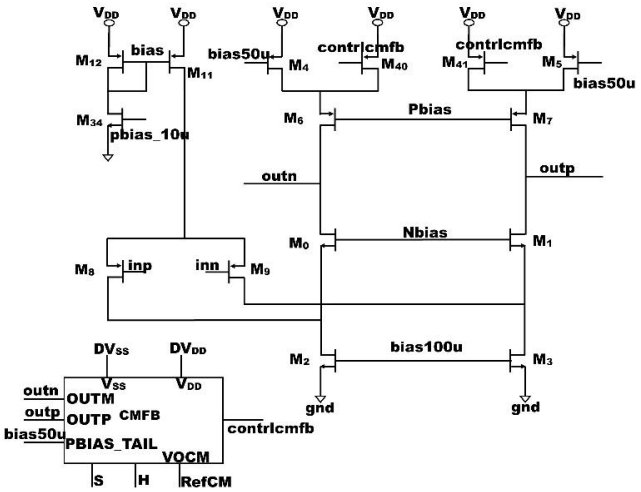

Fig 6: Folded Cascode using CMFB circuit

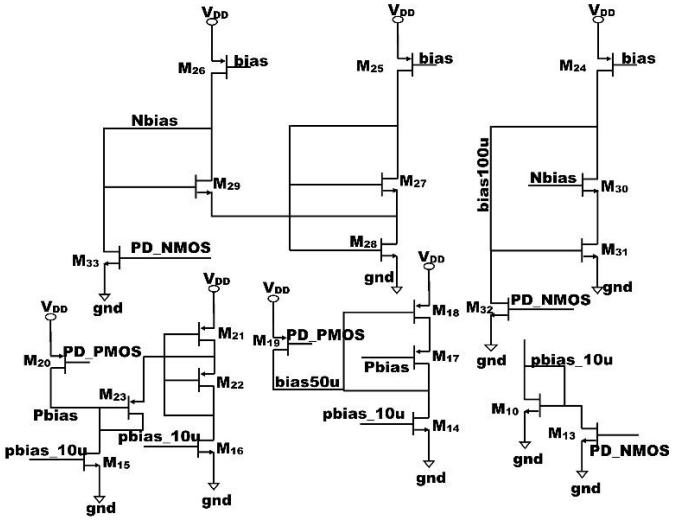

Fig 7: Biasing circuit for the folded cascode

In order to stabilize the output voltage swing, output common mode feedback signal is implemented. In the output CMFB circuit, error signal is generated which shows the similar traits of the feedback system. As in the case of the negative feedback, whenever the error signal is generated there is a rise in the current of one arm i.e. one arm of the folded cascode goes to the positive rail supply voltage and the other goes to the negative rail supply [17]. Fig 8 shows the output CMFB circuit. In order to increase the capability and to make the op-amp fully differential the output voltage swing must be maintained as the op-amp can go from the positive swing to the negative swing i.e. it swings between rail to rail power supplies. The CMFB circuit implemented in the folded cascode topology in order to improve the output voltage swing is usually employed in the switched capacitor mode with the help of various pass transistor logic, capacitive loads and the clock signals[18]. Here 'S-clock' and 'H-clock' signals are the two complimentary clocks which are passed through pass transistor logic and can be used as the 'ON' and 'OFF' signals.

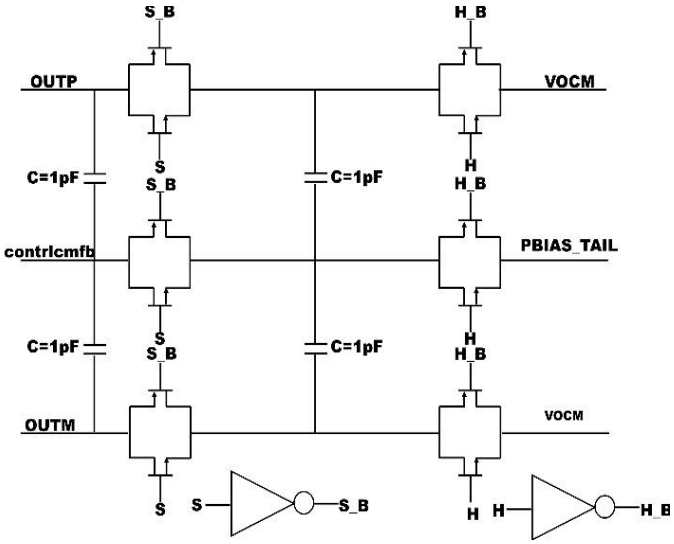

Fig 8: Output CMFB circuit

The design is further compared with the existing architectures in Table V. Based on the design, the simulations were carried out and the analysis done shows the open loop DC gain value of 81.33 dB with an excellent PM value of 83.6^0 and a comparatively fair UGB of 35 MHz while working at +5V power supply and bias current of 12.11 µA. The power dissipated by the proposed design is also low and numerically equals 92.14 µW.

From the Table V we get to know the various simulation results of the folded cascode operational amplifier which has been designed. A comparative analysis of the previous work and the current work done is accomplished in Table. It is clear that the folded cascode op-amp designed at 0.18 µm have a comparatively higher gain value of 81.33 dB with excellent PM value of 83.6^0 and UGB equals 35 MHz. The power dissipated by the circuit is also at a lower level having value equals 92.14 µW. But the only drawback is the relatively fair value of UGB which is 35 MHz.

IV.RESULT AND DISCUSSION

The implementation of fully differential folded cascode op-amp topology along with the common mode feedback circuit (CMFB) is depicted in Figs 6, 7 and 8. From the Fig 9 the AC gain plot is illustrated in Bode plot format from which it is clear that the open loop DC Gain of the folded cascode op-amp is 81.33 dB having excellent UGB value of 35 MHz. Based on the design specification the gain achieved is itself is one of its kind at such a lower value of power supply voltages and the bias current and a decrease in the value of the phase margin. From the Table V we get to know the various simulation results of the folded cascode operational amplifier which has been designed. Based on the above Fig 10, which depicts the phase response of the operational amplifier working in the folded cascade topology. From the Fig it can be deduced that the Phase Margin of the system is about 83.6^0 which excellent in its own term. Moreover, the power dissipated by the whole circuit is 92.14 µW.

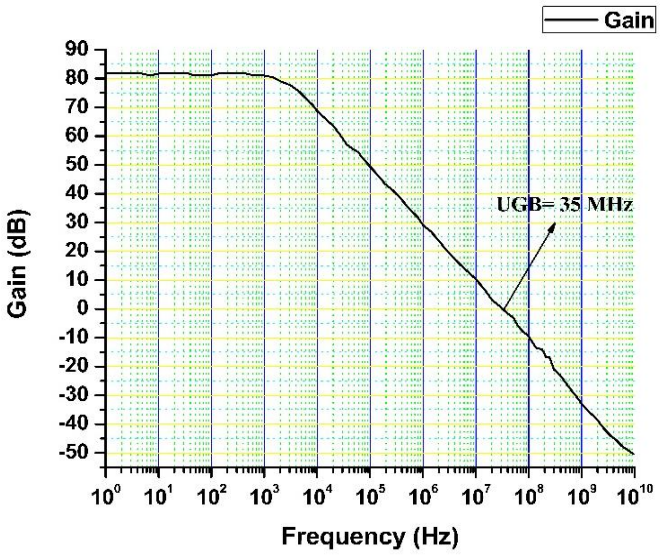

Fig 9: AC Gain Plot of Folded Cascode using CMFB Circuit

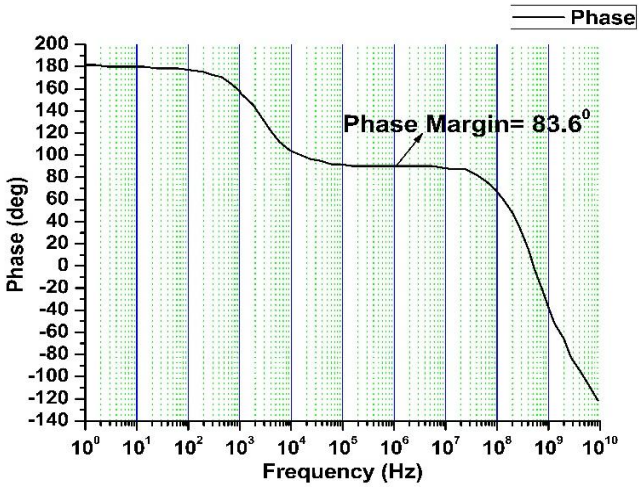

Fig 10: AC Phase Plot of Folded Cascode using CMFB

TABLE IV: Simulation Results

Parameters	Assumed Values	Values obtained
Open Loop DC gain (dB)	≥65	81.33
Phase Margin (PM in degree)	≥45	83.6
UGB (in MHz)	≥10	35
Power Dissipation (μW)	≤200	92.14
Power Supply Voltage	+5V	+5V
Load Capacitance (fF)	250	250
CMRR (in dB)	≥20 (magnitude)	-38.40
PSRR (in dB)	≥30 (magnitude)	-44.06
ICMR (in V)	≥2.5	4.8

TABLE V: Comparative Results

Parameter Analyzed	This Work	Ref.[13]	Ref.[[12]	Ref.[[19]	Ref.[[16]
Open Loop DC Gain (dB)	81.33	80.12	62.56	75.1	60
PM	83.6^0	71^0	65.01^0	53.8^0	-
UGB	35 MHz	90 MHz	180.03 MHz	30.5 MHz	-
ICMR	4.8V	4.4V	-	1.8V	-
PSRR	44.06dB	83.08 dB	-	-	-
CMRR	38.40dB	74.496dB	-	77.8dB	-
Power Dissipation	92.14 μW.	-	-	-	-

This is the static power dissipation which is the product of the total source or sink currents in the differential arms and the power supply voltages. By increasing the bias current we could increase the UGB and slew rate (SR) but the power dissipation also increases along with the increase in the MOS chip area and a decrease in the value of the phase margin.

A comparative analysis of the previous work and the current work done is accomplished in Table V. It is clear that the folded cascode op-amp designed at 0.18 μm have a comparatively higher gain value of 81.33 dB with excellent PM value of 83.6^0 and UGB equals 35 MHz. The power dissipated by the circuit is also at a lower level having value equals 92.14 μW. But the only drawback is the relatively fair value of UGB which is 35 MHz.

V.CONCLUSION

This paper presents the design of the low power, high gain folded cascade operational amplifier for the front end read-out circuits using 0.18 μm CMOS technology. This design is further compared with the reported architectures. Based on the design, the simulations were carried out and the analysis done shows the open loop DC gain value of 81.33 dB with an excellent PM value of 83.6^0 and a comparatively fair UGB of 35 MHz while working at +5V power supply and bias current of 12.11 μA. The power dissipated by the proposed design is also low and numerically equals 92.14 μW. The achieved results in this paper for the proposed approach presents high dynamic range along with very good noise performance. The two parameters are very important as required by readout circuits in noisy environment.

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REFERENCES

1. Qu, H." CMOS MEMS fabrication technologies and devices." Micromachines, vol.7 no.1, pp.14, 2016.
2. N. Yazdi et al. "Micromachined Inertial Sensors." in Proc. IEEE, vol. 86, pp. 1640-1659,Aug. 1998.
3. C. Lu, M. Lemkin, B.E. Boser. "A Monolithic Surface Micromachined Accelerometer with Digital Output." in IEEE J. Solid-State Circuits, vol. 30, pp. 1367-1373, Dec. 1995.
4. University of California, Berkeley. Berkeley Sensor & Actuator Center. B.E. Boser."Electronics for Micromachined Inertial Sensors.", Berkeley, CA., 1997.
5. N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors,"in Proc. IEEE, vol. 86, no. 8, pp. 1640−1659, Aug. 1998.
6. L. Baxter, "Capacitive sensors: design and applications," IEEE Press,1996.
7. M. Kranz, S. Burgett and T. Hudson, "Performance of a silicon-on insulator MEMS gyroscope with digital force feedback," in PLANS 2004, pp. 7−14, Apr. 2004.
8. B. Razavi, *Design of Analog CMOS Integrated Circuits*. Boston, MA: McGraw-Hill, 2001.
9. Gaurav Sharma, Anil Bhardwaj, Sumeet Gupta, " A High gain and High stability Operational amplifier for the capacitance to voltage converters at 180 nm technology. " International Journal of Electronics and Communication Engineering & Technology (IJECET). Volume:9, Issue: 1, Pages:31-41, 2018.
10. Tan, Min, and Qianneng Zhou. "A two-stage amplifier with active miller compensation." In *2011 IEEE International Conference on Anti-Counterfeiting, Security and Identification*, pp. 201-204. IEEE, 2011.
11. Akbari, M., Javid, A., & Hashemipour, O. (2014, May). Akbari, Meysam, Ardavan Javid, and Omid Hashemipour. "A high input dynamic range, low voltage cascode current mirror and enhanced phase-margin folded cascode amplifier." In *2014 22nd Iranian Conference on Electrical Engineering (ICEE)*, pp. 77-81. IEEE, 2014.
12. Aminzadeh, H., Danaie, M., & Lotfi, R. Design of high-speed two-stage cascode-compensated operational amplifiers based on settling time and open-loop parameters. INTEGRATION, the VLSI journal, 41(2), pp.183-192 , 2008 .
13. Guo, Y. "An accurate design approach for two-stage CMOS operational amplifiers." In Circuits and Systems (APCCAS), 2016 IEEE Asia Pacific Conference, pp. 563-566, 2016.
14. Ren, M. Y., Wu, T., Song, M. X., & Zhang, C. X. "Design Procedures for a Fully Differential Telescopic Cascode Two-Stage CMOS Operational Amplifier." Procedia Engineering, pp.29, 4030-4034, 2012.
15. Gupta, A., Chandrawat, U. B. S., Mishra, D. K., Khatri, R., & Jain, P. "A two stage and three stage CMOS OPAMP with fast settling, high DC gain and low power designed in 180nm technology." International Conference on In Computer Information Systems and Industrial Management Applications (CISIM), pp. 448-453, 2010.
16. Lahariya, A., & Gupta, A. "Design of two stage CMOS operational transconductance amplifier with slew rate enhancement technique using 180nm." In Electrical, Electronics, Signals, Communication and Optimization (EESCO), International Conference on, pp. 1-6, 2015.
17. Kuo, P. Y., Kan, T. H., & Hsu, K. Y. "The standard design flow for two-stage amplifier design." In Consumer Electronics-Taiwan (ICCE-TW), 2015 IEEE International Conference, pp. 458-459, 2015.
18. Dillep, P., & Saini, G. "Enhanced cascode node impedance to the improved recyclic folded cascode OTA." In Advanced Communication Control and Computing Technologies (ICACCCT), pp. 451-455, 2014.
19. Bendre, V., & Kureshi, A. K., "Performance analysis of operational transconductance amplifier at 180nm technology." Second International Innovative Applications in Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH), pp. 271-276, 2016.

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