

# Analytical 2D Modeling of Surface Potential and Threshold Voltage for Lightly Doped Substrate NMOS

Nitin Sachdeva, Tarun Kumar Sachdeva



**Abstract:** Reducing the device dimensions leads to scaling of various parameters like junction depth, supply voltage and gate oxide thickness and results to the variation of threshold voltage. Threshold voltage variations can cause serious design problems. So threshold voltage can be adjusted by various ways which is the most important parameter of the MOSFET. This paper depicts the analytical modeling and simulation of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The expression for potential at source and drain ends and threshold voltage has been derived and the theoretical values are compared with simulated values. From simulation results from SILVACO TAD tool, threshold voltage of 0.22V is achieved at a work-function of 4.12eV.

**Keywords:** MOSFET, NMOSFET, SILVACO, Athena, Atlas, GCA.

## I. INTRODUCTION

The Gradual channel approximation (GCA) claims that the electric field components parallel and perpendicular to the surface are effectively separated and therefore, can't completely contribute for the observed device characteristics. These small-geometry characteristics may critically limit the operating conditions of the transistor and impose limitations upon the practical utility of the device. Precise identification and characterization of these small-geometry effects are vital especially for sub-micron MOSFETs. The progress in VLSI fabrication technologies are primarily based on reduction of device dimensions such as channel length, the junction depth and gate oxide thickness. This paper involves the analytical modeling of potential distribution, threshold voltage, electric field distribution and donor concentration and valence and conduction band diagram of lightly doped 45 nm NMOS has been discussed. The design, analysis and simulation work has been carried out in ATHENA and ATLAS of SILVACO TCAD tool. The virtual fabrication of 45nm NMOS is carried

out in ATHENA and simulation work is done in ATLAS. The device is virtually fabricated with lightly doped substrate having  $5 \times 10^{15} \text{cm}^{-3}$  concentration and effective channel length of 40nm. The device structure after simulation is shown

Figure 1 below:

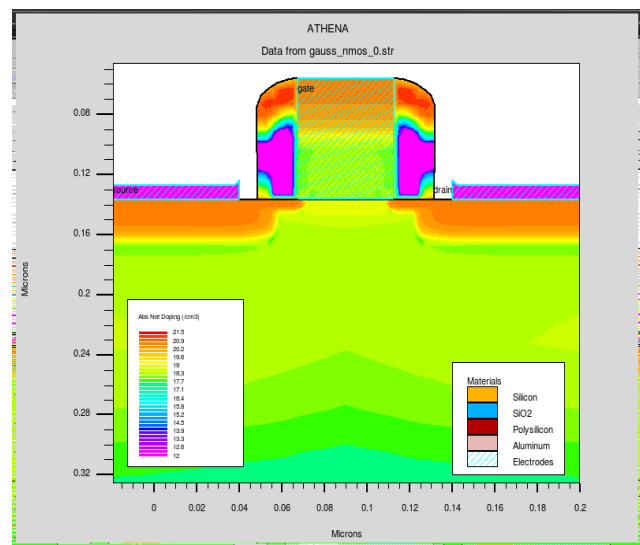


Figure 1 Structure of NMOS device

## II. MODELING OF POTENTIAL DISTRIBUTION

To obtain the physical behaviour characteristics of NMOS, potential distribution of the gate, drain and source under different biasing condition must be studied. Potential distribution can best understand by Poisson equation.[1] The potential distribution in MOSFET is determined by 2D Poisson's equation

$$\frac{\partial^2 \phi}{\partial x^2}(x,y) + \frac{\partial^2 \phi}{\partial y^2}(x,y) = \frac{\rho(x,y)}{\epsilon_{si}} \dots \dots \dots (1)$$

The Parabolic function is given by:

$$\phi(x,y) = C_0(x) + C_1(x) \cdot y + C_2(x) \cdot y^2 \dots \dots \dots (2)$$

and the boundary condition for surface potential is given by equation 3

$$\phi(x,0) = \phi_s(x) \dots \dots \dots (3)$$

The electric field at  $y=0$  is resolved by gate voltage,  $V_G$  or the electric flux at gate oxide interface is

$$\left. \frac{\partial \phi}{\partial y}(x,y) \right|_{y=0} = \frac{\epsilon_0 \epsilon_x}{\epsilon_{si}} \cdot \frac{\phi_s(x) - V_{GS}}{t_{ox}} \dots \dots \dots (4)$$

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$$\left. \frac{\partial \phi}{\partial y} (x, y) \right|_{y=0} = \frac{cox}{\epsilon si} (\phi_s(x) - V_{gs} + V_{fb}) \dots \dots \dots (5)$$

Where

$$V_{fb} = \phi_m - \chi_{si} - \frac{E_g}{2Q} - V_T \ln \left[ \left| \left( \frac{Na(xi)}{ni} \right) \right|_{y=0} \right]$$

Band gap of silicon at 300k

$$E_g = \left[ 1.16 - \left( \frac{7.02 \times 10^{-4}}{1108 + T} \right) \right]$$

$$ni = 3.1 \times 10^{16} T^{\frac{3}{2}} \exp \left( \frac{E_g}{2KT} \right) \text{ and}$$

$$V_T = \frac{KT}{q}$$

$$\phi(x, y) = V_{bs} \text{ and } \left. \frac{d\phi}{dy} (x, y) \right|_{y=tsi} = 0$$

The surface potential at source end is

$$\phi(0, 0) = \phi_s(0) = V_{bi}$$

The surface potential at drain end is

$$\phi(L, 0) = \phi_s(L) = V_{bi} + V_{ds}$$

Now we have

$$\phi(x, y) = C_0(x) + C_1(x) \cdot y + C_2(x) \cdot y^2 \quad (6)$$

$$\phi(x, 0) = C_0(x) = \phi_s(x) \text{ at } y=0$$

Put the value in equation (6)

$$\phi(x, y) = C_0(x) + C_1(x) \cdot y + C_2(x) \cdot y^2 \quad (7)$$

Differentiate w.r.t y

$$\frac{\partial \phi}{\partial y} (x, y) = C_1(x) + 2y \cdot C_2(x)$$

$$\left. \frac{\partial \phi}{\partial y} (x, y) \right|_{y=0} C_1(x) = \frac{\epsilon ox}{\epsilon si} \cdot \frac{\phi_s(x) - V_{gs}}{t_{ox}}$$

Put the value of  $C_1(x)$  in equation (2)

$$\phi(x, 0) = \phi_s(x) + \frac{\epsilon ox}{\epsilon si} \cdot \frac{\phi_s(x) - V_{gs}}{t_{ox}} \cdot y + C_2(x) \cdot y^2 \dots \dots \dots (8)$$

Now

$$\left. \frac{\partial \phi}{\partial y} (x, y) \right|_{y=tsi} = \frac{\epsilon ox}{\epsilon si} \cdot \frac{\phi_s(x) - V_{gs}}{t_{ox}} + 2y \cdot C_2(x) = 0$$

$$C_2(x) = - \frac{\epsilon_{ox}}{2 \epsilon_{si} t_{si}} \frac{\phi_s(x) - V_{gs}}{t_{ox}}$$

Put the value of  $C_2(x)$  in equation (8)

$$\phi(x, 0) = \phi_s(x) + \frac{\epsilon ox}{\epsilon si} \cdot \frac{\phi_s(x) - V_{gs}}{t_{ox}} \cdot y - \frac{\epsilon_{ox}}{2 \epsilon_{si} t_{si} t_{ox}} (\phi_s(x) - V_{gs}) \cdot y^2$$

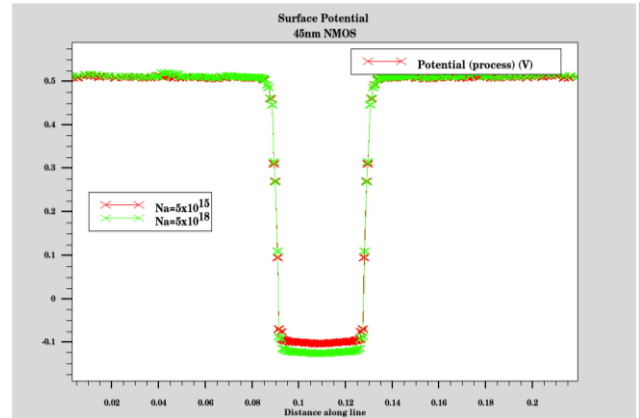


Figure 2 Surface Potential at different doping concentrations

The Figure 2 shows the surface potential at different substrate doping concentrations. The surface potential is shown for lightly doped substrate having concentration of  $5 \times 10^{15} \text{cm}^{-3}$  and heavily doped substrate having concentration of  $5 \times 10^{18} \text{cm}^{-3}$ .

### III. THRESHOLD VOLTAGE MODELING

The minimum Gate voltage,  $V_{GS}$  required to cause surface inversion is well known as threshold voltage. Threshold voltage depends on work-function between the gate and channel, the gate voltage component to change the surface potential, the voltage component to offset the fixed charges in the gate oxide and in the silicon oxide interface [2,3]. The work-function difference between the gate and the channel indicates the built-in potential of the MOS system. Depending on the gate material, the work function difference is

$$\phi_{GC} = \phi_F(\text{substrate}) - \phi_F(\text{gate}) \dots \dots \dots (9)$$

The first part of the threshold voltage reports the voltage drop across the MOSFET that is built in potential. The input gate voltage is varied stepwise to achieve surface i.e. to change the surface potential by  $-2\phi_F$ . This reports the second component of the threshold voltage. Now third component of the applied gate voltage is demanded to offset the depletion region charge, which is due to the fixed acceptor ions located in the depletion region.

$$Q_{B0} = -\sqrt{2q \cdot N_a \cdot \epsilon_{si} \cdot | -2\phi_F |}$$

The depletion region charge density can be expressed as a function of source-to-substrate voltage,  $V_{SB}$

$$Q_{B0} = -\sqrt{2q \cdot N_a \cdot \epsilon_{si} \cdot | -2\phi_F + V_{SB} |}$$

The component that neutralizes the effect of depletion region charge is equal to  $-Q_B/C_{ox}$ ; Where  $C_{ox}$  is the gate oxide capacitance per unit is.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

The generalized form of the threshold voltage can also be written as in equation 10.

$$V_{T0} = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \dots \dots \dots (10)$$

The depletion region charge density must be modified to indicate the influence of  $V_{SB}$  upon that charge is given by:

$$V_{T0} = \phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \dots \dots \dots (11)$$

The generalized form of the threshold voltage can also be written as

$$V_T = \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

$$= V_{T0} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

$$\frac{Q_B - Q_{B0}}{C_{ox}} = - \sqrt{\frac{2 \cdot q \cdot N_a \cdot \epsilon_{si}}{C_{ox}}} \cdot (\sqrt{-2\phi_F + V_{SB}} - \sqrt{|2\phi_F|})$$

The most general expression of the threshold voltage is

$$V_T = V_{t0} + \gamma \cdot \sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \dots \dots \dots (12)$$

where the parameter  $\gamma$

$$\gamma = \sqrt{\frac{2 \cdot q \cdot N_a \cdot \epsilon_{si}}{C_{ox}}}$$

According to the expression of threshold voltage, Gate oxide thickness ( $t_{ox}$ ) is inversely proportional to Oxide Capacitance ( $C_{ox}$ ) [4]. Theoretically, if the  $t_{ox}$  is decreased from 2nm to 1nm, the value of  $C_{ox}$  increases and  $C_{ox}$  is directly proportional to threshold voltage. So the increased value of  $C_{ox}$  will increase the value of threshold voltage as shown in graph also. The theoretical and simulated value of threshold voltage is matched here to analyse the effect of threshold voltage.

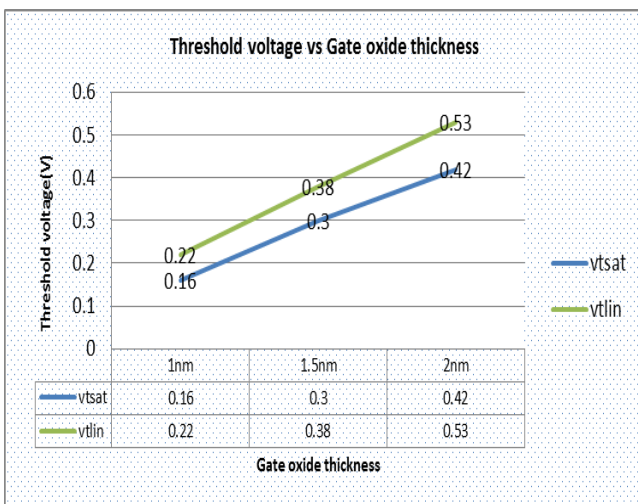


Figure 3 Variation of Threshold voltages with Gate oxide thickness

Figure 3 shows the variation of threshold voltage with various gate oxide thicknesses. There are two threshold voltages: One is  $V_{tsat}$  at  $V_{ds}=1.2V$  and  $V_{tlin}$  at  $V_{ds}=0.05V$ . These two voltages are considered at various drain voltages to analyse the effect of DIBL.

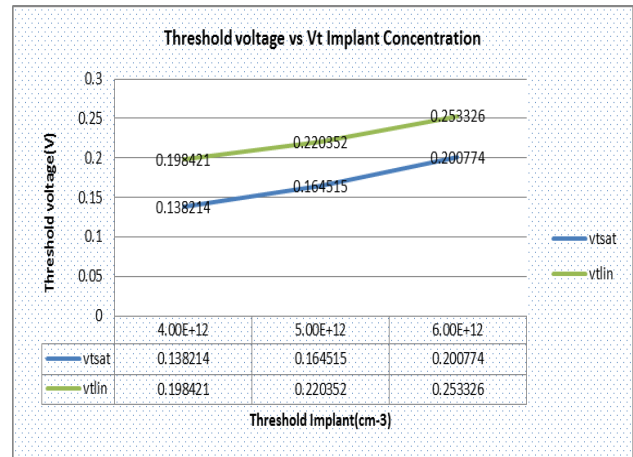


Figure 4 Variation of threshold voltage with threshold implant concentration

According to the expression of threshold voltage, threshold adjust concentration is directly proportional to the threshold voltage. It can be adjusted by varying its concentration. During fabrication, a layer of threshold implant is implanted by ion implantation process to adjust threshold voltage [5,6]. After simulation of the device, Figure 4 shows the adjustment of threshold voltage with threshold implant concentration. The value of threshold voltage can be increased or decreased by increasing or decreasing the concentration of threshold implant concentration respectively. .

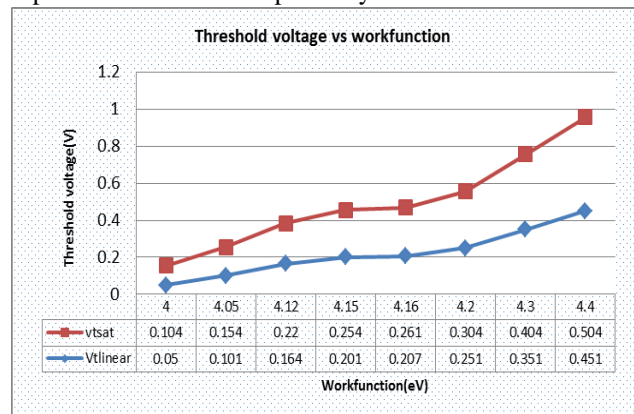


Figure 5 Variation of Threshold voltage with different work-functions

Threshold voltage can also be adjusted by increasing or decreasing the work-function of the Gate electrode. It is directly proportional to the threshold voltage. The work-function of 45nm NMOS device is varied from 4 eV to 4.4 eV in SILVACO and the above figure 5 shows the simulated results that the as the work-function of the gate electrode increases, the value of threshold voltage increases.

#### IV. CONDUCTION AND VALENCE BAND ENERGY DIAGRAM

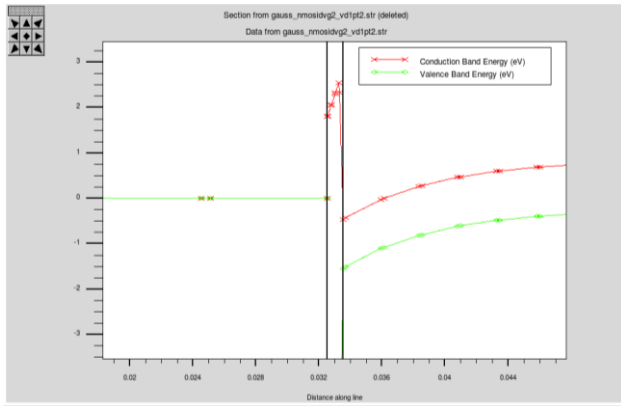
An intrinsic semiconductor has equal no. of holes and electrons so its Fermi level is in the middle of valence and conduction band [7]. Fermi level is represented by Fermi-Dirac function which is dependent on temperature. It is represented as:-



$$F(E) = \frac{1}{1 + e^{(E-E_F)/KT}} \dots\dots\dots(13)$$

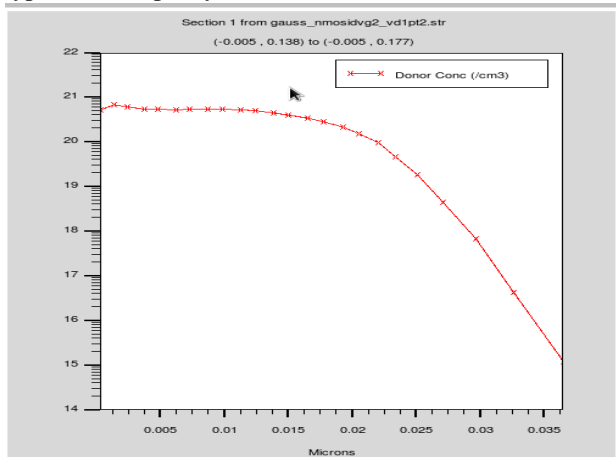
Where K denotes Boltzmann constant.

After simulation, the energy band diagram is shown in below Figure 5



**Figure 6 Conduction Band and Valence Band Energy V Donor Concentration:**

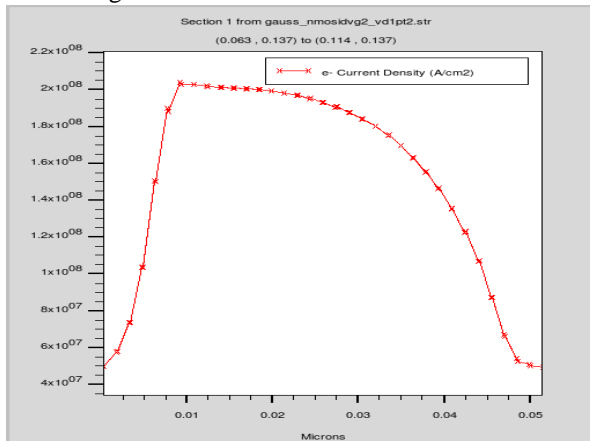
In NMOS, the channel is created to make electrons flow from source to drain. So a P type substrate is to be doped with n type donor impurity to make source and drain [8].



**Figure 7 Donor Concentration**

## V. ELECTRON CURRENT DENSITY :

When a voltage is applied at gate greater than threshold voltage and drain positive than source, electrons flow from source to drain. The electron current density after simulation of device is given below:



**Figure 8 Electron Current Density**

## VI. CONCLUSION

This paper concludes the theoretical and practical analysis of potential, threshold voltage and electron current density. From the analysis of theoretical and simulated results, potential is analysed at different doping concentrations, threshold voltage of 0.22V is achieved at 4.12eV work-function at 1nm gate oxide thickness which is the best value at 45nm technology according to ITRS guidelines. The threshold voltage can be adjusted by varying the threshold implant concentration during fabrication.

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Nitin Sachdeva is an Assistant Professor in Electronics Engineering Department at J.C. Bose University of Science & Technology, YMCA, Faridabad from January, 2007. She has completed her B.Tech in ECE from PTU, Jalandhar in 2003. She has completed his M.Tech. in VLSI Design & CAD from Thapar Institute of Engineering & Technology, Patiala in 2005. She has supervised 20 M.Tech Thesis and Projects. She has published several papers in various National & International Conferences/Journals. She is pursuing Ph.D in the field of VLSI Design from YMCA UST, Faridabad (Haryana).



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