A Wavelet architecture for Abdominal ECG preprocessing and fetal QRS detection implemented in FPGA using 90nm technology

Radha Abburi, M. Asha Rani

Abstract*: During labor ECG Monitoring is one of the most used method to determine the condition of the fetus. The type of monitoring varies from patients to patients. Few require continuous monitoring because of medication while others require only intermittent monitoring. The fetal ECG is the only information source in early stage diagnosis of fetal health and status. This paper describes the implementation of a system based on FPGA which denoises the abdominal ECG and separates the Fetal ECG from the abdominal signal. For preprocessing a VLSI hardware in FPGA for wavelet transform method is designed and implemented. The embedded architecture on FPGA is based on quadrature spline wavelet transform. FPGA implementation of quadrature spline wavelet transform filter was done with different multipliers. The extraction of fetal electrocardiogram signal was done using slope threshold and two stage template search method where the fetal ECG is extracted from the abdominal ECG. The logical elements, power and delay for the proposed architecture is reported in this paper. For implementation Cyclone II kit and Quartus software was used. In future the classification method will be implemented.

***Keywords* : Fetal ECG, FECG extraction, Template matching, Wavelet Transform, QSW.**

I. INTRODUCTION

Current VLSI technologies have improved the biomedical SoC designs for numerous diagnosis and treatment process. The main challenges are complex computing block design, speed and power consumption. The FPGA based biomedical system design takes less time to convert from concept to production. The flexibility and readymade prototype verification through iteration makes the work to be implemented in FPGA. As the latest FPGA contain embedded processors and memory building a fetal monitoring system will be easier and efficient. But the devices have low capacity and consume more power. To avoid these issues the development is carried out using optimized architectures. The work is focused on the design of architecture for abdominal ECG signal processing and Electrocardiogram (ECG) feature extraction. The optimization is carried out on the design of the multiplier. The need for abdominal ECG preprocessing arises since the signal consists of low amplitude voltages in the presence of high offsets and noise. Various noise sources affect the abdominal signal due to half cell potential developed at the electrodes, power line interference, and instrumentation noise. The maternal ECG is the dominant signal which should be removed to extract the fetal ECG signal. In past years several ECG signal analysis methods were gained momentum with tremendous amount of work being carried out in different fields.

A mECG removal technique (Vullings et al (2007)) [1] based on dynamic segmentation of the mECG and subsequent linear prediction of the mECG may be better in simulations when compared to the performance of spatial filtering and signal correlation technique. It reduces the artifact sensitivity towards MECG removal. Kezi Selva Vijila et al (2006) [2] presented a Adaptive noise cancellation (ANC) based on neuro fuzzy logic technique (ANFIS). Simulation results alone was presented using ANFIS and comparison of its output with other techniques with sine wave as bench but no real time data was used. The only advantages is the technique has adaptation ability to the changing environment, low signal distortion and low output noise. Taralung et al (2007) [3] proposed a algorithm for smooth extraction of the QRS complex containing the most disturbing energy of the mECG. The noise removal process reaches a stable solution only after a longer time when BSS is used. For extraction more number of electrodes is required and the method is hard to implement in hardware. Even though in simulations BSS shows a more robust, superior performance in the problem of FECG extraction from maternal cutaneous recordings, the hardware implementation is too complex (Zarzoso et al (2000)) [4]. ICA (Ruben Martın Clemente et al (2011) [5] and J. L. Camargo Olivares (2011)) [6] reduces the dimensions and makes the computations simple. Similar to BSS the ICA have problem in convergence. Array signal processing (Masoumeh Haghpanahi and David A Borkholder (2011)) [7] have very good convergence behavior but failes in phase alignment of R-peaks.

Vigneron et al (2003) [8] proposed an ICA and Wavelet based denoising to remove maternal signal and reduce motion artifacts. The extraction performance is good only when there are more number of electrodes involved (5 atleast), which is practically difficult during labor it's impossible. The nonlinear dependency of maternal ECG on abdominal ECG is utilized for the estimation of V-SVR (Liang Han et al (2015)) [9]. The estimated maternal component is subtracted from the abdominal ECG to get the fetal ECG. The extraction process is faster when there is no phase difference. M A Hasan et al (2009) [10] used a neural network based Fetal ECG extraction from Maternal Abdominal ECG.

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Different learning constants were utilized where complex problems can be solved. Training and testing patterns is selected properly the extraction is easier. Implementation in hardware is complex. Consumes more memory since it's iterative. Time consuming to make proper training and testing vectors. Mohammad Niknazar et al (2013) [11] proposed a extended state kalman filtering fetal ECG extraction on single-channel recordings. But this method detects only R-peaks, other features are not extracted. The time to reach the accuracy is more. Shuicai Wu A et al (2013) [12] extracted the featl ECG using wavelet and adaptive filters. Compared to fourier analysis and time series analysis the wavelet transform is advantages in quantifying the signal features. The method analysis both the time and frequency functions of the QRS complex. Not only quantifies the features but specifies the exact positions of the features. The adaptive digital signal filtering method to extract fetal ECG from noisy measurement is accurate and no separate coefficient file is required for filtering. The coefficients are updated by it for every step. RLS and LMS algorithms are advantages in its own way. Easy to implement when compared to BSS, ICA methods. A new mother wavelet has to be designed similar to the shape of the QRS complex of maternal and fetal. The hard and soft thresholding range should be predetermined based on the frequency of the noise component for denoising and QRS component for extraction. If measured signal were corrupted by high amplitude of noises, detected heart rate profiles were noisy and hard to evaluate. The adaptation time is higher for more noise environment. Catherine and Tressa (2013) [13] implemented a FPGA based correlator to detect the QRS wave of the ECG signal. But reference mismatch happens detection will be error. Indranil Hatai et al (2013) [14] proposed a FPGA based fetal heart rate monitoring using adaptive filters. Even though the coefficient block is eliminated the design suffers from convergence factor and proper reference is required. Muhammad A. Hasan et al (2009) [15] modeled a VHDL based artificial intelligence system for extraction. But the complexity in implementation is more and accuracy is not met due to modeling and not a real design. Dheyaa Alhelal et al (2015) [16] proposed a FPGA based denoising method using FIR filter. Power line interference was removed. Removes the noise and detects the beats. Simple to design compared to Adaptive and BSS. Accuracy is less. More taps required for removal of noise completely.

II. BACKGROUND METHODOLOGY

A. QRS Detection Methods

There are many methods for a reliable QRS recognition and interpretation of the 12-lead ECG (Jiapu Pan and Willis (1985)) [17] using computers is a popular technique. For several years' arrhythmia monitors, Holter scanning devices were used. The analysis of the ECG is widely used for diagnosing (Juan Pablo Martinez et al (2017)) [18] cardiac diseases. The automatic delineation of ECG has been widely researched. QRS detection algorithms and wave delineation algorithms proposed in the last decade presents a two-stage architecture with preprocessing stage as first stage with including linear filters followed by a nonlinear transformation and the second stage is the decision rule. The different delineation approaches discussed in previous section are matched filters, Adaptive filters, the wavelet transform (WT), nonlinear time-scale decomposition, artificial neural networks and BSS. When few algorithms can extract the ECG characteristic points in detail the others can do only time analysis.

B. Conventional Heart Beat Extraction

Yozaburo Nakai et al (2015) [19] presented an R-wave detection using threshold determination which is widely used approach for heart rate detection from ECG. The well known Pan–Tompkins (PT) algorithm for adult ECG based on slope thresholding using band-pass filtering, differentiation, squaring, and moving window integration is less efficient for abdominal signal analysis. The Quad Level Vector (QLV) algorithm (Hyejung Kim et al (2010)) [20] uses DWT and the adaptive threshold by the maximum mean deviation (MD) of the previous heartbeats to evaluate the adult ECG. A general approach used for extracting R-waves is Threshold determination. Various statistical methods have been proposed for calculating the threshold of noise-tolerant. However, the problems of false detection and misdetection due to various noise signals from various sources like myoelectric signals generated from muscles, movements of electrodes due to power utilization and the distance of the electrode from the wearable system along with its volume and weight are increasing in wearable healthcare systems. To eliminate these errors and to make the system more robust we need algorithms that can prevent false detection and the most reliable algorithms available are autocorrelation and template matching which uses the QRS of the complex waveforms for measuring the similarity index and these algorithms do not have any process of threshold calculation. The limitation of the Autocorrelation is that this method requires a lot of computations to calculate average heart rate over a period of 30s and it can been used only in non-invasive monitoring systems.

C. Problems Identified

- A periodic threshold adjustment using QRS morphology and the heart rate will give efficient analysis.
- The hardware of the algorithm was implemented using conventional circuits like adders, shift and add multipliers and Accumulator. The area and power is higher.
- The existing methods use conventional Embedded Multiplier which are bulky and more power consuming.
- The methods like blind source separation and adaptive filters suffer from large memory size and convergence problem.
- FPGA based design are done for only adult ECG analysis which cannot` be used for fetal ECG analysis.
- FPGA implementation of Fetal ECG classification was not available in literature.

III. EXISTING ARCHITECTURES FOR MULTIPLIERS

A. Baugh Wooley Multiplier

The architecture of the Baugh wooley multiplier to perform unsigned multiplication is shown in figure (1). The structure based on Baugh wooley algorithm (Vishal Shankarrao et al (2015)) [21] is suitable for both regular multiplier and 2's complement number.

Effective when FPGA is used with AND terms, half-adders and full-adders with carry outs chained to the next MSB at each level of addition. The multiplier will be suitable for the block used for QRS detection.

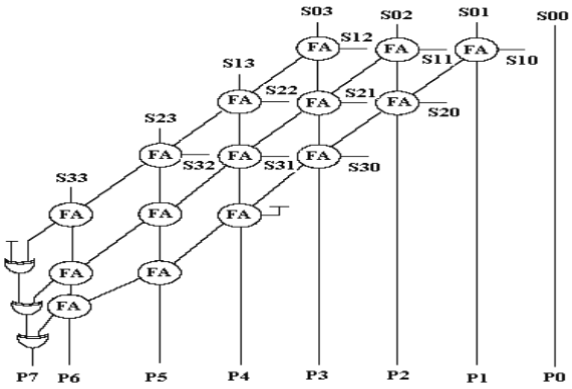

Fig. 1 Architecture of Baugh Wooley Multiplier.

B. Braun Multiplier

Braun multiplier is the simplest parallel multiplier. Cascaded carry save adders collect the computed partial products and these partial products are computed in parallel. Propagation time and depth of the carry save adder limits the completion time. Braun multiplier (Madhu Thakur and Javed Ashraf (2012)) [22] is only suited for positive operands. Unsigned multiplication based on Braun algorithm structure is shown in the figure (2).

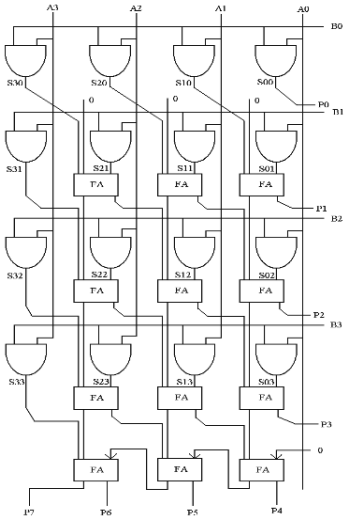

Fig. 2 Architecture of Braun Multiplier.

C. Wallace Tree Multiplier

The rearranged tree structure of partial-sum adder reduced the requirement of number of adder cells and critical path. For larger multiplier the tree like fashion saves the substantial hardware realization and reduces the propagation delay. The propagation delay of the tree structure is equal to O (log 3/2 (N)). For larger multiplier word length it's substantially faster compared with carry save adder. The structure of 4 bit Wallace tree multiplier is shown figure (3).

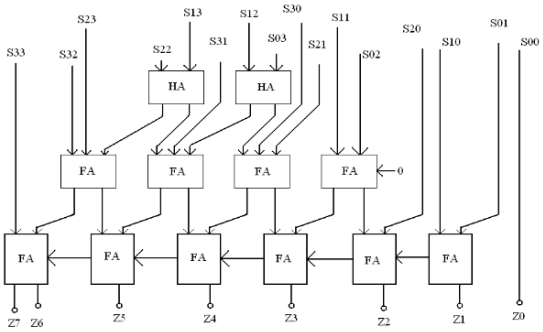

Fig. 3 Architecture of Wallace Tree Multiplier.

IV. PROPOSED METHODOLOGY

A. Proposed algorithm for FPGA Implementation

The proposed FPGA implementation of a hybrid algorithm combining the efficiency of wavelet transform and template matching. The proposed methodology achieves good reasoning in quality and quantity. Wavelet based extraction extracts the features of the fetal information from the abdominal ECG The block diagram of the proposed FPGA implementation is shown in figure (4).

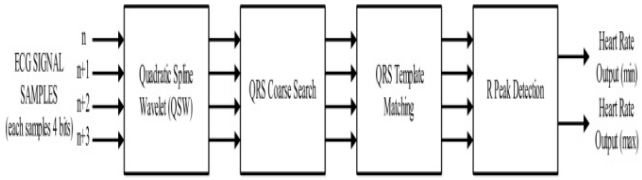

Fig. 4 Block diagram of fetal ECG extraction.

In general QSW method is used to reduce the low-power noise in ECG signals. By using this method we can efficiently suppress the hum-noise and baseline wandering. QSW and QRS complex operates at the same frequency making the QSW alone very difficult to remove the noises generated by QRS solely. For this purpose a FIR filter with impulse response of prototype quadratic spline wavelet is proposed for the fetal ECG analysis.

$$H[n] = 1/8.\{\delta[n+2] + 3\delta[n+1] + 3\delta[n] + \delta[n-1]$$

$$G[n] = 2.\{\delta[n+1] - \delta[n]\} \quad (1)$$

The wavelet based approach for ECG delineation is a differentiator filter bank approach. The block diagram of the proposed QSW block for abdominal ECG signal denoising is given in figure 5. The implemented FPGA consists of various blocks like Summer, Subtractor, registers, and accumulators.

B. Multiplier Accumulate Unit for the proposed QSW Block

The Multiplier- Accumulator (MAC) operation is the key operation in the implementation of the algorithm. MAC unit consist of various multiplier, adder and an accumulator. In this paper, we used various multipliers like array, vedic braun, baugh wooley etc. The MAC inputs for the multiplier block are obtained from the memory location which is having 8 bits of data.

Once the multiplier is fed with the 8 bit input it starts computing value for the given input and a 16 bit output will be generated.

The multiplier in figure (5) is replaced with different types of multiplier architecture. Output is given to the remaining blocks.

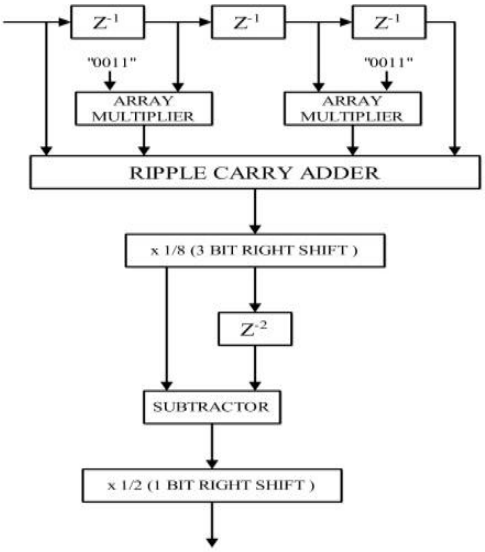

Fig. 5 Block Diagram of QSW.

C. Array Multiplier

Array multiplier is very familiar because of its regular structure. Array multiplier structure (Priyanka Srivastava et al (2013)) [23] is working based on repeated addition and shifting principle. The multiplication of each multiplier digit with multiplicand generates a partial product. Those partial products are added, before it is shifted into their bit sequence. A normal carry propagation adder is used to perform the summation. In array multiplier, N is the no. of multiplier bits; N-1 adders are required for implementation. The architecture of vedic multiplier is shown in figure (6).

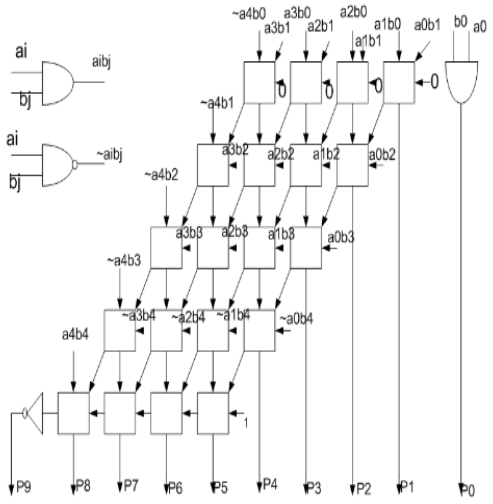

Fig. 6 Architecture of Vedic multiplier.

D. Vedic Mathematics based multiplier

Vedic mathematics is based on sixteen sutras. The Vedic multiplier implemented for the QSW block is based on only one sutra "Urdhva Tiryakbhyam". Pratyusha Chowdari et al (2016) [24] The technique is faster and based on "vertically and crosswise". For the implementation of 2X2 Vedic multiplier, the AND operation is used for 1-birt multiplication and the half adder structure is used for two bit multiplication. The carry of the half adder is taken as one input of next half adder. The structure of 2X2 Vedic is shown figure (7).

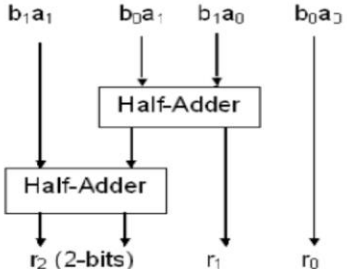

Fig. 7 Block diagram for 2X2 Vedic Multiplier.

Here, r0 and r1 (1 bit), r2 (2 bit);

$$r0 = a0.b0$$
$$r1 = a0.b1 + a1.b0$$
$$r2 = b1.a1 + c1 \quad (2)$$

Even though the different multipliers have different features, in this paper the comparison is made on the power delay and area.

E. Proposed QRS detection

The instantaneous ECG samples which consists of 8 bits of data enters this block after successful removal of noise from the QSW filter. These samples without any noise are sent for comparison of QRS template to course and fine search blocks.

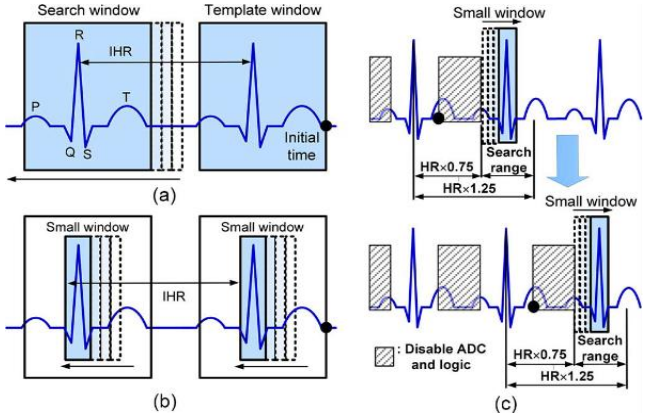

Fig. 7 Overview of coarse-fine QRS template generation and template matching with QRS prediction. (a) Coarse QRS search. (b) Fine QRS search. (c) Template matching.

F. Coarse search and Fine search block

Here separate blocks are done for fetal and maternal separation. But the working is same. For the template four constant data (each 8 bit) is chosen as "Fetal template" and "Maternal Template" for fetal and maternal (figure (7)). The input 128 bit data is compared with the "Fetal template" and "Maternal Template".

For that we have splited the 128 bit data into 16 bytes. Each byte from 128 bit is compared with “Fetal template” and “Maternal Template”. If the byte is matched with anyone of that particular “Fetal template” and “Maternal Template” then Z becomes high, otherwise Z becomes low. This process continued till all 16 bytes is compared with the “Fetal template” and “Maternal Template”. If the value of Z is zero at the end then the fetal and maternal is occurred, the output display as high (1111111111111111) is any maternal or fetal is occurred. Otherwise the fetal (or maternal) is not occurred, the output display as low (0000000000000000).)

Fine search: The above operation is done again but with highest accuracy to make the template matching perfect.

G. R-Peak Detection and Heart rate analysis.

The heart rate is measured by detecting the R-Peaks. The heartbeat detector will have a sampling frequency rate of 360 Hz. The QRS waveforms are specific for each patient and are labeled as the original QRS templates. The original templates are updated continuously by the other heartbeat signals which are satisfying the conditions of template matching and waveform similarity. On completion of every iteration the waveforms of the three original QRS templates of the training heartbeats are changed. Therefore QRS templates are modified with respect to patient values. The positive peak in the QRS region is termed as R peak. These R peaks are detected by comparison of the relative magnitude in each QRS waveform. To eliminate errors in baseline a maximum search is done on the relative magnitudes for each window. In each window of the QRS waveform the maximum and minimum amplitude values are calculated for the ECG data array. The wavelet transforms are used for the extraction of feature vectors and are applied to SVM classifier as input in future.

V. RESULTS AND DISCUSSION

A. Implementation of QSW with Various multipliers

The parameters of the QSW implementation with vedic and Wallace tree Multiplier are shown in table (1) and (2) respectively. The table represents the performance based on area-logic elements, power and delay for four different devices namely the Cyclone II, III, Stratix II and III. The comparison chart is presented in figure (8) and (9).

Table 1 Parameter analysis of QSW with Vedic Multiplier.

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
Logic Element	6071	6056	5760	5846
Power	196.38mW	115.86mW	378.59mW	465.59mW
Time	16.666nS	13.704nS	14.687nS	12.366nS

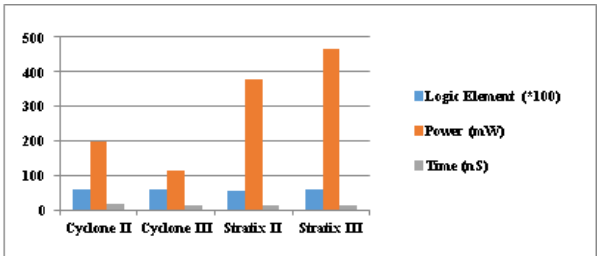

Fig. 8 Parameter analysis of QSW with Vedic Multiplier.

Table 2 Parameter analysis of QSW with Wallace tree Multiplier.

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
Logic Element	5750	5316	5029	4930
Power	113.90mW	98.50mW	348.33mW	442.69mW
Time	17.379nS	15.403nS	13.434nS	10.998nS

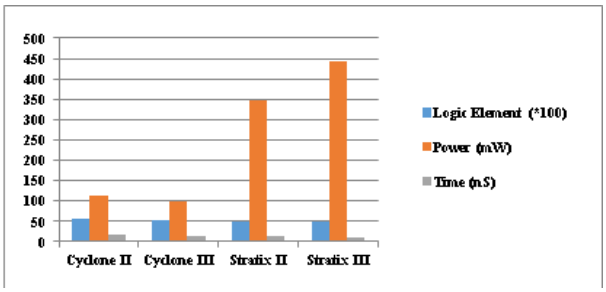

Fig. 9 Parameter analysis of QSW with Wallace Tree Multiplier.

The Implementation of QSW with Braun multiplier and array multiplier is presented in table (3) and (4) respectively. The respective comparative charts are presented in figure (10) and (11).

Table 3 Parameter analysis of QSW with Braun Multiplier.

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
Logic Element	6500	6413	5413	5383
Power	115.22mW	99.70mW	350.35mW	445.29mW
Time	15.792nS	13.135nS	12.506nS	9.662nS

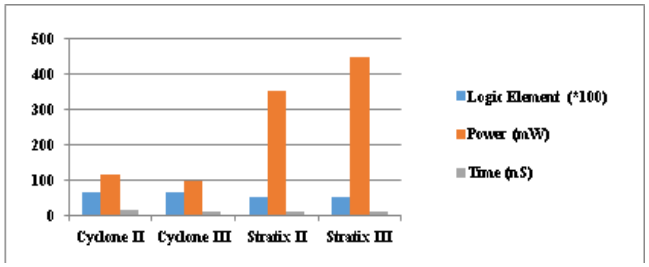

Fig. 10 Parameter analysis of QSW with Braun Multiplier.

Table 4 Parameter analysis of QSW with Array Multiplier.

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
Logic Element	4693	4700	4561	4544
Power	118.08mW	102.14mW	357.42mW	450.44mW
Time	19.144nS	15.658nS	13.426nS	10.684nS

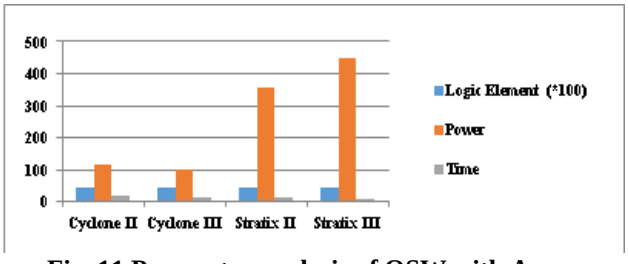

Fig. 11 Parameter analysis of QSW with Array Multiplier.

B. Implementation of Feature Extraction and heart beat block

The performance analysis of feature extraction and heart beat detection block is presented in table (5) and (6). The charts in figure (12) and (13) represent the performances.

Table 5 Parameter analysis of Feature Extraction.

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
Logic Element	87	86	78	78
Power	73.21mW	64.11mW	463.39mW	461.95mW
Time	15.286nS	7.914nS	7.914nS	6.390nS

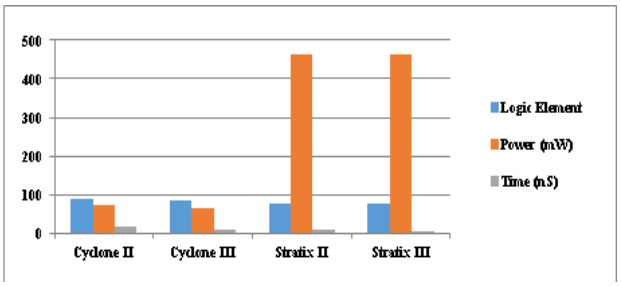

Fig. 12 Parameter analysis of Feature Extraction.

Table 6 Parameter analysis of Heart Beat Detection.

Parameter	Cyclone II	Cyclone III	Stratix II	Stratix III
Logic Element	485	486	401	400
Power	36.37mW	60.86mW	325.65mW	400.79mW
Time	10.538nS	8.156nS	7.772nS	7.194nS

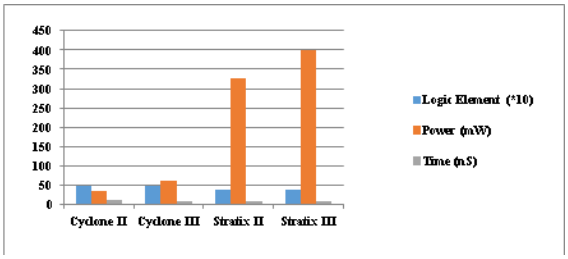

Fig. 13 Parameter analysis of Heart Beat Detection.

The comparative analysis of various multipliers in QSW with respect to logic elements, power and delay are presented in figures (14), (15) and (16) respectively.

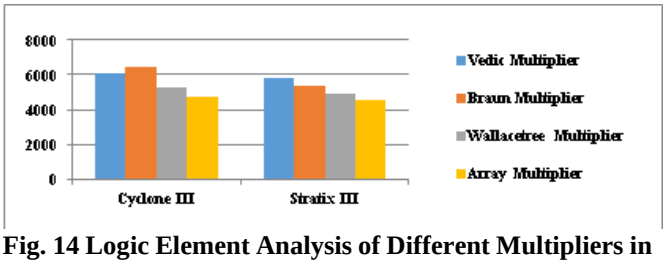

Fig. 14 Logic Element Analysis of Different Multipliers in QSW.

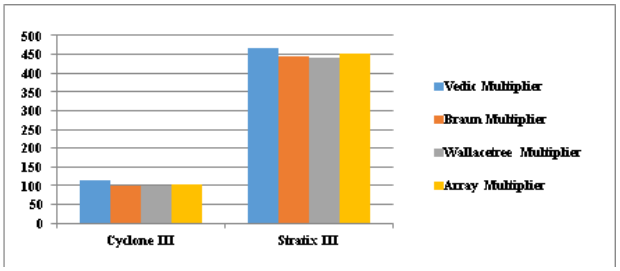

Fig. 15 Power Analysis of Different Multipliers in QSW.

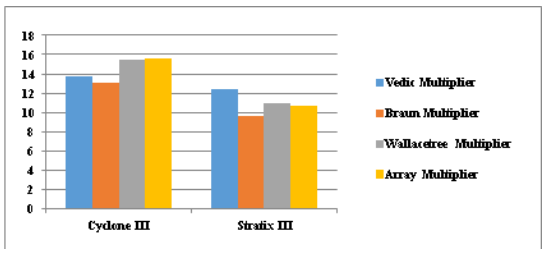

Fig. 16 Time Analysis of Different Multipliers in QSW.

VI. CONCLUSION

The objective of the work for designing a Heart beat detector for a fetal ECG monitoring is met. The novel architecture for the heart beat detector with wavelet block stands unique in its architecture. The heart beat detection proposed in this project contains adder and different multiplier as its main processing elements and it gets the data as binary input. The coarse search and template matching is been done followed by minimum and maximum finding. Power area and delay analysis of different block are done and analyzed. In the near future the other blocks of the chip will be implemented and combined.

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