Novel Technique To Implement Low Power Differential Delay Cell Ring VCO With Variable Centre Frequency

Shitesh Tiwari, Sumant Katiyal, Parag Parandkar

Abstract: Ring VCO with variable center frequency incorporating the design of differential delay cell working at low power is illustrated in the current research work. Concept of variable frequency with low power consumption is a novel VCO implementation technique. A differential delay cell is used to generate variable frequency to design a ring VCO at 32 nm technology operated at 1.2 V supply power voltage to achieve low power and low phase noise characteristics. Five stage ring VCO is designed with switches, to ensure that one stage works at a time, keeping two stages off. This switching of stages is dependent on the desired frequency of operation by the VCO. The proposed research work also facilitates the additional computation of width and length of PMOS and NMOS transistor along with the computation of optimal parameters. At 1 MHz offset frequency, the proposed VCO achieves phase noise of -105.53 dBc/Hz with minimum power consumption of 1 mW. The proposed VCO is poised to act as a major building block of a multi-standard wireless communication system such as GSM, Blue tooth, and 802.11g ZigBee applications.

Keywords: Center frequency; Current mirror; Digital phase locked loop; Dynamic power dissipation.

I. INTRODUCTION

Many researches have been carried out to achieve the goal of low power consumption with a centre frequency. An output frequency is generated by VCO in response to input applied voltage. The range of the frequencies which VCO can generate for applied voltage is decided by voltage to a frequency conversion factor of VCO which is an important parameter and is given by:

\[ K_{VCO} = 2\pi (f_{max} - f_{min})/(V_{max} - V_{min}) \text{ (radians/s.V)} \]

(1)

Where \( K_{VCO} \) = Gain, \( f_{max} \) & \( f_{min} \) are the maximum and minimum frequencies respectively.

\( V_{max} \) & \( V_{min} \) are the maximum and minimum control voltages respectively.

Ideally control voltage of the VCO should vary with the output in a linear manner, but the linearity is obtained over a very limited range in practice. Variation in delays offered by differential delay cells is the root cause for the non linearity incurred for some range of voltages. Typically for any configuration of VCO, in the ideal case, single output frequency is expected for a fixed control voltage. But practically, for a single voltage, there exists small band of frequencies.

1.1. Differential Ring VCO

The ring VCO configuration is one of the most popular VCO configurations pertaining to the benefits in terms of better immunity to common mode noise, spectral purity and provide 50% duty cycle [1]. Each delay cell in this VCO consists of two NMOS transistor, which accept input from the previous stage and four PMOS transistors, out of which two transistors (inner side) are responsible for controlling frequency on the application of control voltage and two (outer side) acts as pre-charge transistors. Increase in number of stages gives rise to enhancement of power dissipation. The proposed design varies the central frequency based on the output frequency requirement by targeting different number of stages.

Fig. 1: Circuit schematic of a Differential delay cell

As depicted in Fig. 1, the differential delay cell serves the purpose of ring oscillator and the current sources surrounding it limit the current available to the cells. Following equations are used to design the proposed VCO [2].

The output frequency is given by

\[ f = \frac{\beta \cdot (V_c - V_t)^2}{2 \cdot N \cdot C_{eff} \cdot V_c} \]

(2)

Where \( f \) is the required oscillation frequency, \( N \) is the number of delay cells, \( C_{eff} \) is the effective capacitance, \( \beta \) is process parameter, \( V_c \) is control voltage, \( V_t \) is threshold voltage of PMOS transistor.

From equation 2, W/L ratio of PMOS transistor can be calculated as,

\[ f = \frac{1}{2 \cdot N \cdot t_{delay}} \]

(3)

Where, \( t_{delay} \) is the delay of each cell.

\[ t_{delay} = R_{eff} \cdot C_{eff} \]

(4)

Where, \( R_{eff} \) is effective resistance given by

\[ R_{eff} = \frac{V_{loadmax}}{I_{loadmax}} \]

(5)

Where, \( V_{loadmax} \) is maximum load voltage and \( I_{loadmax} \) is maximum load current.
\( C_{eff} = K \cdot C_{ox} \cdot (W_{nmos} \cdot L_{nmos} + W_{pmos} \cdot L_{pmos}) \)  

\[ ... \]

Where, \( K \) is the gain of the VCO, \( C_{ox} \) is oxide capacitance, \( W_{nmos} \) and \( W_{pmos} \) are the width of PMOS and NMOS transistor respectively and \( L_{nmos} \) and \( L_{pmos} \) are the length of NMOS and PMOS transistor respectively.

Equation 6 is used for calculation of W/L ratio of NMOS. After this, the next important performance parameter of VCO called as phase noise is evaluated. Phase noise is defined as the ratio of the noise at 1-Hz bandwidth at a specified frequency offset, \( \Delta f \) to the oscillator signal amplitude at frequency \( f_c \).[3]

\[ l(\Delta f) = 10 \log \left( \frac{2 \pi \cdot f_c}{\Delta f} \right) \times \left( \frac{f_0}{\Delta f} \right)^2 \]  

Where \( P_{min} \) is the minimum power dissipation of ring oscillator that is proportional to the parasitic capacitance value and the square of the bias voltage. From this, figure of merit can be calculate as

\[ FOM = l(\Delta f) - 20 \log \left( \frac{f_c}{\Delta f} \right) + 10 \log \left( \frac{P_{min}}{1mW} \right) \]  

where \( l(\Delta f) \) is the measured phase noise in dBC/Hz at a frequency offset of \( \Delta f \) from the carrier frequency \( f_c \) and \( P_{min} \) is the measured power dissipation of the oscillator in milliwatts.

After the introduction about Differential cell ring VCO the rest of the paper is organised in the following three sections. First section has already covered the introduction. The second section II section elaborates power dissipation within the VCO. The third section throws the light on the survey of related literature. The forth section proposes the naive method for the design of low power driven VCO and discusses the factors influencing power dissipation. The fifth section presents the simulation results and related discussion. The last section concludes the proposed work.

II. POWER DISSIPATION OF VCO

Major component of power dissipation in the differential VCO is due to the ring oscillator whose frequency is given by

\[ F = \frac{I}{N} \times (t_{phl} + t_{phh}) \]  

Where, \( t_{phl} \) is the high to low delay time period and \( t_{phh} \) low to high delay time period. The minimum delay occurred into every stage of ring oscillator lies on the size of the transistor and process parameters. Hence the each stage is influenced by the complete ring directly or indirectly. At the center frequency, the control voltage applied to the VCO is equal to half of the power supply voltage, \( V_{dd} \). It is mathematically represented as

\[ F = F_{center} \text{ When } \left( V_{invco} = V_{dd}/2 \right) \]  

\[ I_{Dcenter} = I \text{Dcenter} \]  

Where \( V_{invco} \) is the control voltage applied to the VCO. VCO stops oscillating when control voltage is less than threshold voltage of MOSFET and this condition is given by

\[ V_{min} = V_{thn} & F_{min} = 0 \]  

2.1. Estimation of average power dissipation of VCO

The average power dissipation of the VCO can be calculated as

\[ P_{avg} = V_{DD} \times I_{avg} \]

\[ P_{avg} = V_{DD} \times N \times V_{DD} \times C_{load} \times f_{osc} \]

As the VCO works on the operational principle of ring oscillator, its power dissipation can be estimated by equation (12). The method of estimating power dissipation is similar to that of a current starved (inverted based) ring oscillator but in addition to that current mirror based on MOSFETs will also dissipate power so the power is doubled[12].

III. LITERATURE SURVEY

Xueimei Lei and his friends[4] designed ring VCO on 180 nm technology which generates frequency range from 75 MHz to 6.9 GHz and also shown better phase noise when control voltage is higher. They obtained these results by applying control voltage at the gate of MP4 and MP5 instead of MP3.

Shweta Dabas, Manoj Kumar[5] obtained frequency range from 1.004 GHz to 2.875 GHz by designing three and five stage digital controlled oscillator. In this VCO, they place NMOS network in between \( V_{dd} \) and inverter cell in which gate is controlled digitally.

Prachi Gupta, Manoj Kumar[6] shown various load inverter based ring oscillator for three stages, four stages and five stages. They concluded that unsaturated load and pseudo NMOS load inverter is better choice for ring oscillator because they have better tuning range as compared to saturated and linear load inverter based ring oscillator.

Joshapath Johnson, Maran Ponnambalam and Dr. Premanand Venkatesh Chandramani [7] compared single ended and differential ended injection locked based VCO for 1.5-3.1 GHz frequency range. They also proved that although single ended require less number of transistors to design VCO but differential ended VCO is better than single ended because it can suppress harmonics better than the single ended.

C. Zhang, Z. Li, J. Fang, J. Zhao, Y. Guo, and J.Chen [8] employed inductive peaking technique with active inductors. In addition, a PMOS pair with gate connected to ground is added to increase oscillation frequency and linearity of VCO. They obtained phase noise of -86.7 dBc/Hz at 1 MHz offset.

Jail1, M.B.I.Reza, M.A.M.Ali, and T.G.Chang [9] designed three stage ring VCO for RFID transponder which included PMOS transistor with fixed value capacitor. From this design, they achieved oscillation frequency of 2.2-
2.85 GHz with phase noise of -112 dBc/Hz at 10 MHz offset.

Aditya Dalakoti, Merritt Miller and Forrest Brewer [10] design ring oscillator using one OR gate block and eighth pulse buffer to generate frequency of 513 MHz to 2.64 GHz. They also shown lower phase noise and better figure of merit with this architecture.

J.K.Panigrahi, D.P.Acharya[11] use basic architecture of delay cell to design two and three ring VCO and achieved phase noise of -90.01 dBc/Hz at 1 MHz offset. This ring oscillator oscillates in the range of 1.22-3.22 GHz.

4. Design for Low Power
The low power design of a VCO is comprehended by the following techniques:
- Power supply voltage reduction.
- Low frequency operation or reduction in transitions.
- Disabling part of the circuit which is not required at a particular instant.

The various low power VCO designs use techniques no. 1 and 3. Frequency dependent approaches depends on the application. In general, when voltage is decreased, the corresponding threshold voltage for logic levels also decreases, which leads to the reduction in noise margin. But by decreasing the threshold voltage this drawback can be avoided. This is done by applying better fabrication techniques.

When the PLLs and VCOs work with Non Return to Zero (NRZ) data patterns, VDD & VSS of circuit are choosen as differential and the levels of the signal can be distinguished clearly. Hence, the supply voltage of VCO is chosen as 1.2 V.

The average power dissipation depends on the number of stages as given in equation (12). When the VCO starts working, unnecessary power dissipation can be avoided by switching OFF those stages which are not required for operation and turning ON those stages which are essential for specific frequency generation. The number of stages which are not in use are switched OFF by using MOS-Switches. And feedback path is also switched off for those stages. Multiple feedback paths are used, out of which depending on the required frequency only the essential feedback path is chosen and rest are maintained OFF. The particular switch is used to select the feedback path. Based on the required path the selected line is enabled.

Fig. 2 shows the basic block diagram of variable centre frequency VCO. The center frequency will also vary with variable number of stages (N) in VCO. Fig. 3 shows the transistor level schematic of the variable center frequency VCO. The stages are switched ON and OFF to vary the number of stages required for operation of VCO using reliable switches. Switches are designed by using MOS Transmission gates. Mux 2x1 is the basic building block of a transmission gate. To select particular feedback path, the CMOS switches are connected represented in Fig. 3 for multiplexing.

Fig. 2 : Block diagram of five stage ring VCO

Fig. 3 : Circuit schematic of variable frequency ring VCO
IV. RESULTS & DISCUSSION

Based on the different transient test conditions, the circuit is simulated using T-Spice. Table 5.1 demonstrates the comparison of frequency versus tuning voltage for 3, 4 and 5 stages. It also shows band of frequencies each stage is capable of generating. Moreover, some frequencies are generated with the help of using 3 stages or using 4 stages or by using 5 stages. Minimum frequency generated is 690 MHz while maximum frequency generated is 5.56 GHz.

It is investigated that number of stages is directly proportional to the power dissipation. Also the design makes this flexibility to take variable number of stages at a given time. So the power dissipation will also vary accordingly. Table 2 shows the variation of power with the number of stages.

Table 1: Comparison of Frequency vs Tuning voltage for 3, 4 and 5 stages

<table>
<thead>
<tr>
<th>$V_{tune}$ (V)</th>
<th>Frequency (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Stage 3</td>
</tr>
<tr>
<td>0.5</td>
<td>2.17</td>
</tr>
<tr>
<td>0.6</td>
<td>1.92</td>
</tr>
<tr>
<td>0.7</td>
<td>2.04</td>
</tr>
<tr>
<td>0.8</td>
<td>4.54</td>
</tr>
<tr>
<td>0.9</td>
<td>5.56</td>
</tr>
<tr>
<td>1</td>
<td>5.56</td>
</tr>
</tbody>
</table>

Table 2: Comparison of Power dissipation vs Tuning voltage for 3, 4 and 5 stages

<table>
<thead>
<tr>
<th>$V_{tune}$</th>
<th>Power Dissipation (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Stage 3</td>
</tr>
<tr>
<td>0.5</td>
<td>0.399</td>
</tr>
<tr>
<td>0.6</td>
<td>0.552</td>
</tr>
<tr>
<td>0.7</td>
<td>0.71</td>
</tr>
<tr>
<td>0.8</td>
<td>0.951</td>
</tr>
<tr>
<td>0.9</td>
<td>1.17</td>
</tr>
<tr>
<td>1</td>
<td>1.27</td>
</tr>
<tr>
<td>1.1</td>
<td>1.28</td>
</tr>
</tbody>
</table>

In a differential VCO, the generation of frequencies is decided by number of stages. The value of frequency generated is inversely proportional to number of stages. More are the stages, lesser is the value of frequency that they can generate. Another advantage of using this VCO architecture is that it is capable of generating more than one frequency as well, in the form of a frequency band. Therefore, two unmatched, but close frequencies can be generated, that helps PLLs the capability to distinguish two close frequencies. The VCO linearity lies upon the linearity of the applied voltage to the input.

Table 3 shows parameter performance variation with application of 3, 4 and 5 stages.

Table 3: Performance variation with 3,4 and 5 stages

<table>
<thead>
<tr>
<th></th>
<th>Three</th>
<th>Four</th>
<th>Five</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency range(GHz)</td>
<td>1.92-5.56</td>
<td>0.96-3.12</td>
<td>0.69-2.17</td>
</tr>
<tr>
<td>Phase Noise(dBC/Hz) at 1MHz offset</td>
<td>-98</td>
<td>-98.35</td>
<td>-98.73</td>
</tr>
<tr>
<td>FOM(dBC/Hz)</td>
<td>-206</td>
<td>-205.98</td>
<td>-205.99</td>
</tr>
<tr>
<td>Power consumption maximum(mW)</td>
<td>1.28</td>
<td>1.45</td>
<td>1.6</td>
</tr>
<tr>
<td>Power consumption minimum(mW)</td>
<td>0.399</td>
<td>0.433</td>
<td>0.472</td>
</tr>
<tr>
<td>Application</td>
<td>multi-standard wireless communication systems, Clock recovery system, WBAN, LTE, LTE, GSM, UMTS</td>
<td>multi-standard wireless communication systems, Clock recovery system, ISM Band, PLL, LTE, GSM, UMTS</td>
<td>multi-standard wireless communication systems, GSM, UMTS</td>
</tr>
</tbody>
</table>

Fig. 5 shows plot of transfer characteristic of a VCO architecture having three ON stages. This architecture imbines tuning range at 3.08 GHz and frequency ranges...
from 1.92-5.56 GHz. For more frequency generation number of stages in the VCO architecture needs to be altered.

![Plot of Transfer characteristics for 3 stage VCO](image)

**Fig. 5 : Plot of Transfer characteristics for 3 stage VCO**

The characteristics of VCO is simulated with 4 and 5 ON stages as shown in Fig 5.6 and 5.7 respectively. Fig 5.6 shows that a VCO with 4 ON stages can generate output frequencies from 0.96 GHz to 3.12 GHz. Fig 5.7 shows that VCO with 5 ON stages can generate output frequency from 0.69 GHz to 2.17 GHz. The proposed variable incorporation of number of stages in a VCO is aimed at choosing the optimum number of stages which reduce the power dissipation at its minimum. The power dissipation is significantly reduced by one third by reducing VDD, in general by incorporating differential VDD and VSS in VCO. Switching off presently unused circuit further results in remarkable reduction of power dissipation without addition of any additional hardware. Fig. 5.8 shows the characteristics of VCO is simulated with all 3, 4 and 5 ON stages. It shows that VCO frequency tuning ranges from 0.69-5.56 GHz.

![Plot of Transfer characteristics for 4 stage VCO](image)

**Fig. 6 : Plot of Transfer characteristics for 4 stage VCO**

![Plot of Transfer characteristics for 5 stage VCO](image)

**Fig. 7 : Plot of Transfer characteristics for 5 stage VCO**
Another important characteristic for the VCO is phase noise. Table 4 shows different values of phase noise obtained for the proposed VCO architecture having 3, 4 and 5 stages. From the table, it is evident that phase noise for third stage VCO is -98 dBc/Hz, for four stage VCO is -98.35 dBc/Hz and for five stage VCO is -98.73 dBc/Hz for 1 MHz offset frequency.

### Table 4: Phase noise(dBc/Hz) for all the stages

<table>
<thead>
<tr>
<th>Offset Frequency(Hz)/Stage</th>
<th>Three</th>
<th>Four</th>
<th>Five</th>
</tr>
</thead>
<tbody>
<tr>
<td>1K</td>
<td>-38.0011</td>
<td>-38.3562</td>
<td>-38.7308</td>
</tr>
<tr>
<td>10K</td>
<td>-58.0011</td>
<td>-58.3562</td>
<td>-58.7308</td>
</tr>
<tr>
<td>100K</td>
<td>-78.0011</td>
<td>-78.3562</td>
<td>-78.7308</td>
</tr>
<tr>
<td>1M</td>
<td>-98.0011</td>
<td>-98.3562</td>
<td>-98.7308</td>
</tr>
<tr>
<td>10M</td>
<td>-118.0011</td>
<td>-118.3562</td>
<td>-118.7308</td>
</tr>
</tbody>
</table>

Fig. 9, 10 and 11 shows the plot of phase noise vs frequency for 3, 4 and 5 stages.
Figure 9: Phase noise curve for three stages

Figure 10: Phase noise curve for four stages

Figure 11: Plot of phase noise vs frequency for five stages
6. Conclusion

Low power design of CMOS VCO with variable center frequency is widely illustrated in the proposed paper. The center frequency of the differential delay cell based VCO depends on the number of stages which is varied here to get variable center frequency design. The main circuitry containing the differential delay chain in the VCO is applied the lower supply voltage. Selective disabling of the various stages successfully contributes to lower the power dissipation and variable center frequency generation. The proposed Ring VCO consist of five stages. The stages are switched by using switches containing transmission gate and a inverter. For the proposed VCO, three stages gives frequency range of 1.92-5.56 GHz, four stages gives frequency range of 0.96-3.12 GHz and five stages gives frequency range of 0.69-2.17 GHz. Minimum power consumption of 0.399 mW, 0.433 mW and 0.472 mW is achieved for three, four and five stages respectively. Proposed VCO has been designed on Tanner eda using 32 nm technology operating at 1.2 V power supply voltage. The VCO shows phase noise of -98 dBc/Hz for third stage, -98.35 dBc/Hz for fourth stage and -98.73 dBc/Hz for fifth stage at 1 MHz offset.

REFERENCES