International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-3, September 2019

Symmetric Stacking Based Fast Binary Counter Using Modified Gate Diffusion Input (M-GDI) Technique

Pavani Ivaturi, N. Prasad

Abstract— In this paper, modified-Gate Diffusion Input (M-GDI) based binary counter is designed using symmetric stacking method. The binary counter is designed using 3-bit stacker circuit that groups the one bit together and symmetric method is used to form 6-bit stack. The 6-bit stack is converted to binary count to produce required counters. The M-GDI is used to further reduce the transistor count than the CMOS logic transistor count. Mainly the basic gates are developed using the M-GDI technique and the basic gates are replaced in the 6:3 counters to further improve counter-performance. The proposed 6:3 binary counter has no Exclusive or gate (XOR) gates on the critical path, which leads to faster performance of the circuit. The proposed counter is faster, also consumes less power than the traditional. By using this proposed counter in Wallace multiplier, the delay and power for higher-order multipliers is reduced.

This paper proposes a novel symmetric stacking based fast binary counters using the modified gate diffusion input (M-GDI) technique. This paper proposes a novel binary counter.

Keywords: Counters, Modified GDI, Stacker circuit, Wallace Tree

I. INTRODUCTION

Majority of applications require an efficient processor to perform the processing on a large amount of data [1]. Delay, power, and area are the main parameters which determine the performance of any circuit. The performance of the processor is increased by improving the performance of the multiplier block [1]. The multiplication process mainly includes partial product reduction, final carry propagation addition and partial product generation [1]. The power consumption and delay of the multiplier is determined by the partial product reduction.

Various counters have already been proposed in the literature for the better performance of the partial products reduction stage [2-5]. Full adder circuits are used in the full adder-based counters to construct the 6:3 counter [2]. The delay increases in the higher-order counters due to the presence of the XOR gates in the full adder circuits and also average power increases due to the presence of more number of transistors in the full adder-based counters. Basic gates are used in the parallel counters to construct the 6:3 counters [3]. It was found that this approach gave less delay and average power over [2]. However, this approach gave more transistor count than [2]. A method to further reduce the delay and average power over [2, 3] has been proposed in [4], where multiplexers are used to construct the 6:3 counters. It was found that this approach gave less transistor count over [2, 3]. The 3- bit stacker circuits and basic gates are used in the symmetric stacking-based counter to construct the 6:3 counter [5]. It was found that this approach gave better performance over [2-4].

Counters should provide less delay and average power. These counters should also provide less transistor count. However, most of the existing methods fail to provide less delay and average power [2-5]. Also, they fail to provide less transistor count. So, the development of a novel symmetric stacking based fast binary counters using modified gate diffusion input (M-GDI) technique [6] is required to provide less delay, average power, and transistor count.

MGDI is a low-power design technique [6]. The MGDI technique allows the implementation of basic gates using two-three transistors.

The proposed counter is designed using a stacker circuit, which reduces the number of gates required for the design. Due to this the delay decreases and the power consumed by the circuit also decreases.

Thus, by designing the stacker-based counter using m-GDI technique the number of transistors decreases because the stacker circuit which used 3 input and gate and or gates are designed only by 4 transistors, where 8 transistors are required in CMOS logic. Thus, the count reduces, and the power consumed by the circuit also decreases.

Thus, the proposed m-GDI based counter gives better performance than the traditional counters in terms of delay, the number of transistors, and power consumption. Simulations were run on the counters as well as the Wallace tree multiplier by using all the counters in 90nm technology. The same process is used to design counter-based Wallace tree multiplier [5,7], while the internal counters were changed. The paper is structured as follows. In section 2, MGDI technique for counters is introduced. Section 3 explains the stacker circuit for counters. Section 4 deals with the novel symmetric stacking based fast binary counters using MGDI technique.

Manuscript published on 30 September 2019
* Correspondence Author
Pavani Ivaturi*, Department of Electronics and Communications, Shri Vishnu Engineering College for Women (Autonomous), Bhimavaram, Andhra Pradesh, India.
N. Prasad, Department of Electronics and Communications, Shri Vishnu Engineering College for Women (Autonomous), Bhimavaram, Andhra Pradesh, India.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license http://creativecommons.org/licenses/by-nc-nd/4.0/

Section 5 deals with the novel fast binary counter-based Wallace tree multiplier. The simulation results are discussed in Section 6. Section 7 gives a conclusion.

II. MODIFIED GDI

Modified GDI [8] is one of the techniques which is used for low power. This method is also used for reducing the transistor count and further used for high speed, which is implementable in all current CMOS technologies. The main advantage of this method is the reduction of both subthreshold and gate leakage compared to CMOS technology [8]. So we are going for the modified GDI technique for counters.

a. Primitive Cells

The GDI cell is made up of two transistors and the GDI cell contains four terminals which are G, P, N, D. The G terminal the common gate input terminal of both n MOS and p MOS transistors. The P terminal is the node on the outer diffusion of p MOS transistor. The N terminal is the node on the outer diffusion of n MOS transistor, and D terminal is for both p and n transistors common diffusion node. Fig 1 shows the basic AND, OR, XOR gates constructed using modified GDI technique.

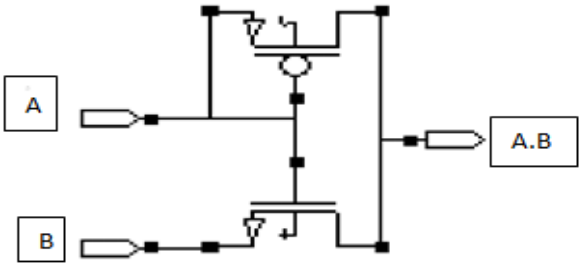

Fig 1(a). 2 input AND gate [6]

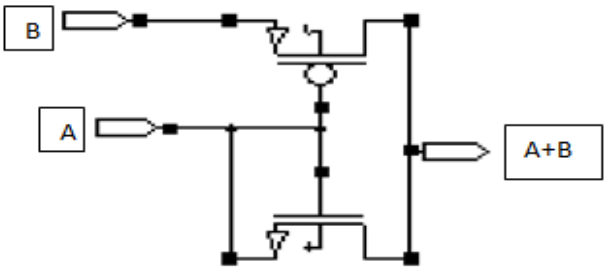

Fig 1(b). 2 input OR gate [6]

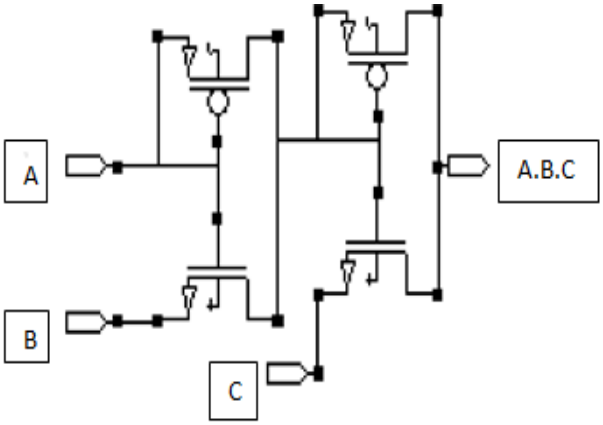

Fig 1(c). 3 input AND gate [6]

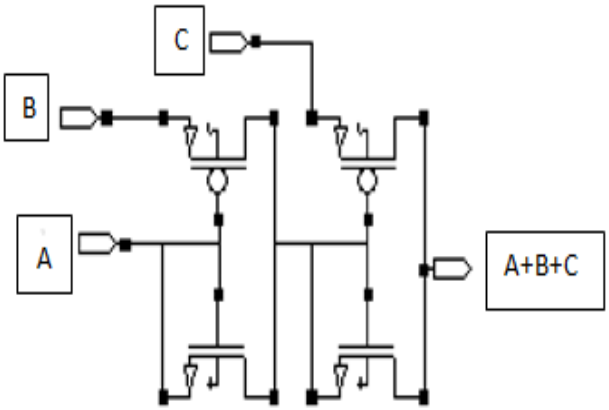

Fig 1(d). 3 input OR gate [6]

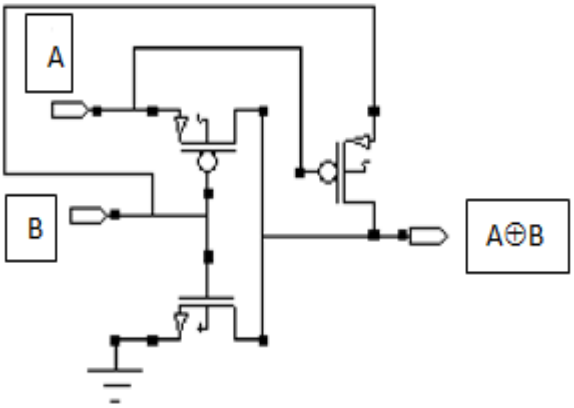

Fig 1(e). XOR gate [6]

Fig 1. Modified GDI based logic gates

The operation of the modified AND gate is given. For AND gate the drain of p MOS is connected to input A and source of n MOS is connected to input B. Both the gate terminals of p MOS and n MOS are connected to input A. when both inputs are zero, p MOS operates in linear and n MOS in cut off region and gives an output zero. When A=1 and B=0 the p MOS is in cut off and n MOS is in linear and gives an output zero. When A=0 and B=1 then p MOS is in linear and n MOS is in cut off and produces an output zero. When both inputs are one, then both p and n are in linear and they produce the output as one.

Since only 2-3 transistors are required for the M-GDI gates design, the number of transistors required for M-GDI technique reduces than CMOS technique [8]. Thus, the power consumption also decreases and delay also decreases.

III. STACKER CIRCUIT

Now by using these modified GDI gates the stacker circuit and counters are designed by using the stacker circuit. The stacker circuit is the one which group all the 1 bits together. The stacker circuit is shown in Fig 2. The circuit mainly consists of 3 inputs X_0, X_1, X_2. These are given to the basic gates to produce the stacker circuit and the outputs are observed as Y_0, Y_1, Y_2.

Retrieval Number C6847098319/2019©BEIESP
DOI: 10.35940/ijrte.C6847.098319
Journal Website: www.ijrte.org

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

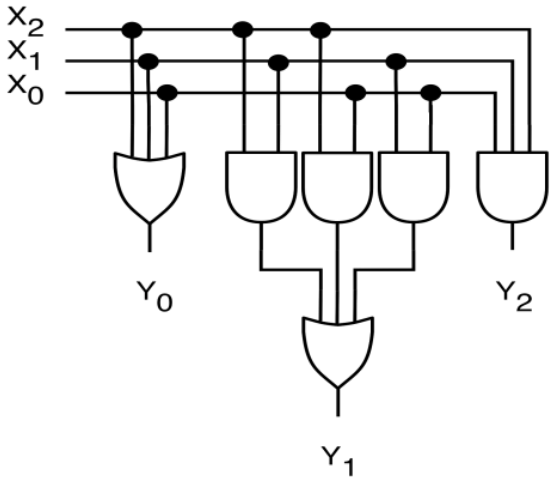

Fig 2. 3- bit stacking circuit [5]

The output equations of this 3- bit stacker circuit are given as [5]

$Y_0 = X_0 + X_1 + X_2$ (1)

$Y_1 = X_0X_1 + X_1X_2 + X_0X_2$ (2)

$Y_2 = X_0X_1X_2$ (3)

From the above equations, the Y_0 will be one if any one of the input is one. The Y_1 will be one if any two inputs are one. The Y_2 will be one if all the three inputs are one.

To form 6 bit stacking circuit from 3-bit stacker circuit, consider the inputs X_0,…X_5 are divided into two groups of 3 bits each and given to the stacker circuits. Consider X_0, X_1, X_2 are stacked as H_0, H_1, H_2, and X_3, X_4, X_5 are stacked as I_0, I_1, I_2. To form the 6-bit stack, two additional 3- bit vectors are required as J_0, J_1, J_2 and K_0, K_1, K_2. The J vector should be filled with 1's first followed by the K vector. So, the equations are given as follows [5]

$J_0 = H_2 + I_0$ (4)

$J_1 = H_1 + I_1$ (5)

$J_2 = H_0 + I_2$ (6)

From this, we can observe that all the 1 bits are occupied by the J vector first. The K vector is obtained from the same inputs by using and gates. The equations for the K vector given as follows [5]

$K_0 = H_2 I_0$ (7)

$K_1 = H_1 I_1$ (8)

$K_2 = H_0 I_2$ (9)

If the length of the sequence is three, then the K place bits are equal to 0's. if the length of the sequence is greater than three places then some K vector bits are equal to one that is both the inputs to the and gate are equal to 1. $J_0 J_1 J_2$ and $K_0 K_1 K_2$ contain number of 1 bit as of the input vector. Now by using two more 3- bit stacker circuits the $J_0 J_1 J_2$ and $K_0 K_1 K_2$ are stacked. The outputs are taken as Y5,.., Y0 vector. The example for this is given in Fig 3.

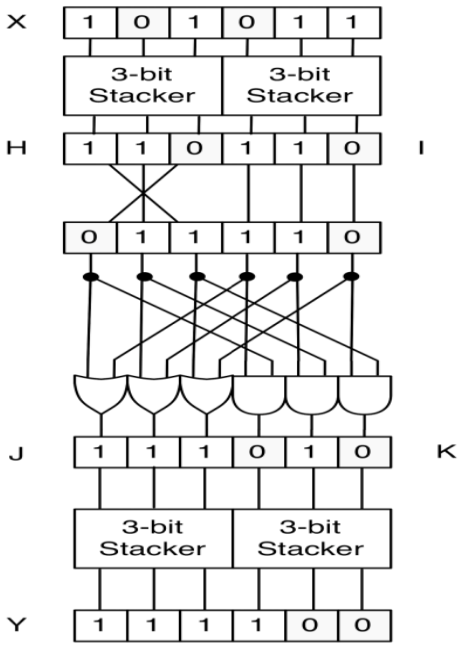

Fig 3. Six-bit stacking example [5]

The bits of J and K are again applied to stacker circuit, to form the final 6-bit stack output.

To perform the 6:3 counter operation, the obtained 6- bit stack should be converted into a binary number. The intermediate values obtained can be used for faster access. Let the outputs bits are considered as c1, c2 and s. the output is represented in the form of c2, c1, s.

IV. STACKER BASED COUNTERS & RESULTS

The 6:3 counter is designed using the stacker circuit. Fig 4 shows the 6:3 counter

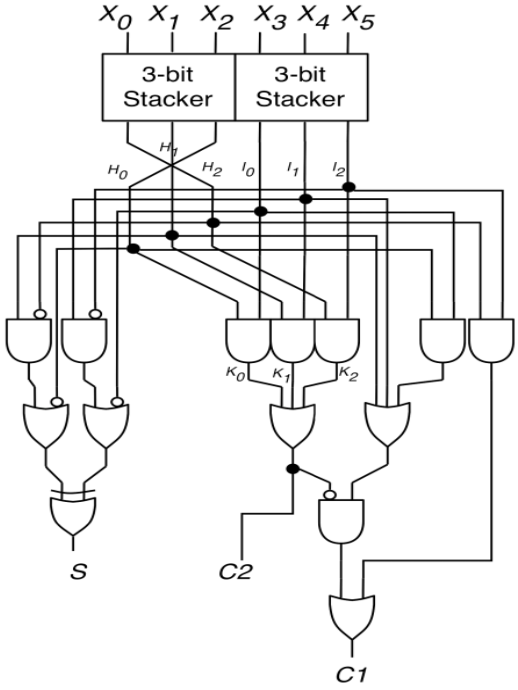

Fig 4. 6:3 counter [5]

To compute the output s, the parity of outputs from stacker circuit should be determined. H vector can be observed as the even parity when zero or two 1's appear in X_0, X_1, X_2. The parity of the I vector should be determined in the same way. Thus, H_e and I_e are given as [5]

$$H_e = \overline{H_0} + H_1\overline{H_2} \quad (10)$$

$$I_e = \overline{I_0} + I_1\overline{I_2} \quad (11)$$

Thus, the output s is given as

$$S = H_e \oplus I_e \quad (12)$$

The above XOR gate is not on the critical path. So, the delay will be further reduced. Similarly, the output c1 is given as, c1 = 1 whenever the count is 2, 3, 6. The general equation for the output c1 is given as [5]

$$c1 = (H_1 + I_1 + H_0I_0)(K_0 + \overline{K_1} + K_2) + H_2I_2 \quad (13)$$

Similarly, the output c2 can be set whenever the 4-bit set is observed. So the equation for c2 is given as

$$c2 = K_0 + K_1 + K_2 \quad (14)$$

From the above equations 12, 13, 14, the 6:3 counter is constructed as shown in Fig 3.

Simulations were run on designed 6:3 counter and the results are given in Table 1. From the simulation table, it can be observed that 6:3 counter performs better than existing. So we use this proposed 6:3 counter in designing of Wallace tree multiplier even though it uses a one more reduction phase.

V. WALLACE TREE MULTIPLIER USING COUNTERS

The proposed 6:3 counter was used in the design of Wallace tree multiplier for better performance. A standard Wallace tree is designed first for two different bit sizes and the delay and average power are calculated for that multiplier. No new designs were made, but the internal counters are varied within the existing multiplier. The different 6:3 counters are placed in the Wallace tree multiplier for 8-bit and 16- bit. The 16-bit counter-based Wallace tree multiplier reduction tree is given in Fig 5.

Table 2 gives the simulation results for 8-bit and 16-bit counter-based Wallace tree multiplier circuits.

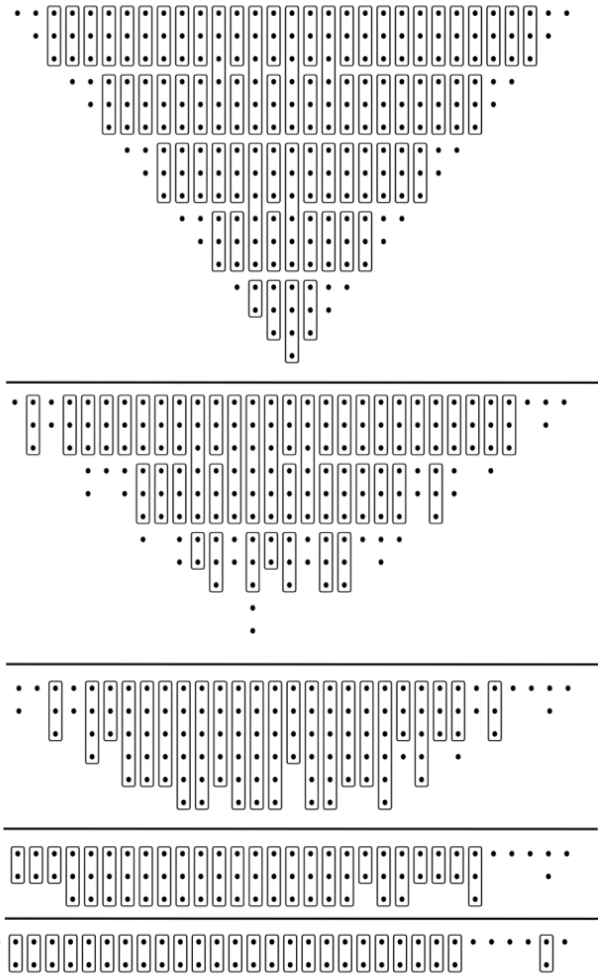

Fig 5: Counter Based Wallace multiplier reduction tree [5]

The partial products generated formed in the inverted triangle form and are grouped by using different half adders, full adders and 6:3 counters. Whenever there are only 2 bits they are grouped by using half adder circuits. Whenever there are 3 bits they are grouped by using full adder circuit. And the 6:3 counters are also used for reducing the partial products. The partial products reduction is done at different levels.

VI. COUNTER AND MULTIPLIER SIMULATION RESULTS

The paper mainly describes delay, average power, and transistors of proposed circuits which are 6:3 counter, counter-based Wallace tree multiplier designed using m-GDI. The delay or the latency is described as the maximum time taken to reach the output from the input [5]. In the counter circuits, the delay is observed from input to the output c1. Average power consumption can be calculated by adding the specter output and dividing it by simulation run time [5]. The transistor count is the total number of p MOS and n MOS transistors present in the design. The simulations were done at 50MHz.

Table 1 lists the results of proposed and conventional 6:3 counters in terms of delay, average power and the transistors. As the number of XOR gates in the full adder-based counter increases the delay is high than other counters. In the case of the parallel counter, the delay is 3 Δ_{XOR} + 2 basic gates. The MUX based counter has a delay of 1 Δ_{XOR} + 3 Δ_{MUX}. The stacker-based counter has no XOR gates or MUX on its critical path. So, the delay decreases in this circuit.

Table 1: 6:3 counter results

DESIGN	LATENCY (ns)	AVG.POWER (μW)	TRANSISTORS
CMOS full adder [2]	5.5	257.8	102
Parallel counter [3]	5.08	272.9	158
MUX-Based [4]	3.8	186.9	112
Stacker based [5]	2.15	137	124
Proposed	1.6	116	80

From the above table, it can be observed that the proposed 6:3 counter performs better in terms of delay and average power. So, we use this proposed 6:3 counter for designing Wallace multiplier even though it uses a one more reduction phase.

Table 2 lists the results of the counter-based Wallace tree multiplier in terms of delay and average power.

Table 2: Wallace tree multiplier using counter results

	LATENCY (ns)					AVG.POWER (mW)				
Size	CMOS full adders based [2]	Parallel counter-based [3]	MUX based [4]	Stacker Based [5]	m-GDI based	CMOS full adders based [2]	Parallel Counter based [3]	MUX based [4]	Stacker based [5]	m-GDI based
8	5.3	5.2	5.08	4.4	3.6	12.7	11.9	7.3	5.3	2.3
16	15.2	18.8	14.6	10.1	9.7	39.3	38	32	30.7	23.4

From table 2, the multiplier designed using stacking-based counter based on m-GDI technique gives better performance. The delay and the average power decreases compared to the traditional counter-based Wallace tree multiplier.

VII. CONCLUSION

A new binary counter is proposed using the stacking method based on m-GDI technique which reduces the transistor count and thereby increasing the performance of the circuit. By using the M-GDI technique, the transistor count decreases than the CMOS logic, thus the power consumption of the circuit decreases. Due to the stacker circuit in the design of the counter, it reduces the gate size thus the delay of the circuit reduces. Different 6:3 counters are designed using this method which can be used in designing the Wallace tree multiplier. The proposed 6:3 counter performs well than the existing counters. The 8 bit and 16-bit Wallace tree multiplier is designed and is simulated. The multiplier gives better performance in terms of delay and average power.

REFERENCES

1. A suggestion for a fast multiplier, by C.S.Wallace in IEEE Trans. Electron. Comput.,
2. Low-voltage and power CMOS full adder, by D.Radhakrishnan in IEE Proc.-Circuits, Devices
3. High-speed multiplier using multi-input counter and compressor circuits, by M. Mehta
4. M. B. Srinivas, S. Veeramachaneni, "Novel architectures for efficient (m,n) parallel counters,"
5. Christopher Fritz and Adly T. Fam, “Fast Binary counters based on symmetric stacking,” in IEEE Transactions on VLSI, Feb. 2017.
6. Pankaj Verma and Y.K. Mishra, "Modified GDI Technique- A power-efficient Method for Digital Circuit Design." In International Journal of Electronics and Computer Science Engineering.
7. Analysis of different architectures of the counter based Wallace multipliers, by S.Asif.
8. Padmanabhan Balasubramanian, JohinceJohn, “Low power Digital design using modified GDI method,” 2006, IEEE.