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Design of Bluetooth Communication System with Micro Controller with UART Based on Multi Bit Flip-Flop Shift Register

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ABSTRACT--- In this paper, we design and implement the first multi bit conversion-based log file with tuner and global asynchronous transmitter (UART) for Bluetooth simplex. UART is the main communication element of the Controller interface with external devices such as GSM, GPS, Bluetooth, etc. One problem with embedded systems is the time it takes to connect the external device to the controller. We focus primarily on fast communication between devices in integrated applications. The simulation results showed that the proposed system is 50% faster than the current system. The code is written in VHDL and ISE-Style KILX 10.1, is made with the help of the HOTGO Spartan 3E material tool.

Keywords— UART, shift register, multi bit flip-flop, microcontroller, single bit flip-flop, FIFO

I. INTRODUCTION

This document is a new structure of nerve fibres with global octane. UARTs are used for Bluetooth communication systems. UART computer interface or processor for the serial data channel. The receiver converts the serial bits, data, Symmetry, and stoups [1]. The sender converts the parallel data into a sequential model and starts automatically, and the bits are Symmetry and stopped. Volumetric weight can be 5, 6, 7 or 8 bits. Equality can be strange or otherwise. Symmetry and generation testing can be interrupted. Disabling objects can be one to two or half when you send 5-bit code [2].

Global Acetate Receiver (UART) is a popular device and is widely used for data communication in communications, embedded systems [9]. In this industry there are different versions of UART. Some of these are for receiver/sender backups and have several modes of 9-bit data (start bits + 9 bits of data + parity + bit down downtown) [4]. This program takes UART fully configured to optimize and implement in a variety of networking devices that have better performance and architecture than current semi tricks (specific products).

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This UART reference design includes receivers and transmitters. The receiver performs a sequential conversion of the asynchronous data frames obtained from the CIN record on the sequence documentation. The sender does business in parallel with the sequence of 8-bit data derived from the processor. To synchronize the unsynchronized serial numbers and add the raw serial data, the Symmetry and the point of consumption. An example of Vanity is shown in Figure 1 below.

Different programs can be used with UART, modems, printers, peripherals, and remote data recovery systems. Up to 8.0 MHz (500K baud) is an expanded range of Interseal barricades that is used at the Tempo of SEOS IV. Given the electricity price requirements, 300 MW is down to 10 MW [8]. Site Logic improves flexibility and simplifies user interface

The UART protocol is a series of protocols that approves the adding of data and produces different components in a row [7]. In destination, another UART segment is reclassified to all bytes. UART does not usually generate or accept external tags used in individual device-specific devices. A special device connector is used to convert from theoretical level to outer marker. External signals can take many different forms. Usually it has 3 lines (conveyor, receiver, ground) contact. Contacts that allow you to have a “Full Double” (Simultaneous sending and receiving) or "semi-binary" (Send/Receive devices)

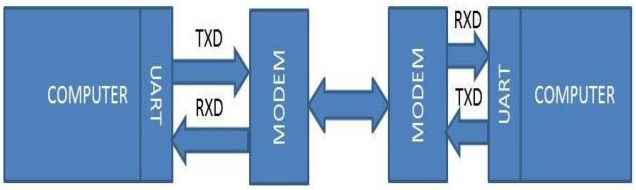

Fig. 1 UART diagram

II. PROPOSED SYSTEM

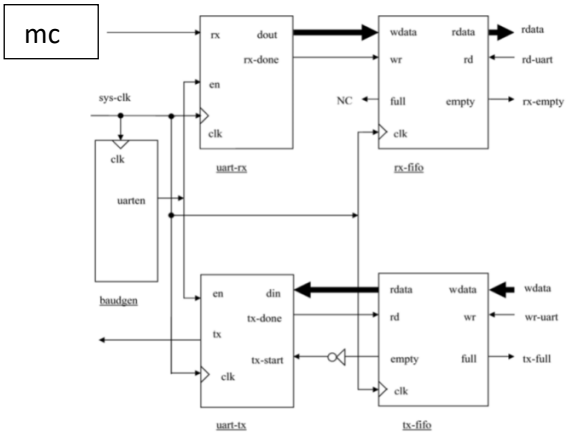

Fig.2. UART module

Bluetooth modules and microcontroller are designed for communication and this communication is done by UART module. The UART module consists of five parts, i.e. (I), "UART-RX ", which agrees with the range data (frame) line "RX ", is the actual information and converts it to parallel (typically bytes). 2) "UART-TX" which triggers the module "UART-RX" corresponded to the module and leaves the frame through the line " TX ". (III) "Baud gen" creates the clock 16 times per minute (by default, the oversampling rate). (IV) "" X-FIFF ", temporary storage bytes (usually for faster processors) because the steering process takes time. (V) A copy of the temporary storage module "RX-50" of the guided digital section, so that the processor can read at its own pace. UART is a module (Fig 2) I) two data corruption (WR write data and RD read data) used in parallel or processor. 2) two lines ("" RX "and " TX), where input data or data flow between two rows interacts. 3) The processor is used to adjust four lines (RD-UART, WR-UART, TX-full, RX-empty). (IV) "System clk" signal for all operations.

III. MULTI BIT FLIP-FLOP & RESULTS

In general, storage parts are memory elements and crafts. Flip flop saves a value periodically [9]. In our proposed system, Flip-flop stores multiple parts. Finally, we designed using more than two trades that were sent four bits. Multi-Small Flip Flop works as a technique for measuring the clock on the Pulse [3]. The timing of the rotation of the clock is displayed. D-Flip will throw all mixtures into the wall socket when the clock is high (active high), or if the clock is low (active low). In both cases, the passive status record contains data. The proposed gearbox is used to move the bits according to the Universal, asynchronous receiver and transmitter.

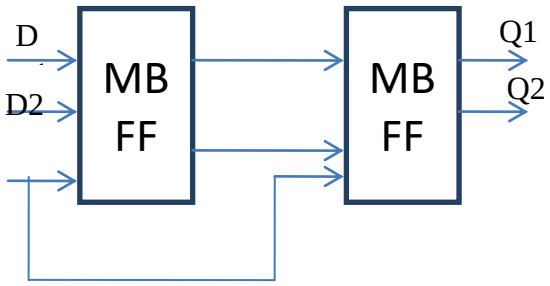

Fig. 3 Multi bit Flip flop shift register

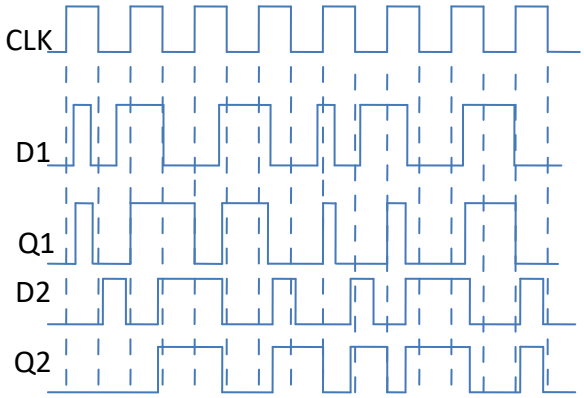

Fig.4. Timing diagram for multi bit flip flop

IV. RESULTS

The proposed system is modelled with Xilinx ise10.1 version. The register transfer level has been shown in the figure 7. The timing results of figure 4 and figure 5 of single bit flip flop and multi bit flip flop simultaneously. Table i shows the differences of the timing between proposed system and existing system. Figure 8 shows the waveforms generated in the model sim. Code is written in vhdl (very high speed integrated circuit hardware description language)

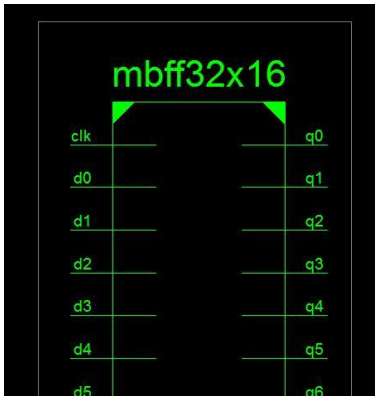

Fig 4: RTL view of Multi bit flip-flop

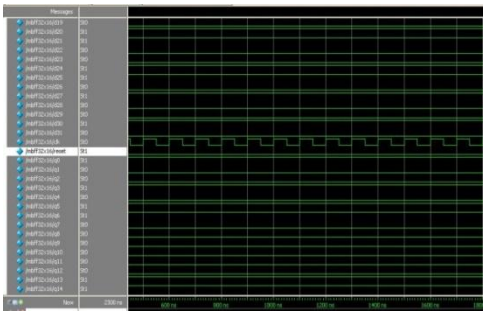

Fig 5: Waveforms of Multi bit flip-flop

Project File:	fergegw.ise	Current State:	Synthesized
Module Name:	mblf1	• Errors:	No Errors
Target Device:	xc3s500e-5fg320	• Warnings:	No Warnings
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	
Design Goal:	Balanced	• Timing Constraints:	
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	

fergegw Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	0	4656	0%
Number of Slice Flip Flops	4	9312	0%
Number of bonded IOBs	10	232	4%
Number of GCLKs	1	24	4%

Fig 6: Design summary of multi bit flip-flop

V. CONCLUSION

We have designed UART for Bluetooth communication with the multifunctional flip-flop shifts register in a generic form that was performed in accordance with the unmistakable and can be adapted to flood shelter with a given possibility and it can be available. The results showed that time decreased by about 50%.

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