International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-3, September 2019

Dolphin Echolocation Based Generation of Application Definite Noc Custom Topology

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Abstract*: Invention of new electronic devices in this technology driven-world has been setting a new scale for faster reach in terms of utilization and communication. The imperfection in the System on Chip (SoC) lead to an innovation of Network on Chip (NoC) that elucidates the communication defects and thereby set a new path for the researchers to enhance the network connectivity. Nature is an inspiration for most of the technologies invented by the researchers. In this paper, we have dealt the existing physical flows and future difficulties with Reliable Reconfigurable Real-Time Operating System (R3TOS) as a software interface with NoC with the proposed customized topology of Transmission Rate based Topology Design using Dolphin Echolocation (TRTD-DE) algorithm. Echolocation is biological scanning system that used by dolphins for movement and chasing the prey. The above ability along with Data flow pipelining (DFP) constructs the customized topology that process the parallel flow of data in order with the availability of the input data. The topology effectively increases the performance due to the clustering phenomena. The algorithm greatly reduces the latency period which is the significant of the topology and increases the throughput. The objectives of the research in the reduction of transmission rate and energy utilization are tested with different multimedia benchmark applications. The transmission rate reduced to average of 41.39% while average of energy consumption reduced to 31.9%.

Keywords: dolphin echolocation, FPGA, NoC, R3TOS

I. INTRODUCTION

As of late, the impact of electronic gadgets is cumbersome and in future, it would not a surprise if technology rules the world. With the cut down in the technology, the confinement imperfection in Field Programmable Gate Array (FPGA) due to the increase in the thickness as a result of deterioration of equipment over time [1]. The physical defects such as enduring flaws or tough flaws emerge as irreversible flaws in the equipment [2- 4]. In order to overcome the existing difficulties and to tackle the upcoming flaws, the researchers focused on equipment with long-durability in applications where alignment is absurd.

Reliable Operating System (ROS) proposed by Brebner, acted as a bridge in user application and executing the tasks in FPGA [5]. Hence, the new platform, R3TOS caters a program for progressing applications of high execution and authenticity into powerful reconfigurable FPGAs. R3TOS acts as software like medium to accomplish the hardware assignment using FPGA [1]. It will be an uphill task for the R3TOS to perform the assignments of SoC. SoC has to manage and execute large number of processors such as Digital Signal Processors (DSPs), storage components and Intellectual Property (IP) cores, with lagging in their performance [6]. The lagging is due to the unmanageable evaluation of Processing Components (Pc) and difficulty in broadcasting that requires a high performing and energy efficient broadcasting channel [7]. Researchers has proposed a NoC that is of less power utilization, energy saving and high broadcasting execution, due to their capacity and packet based broadcasting nature. The dissipation of power, broadcasting and energy are the limitations of structuring NoC [8]. Allocation of tasks to input data and execution of the task is the principal issues that have to be rectified in NoC [9]. In order to reduce the power dissipation, designing of customized topologies are more important rather than mapping to the traditional topologies such as ring, mesh, butterfly and so on.

The present-day Application Definite NoC (ADNoC) has different broadcasting prerequisite between different cores. [10], suggested that including standard topologies results in poor execution and large aloft of power dissipation along with area and therefore requires customized topologies for the application that are possible only with irregular topologies that reduces the power dissipation and area utilization. In order to achieve the best solution, we have to optimize the ADNoC with a couple of alternatives such as mathematical programming and metaheuristic algorithms. Techniques such as linear, nonlinear, stochastic and dynamic are mathematical based that performs confined but highly accurate search than stochastic techniques. However, they required slope and as well as a starting position to perform the same and the variables should be continuous[11]. Metaheuristic methods are naturally inspired optimization method and many researchers have worked on it. In our research, we are incorporating the smartness and intelligence of dolphins' second human in the world. Dolphin's echolocation optimization (DEO) is the approach of dolphin for analyzing their surroundings. Apart from DEO, DFP streamlines the flow of information through channeling, executes the information at the same time, and generates the outcomes parallelly.

Manuscript published on 30 September 2019
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The channeling optimizes at the operation level such as addition, multiplication, and storage operations so thereby increases the synchronous among them and results in better performance [12].

In this paper, we align the following topics as related work in chapter II, The overview of Dolphin Echolocation is explained in the Chapter III while Chapter IV consists of proposed routing element architecture for ADNoC, Chapter V describes of Proposed Application Exact Irregular Topology generation Design, Chapter VI comprises of results and Conclusion in Chapter VII.

II. RELATED WORK

A. Submission of the paper

FPGAs made the hardware tasks to act as a software tasks due to their reconfigurable attributes. These FPGAs captured and linked to various calculating sources on the fly. At present, stable on-chip region plays a vital role in maintaining the hardware multitasking effectively[13]. The reconfigurable calculating subject faces a discrete problem in planning and assigning the exchangeable hardware tasks to the FPGAs to meet the calculation deadline. The deadline for computation fails due to, delay in the allocation of tasks by the reconfiguration port or the unavailability of the resources before the deadlines voids[14]. The presence of compartments like structure in the FPGA makes it impossible for full utilization to deliver the maximum calculation capacities. To manage and overcome the impossibilities, a demand for ROS is mandatory to sort-out the problems on behalf of the user [15]. The main characteristics of ROS are handling of multiple tasks such as broadcasting between tasks and synchronization.

The computing capacity of the FPGA increases as long as the ROS interface are amiable by the user application whenever adding an extra tasks In self-healing FPGA, ROS assigns the already organized hardware tasks to unaffected calculation space and makes the system adaptable while the sloppy flaws are rectified by wiping in the configuration storage [5],[16]. The important drawback of ROS is performing a real-time organizing of task, as the rectification not only be logical but also an interim rectification is mandatory and achieved by having the flawless system at all the time. R3TOS shall achieve this without any additional rates for designing while adapts to the runtime rectification process. Reusability of the resource and calculation transiency is the basis of R3TOS. The finest chip granularity as a resource of R3TOS lets a system gain control in implementing high-level behavioral functionality as structured by system designer [17],[18]. R3TOS provides a concrete background to application to perform maximum at runtime and highly flexible into dynamically reconfigurable FPGAs. R3TOS acts an operating system for the execution of hardware tasks with accessible FPGA portions [17].

The unique sharing nature of resources by R3TOS during runtime execution of high volume applications in smaller devices obtained accurate performance for each while reduced the stable power dissipation [19]. In order to communicate the tasks, R3TOS is capable of generating broadcasting channels while required independently. This is possible only for low bandwidth broadcasting and for broadcasting high bandwidth; NoC is the best suitable space for R3TOS [20].

NoC efficiently distributes the task to R3TOS in real-time broadcasting within the specified deadlines [5]. NoC emerged as an alternative for the traditional bus-based structural SoC as a measurable broadcasting solution [21]. NoC design consists of a packet-switched on chip micro network and the foremost purpose is to enhance the clarity of broadcasting with the help of available link capacity. This results in powerful, quality performance, scalable and power effective broadcasting design in communicating the tasks. The prime feature of NoC is scalable and traceable during design time than conventional network system [22]. The involvement of symmetric topologies for general NoC does not yield the desired results for the required applications, which subsequently resulted in ADNoC, where the irregular topologies reduced the costs and energy consumption [23]. Applications such as multimedia shall run only on high frequency while real time devices such as portable devices requires only less power utilization and also delayed supply to avoid crashing[24]. In general, the energy utilization depends on the distance travelled in carrying the information that has to pass lot of routing elements and more the resources increases energy utilization. Hence, a need of custom topology arises that reduces the travel distance to the destination. With the help of high bandwidth cores, it enhances the performance and optimizes energy utilization [8].

More optimization zone is much more required, which is for ADNoC than traditional topology mechanism. Tosun proposed two topologies TopGen and Genetic algorithm (GA) based custom topology generation algorithm (GATGA) that reduced the consumption of the energy in ADNoC [25]. Holland and Goldberg proposed Genetic algorithm (GA) based on biological evolution of Darwin's theory [26], [27].

The researchers [28] proposed different topologies for ADNoC in the past and in this paper, researchers have proposed a new concept of DEO for topology generation with DFP .The dolphin echolocation optimization provides a better computational effort in a well-controlled manner[29]. The incorporation of dolphin echolocation initiated the energy aware routing and offered a best energy stored in the nodes which literally utilized less energy [30].

As DEO provides an insight about the outcome with reduction in computational cost and less utilization of energy, further to that inclusion of DFP further improves the efficiency. According to J B Dennis, G R Gao, the principles of pipelined execution achieves the high performance on many scientific applications [31]. DFP is a process that let the data flow by the concept of parallelism as an alternative to utilize the number of cores [32]. DFP enhances the mean instructions thereby schedules the flow of data per cycle to enhances the efficiency of the flow that indirectly reduces energy consumption [33]. Different techniques have their unique way in addressing the issues due to energy, power, cost and latency. Combination of two techniques always provides a better outcome in terms of efficiency and desired results.

We have integrated DFP in DEO in our research to amplify the desired outcome.

III. DOLPHIN ECHOLOCATION

To elucidate the compound problems, metaheuristic methods provide optimized solutions with the help of quest agents that land on accessible region unsystematically as well as with special rules [34]. One such optimization method is Dolphin Echolocation that resembles the approach of dolphin in search of their prey. They do with echo sounder to locate the destination as doing so modifies the target and its location.

Griffin coined the term "echolocation" to demonstrate the hunting nature of bats in search of their prey with the help of returning of high-frequency echoes due to the clicks emitted by itself. Mammals and birds belong to such group and the best of them is the Atlantic bottlenose dolphin [35]. Dolphin is capable of generating sounds as clicks and the frequency of sounds various for different species and communication. The energy of the click produced by dolphin determines their returning capacity once they struck the obstacles. As long as dolphin encounters the returning of clicks, it generates the clicks up to certain stage. This helps the dolphin to calculate the time taken between the clicks and returning echo as distance to the prey. Dolphins' evaluate the direction of the object by receiving the various signal strength on both of its heads. According to [11], dolphin continuously emits the sounds and receives the echoes and invades them. The short series of clicks that are directional are for echolocation known as click train and increases on approaching the favorable prey [36].

By optimization technique, it triggers the echolocation of dolphins by limiting its search that is directly proportional to the interval from the destination. To make it simple, assume a proposed optimization problem with two phases. In the first phase, the algorithm inspects to perform local bundle searching and navigates to the uninspected regions. This occurs through some random search across the space to perform the universal search and in the subsequent phase, it focuses all around for the optimal solutions attained from the previous stage. The unique essential attributes of meta-heuristic algorithms controls the randomly generated points to achieve the set of proportions to be achieved in phase 1 and 2 [29]. In addition, the incorporation of DFP helps the achieved data to flow parallelly without flaws while with minimum latency[12].

In this work, we proposed design of DEO based Application Exact Irregular Topology (AEIT) with DFP for ADNoC that comprises of Routing Element structure design and Transmission Rate based Topology Design (TRTD) using Dolphin Echolocation (DE) algorithm. In the following sections, we describe our proposed Routing Element structure and DEO based TRTD algorithm.

IV. PROPOSED ROUTING ELEMENT STRUCTURE FOR ADNOC

Routing Elements are the most important component that contributes the performance of NoC. The DFP incorporation in the structure forms the framework of NoC Routing Element as depicted in fig.1. The framework consists of single input and output port in a most precise way that Head Data Stream Unit (HDSU) is there for the head data besides organizing data flits in Data Executor Unit (DEU) for the input data arrival.

The design of the framework is in such a way to banish Head Data of Stripes (HDS) obstruction with the help of definite HDSU for the head data and data information cached in DEU. When the transmittance of preceding data information happens in to DEU, simultaneously getting the lined up header increases the pace of transmission of the information. The operation of the information flow is to fulfill the appeal of one slits before making the information flow to the subsequent slits by default. As each head data associates the information about the total number of the data information to be transmitted in that package itself, the redundant usage of tail data storage evaded in this structure.

The framework depicts that the input packet categorized into HDSU that consists all the head data and the data packet further into DEU1, DEU2, DEU3 and DEU4. The specific input data flits related to definite head units directly send to respective DEU. The embodiment of DFP via channels allocates the data as per the access design. The flow may be snaky design to improve the processing of new input concurrently rather than waiting to complete processing of previous inputs to reduce the overall inertia [12]. The detailed description of individual block is as per the following:

A. *Data Stream Regulator (DSR)*

The flits to the HDSU and DEU are allocated with the help of DSR. DSR panels the head data in to HDSU while the information data flits with unaccompanied head data flits moves to single DEU. In subsequent transmission of the information data flits finds their respective DEU after initially ensuring with head data flits. The incorporation of DFP allocates the input data based on their design accessibility which is implanted by DSR. The processing of each new input is improved by the incorporation of DFP rather than making it wait for the end of the flow of the earlier inputs with lesser overall latency.

B. *Routing Path Finder Unit (RPFU)*

The head data flits go to Routing Path Finder Unit (RPFU) that process the next routing element happens. The RPFU runs the routing algorithm to calculate the passage for next header unit to reach the arbiter. The algorithm runs without interruption because of adaptable routing for the reduction of time consumed for data travelling.

C. *Decoding Administrator Unit (DAU)*

It controls the picking switch by the enable indicator to illustrate that the elector is occupied or unconfined for sending the information. The grant indication from the arbiter triggers the DEU to identify and select the corresponding DEU as the information flows from HDSU and it is monitored by DAU.

D. *Arbiter*

Arbiter is the decider in sending the input to output, depending on the processing speed of the operation. The prioritization nature of arbiter pushes the information as required and acts a control indicator for an elector.

E. *Picking Switch*

The picking switch maintains the records of the data source sent to the destination as per the information established on the head data unit. Picking switch not only maintains the records but also

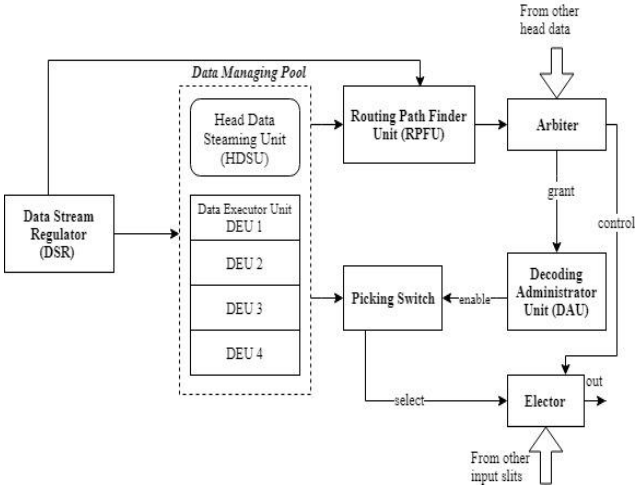

Fig. 1. Block diagram of Routing Element

monitors the DEU unit regard to that of kind of data related to particular head flits. The picking switch sends the select indications to the elector depend upon the quantity of information solicitation sent to the output.

F. *Elector*

The elector receives the information from all the source slits and depending on the information about the flit; the arbiter elects the desired information and send across for subsequent processing.

V. PROPOSED TRTD-DE FOR AEIT GENERATION

In this work, an AEIT is constructed by proposed Transmission Rate based Topology Design using Dolphin Echolocation algorithm (TRTD-DE) is shown in fig.2. Using TRTD-DE methodology, the Pcs are bundled based on the transmission rate between them. Then routing element is apportioned for each bundle to create the intercommunication between them. The main goal of the proposed TRTD-DE methodology is to reduce the total transmission rate and energy utilization in the AEIT. These two factors (i.e. energy utilization and transmission rate) are considered in the local and global bundle routing optimization of the proposed algorithm. Local Bundle Routing (LBR) communicates both inter and intra of neighbor Pc. Global Bundle Routing (GBR) is the communication between the bundles. The calculation of both LBR and GBR is described below to better measure the fitness of the objective.

A. *Local Bundle Routing (LBR) Function*

The LBR is defined by the following (1)

$$LBR = \min\{E_N(S_n \ldots D_n)\} \quad (1)$$

Whereas, initial Pc is Sn in the current bundle (CB) transmits the information through the neighbor bundle (NB) to the targeting Pc is Dn with minimum energy ingesting.

B. *Global Bundle Routing (GBR) Function*

In this routing, transmission occurs between the bundles, which gears end-to-end routing optimization. The transmission of the GBR is calculated as in (2)

$$GBR = \min \sum_{bi}^{bj} E_N \quad (2)$$

GBR objective function calculates the optimal shortest Communication between the bundles having minimum transmission rate and minimum energy utilization.

The algorithmic strides of the proposed topology construction are given subsequently:

Step 1: Random initialization of the dolphins:

The initial step of the calculation is the reinstatement of the number of dolphins (i.e., number of Pc of the given application, represented as N), identification of the random location of Pc, and population size (M).

Step 2:

To calculate the predetermined value and number of routing elements, the following computation performed.

Compute the predetermined value (γ):

The predetermined value defines the variation of convergence during the optimization process, given as (3),

$$\gamma(Mi) = \gamma + (1-\gamma_1) \times \frac{M_i^{\,x} - 1}{M^x - 1} \quad (3)$$

Where γ is the predetermined value, and the intermingling component of the first iteration is given as, γ_1 which builds the outcomes haphazardly. The quantity of current populace size is given as Mi, and convergence curve degree specified by x.

Compute the number of routing elements (re):

After calculating the predetermine value, the number of routing elements (re)can be calculated by (4),

$$r_e = \frac{N-2}{s-2} \quad (4)$$

With 'r' routing elements and assuming's' slits per routing element, we can compute total of r*s slits and r_e-1 links in the topology. Maximum number of Pc is connected to 'r' routing element is constrained to r_e(s-2) +2 value.

Step 3: Determine the fitness measure of individual dolphin using LBR

The fitness measure of the dolphin at the individual location is given as (5),

$$fi = \text{fitness (Fi)} \quad (5)$$

Where fitness (Fi) is the fitness calculation for individual Pc is based on LBT Eqn.1, to maximize the fitness. Total intra transmission (Tir) and inter transmission (Tie) made with PCs of the generated basic bundles computed by using the LBR fitness function.

Step 4: Creation, Selection and integration of group of bundles (C) based on the proportion of K

Based on the proportion of internal and external transmission K= Tir / Tie, the basic bundles are sorted-out in descending manner to forms the new set of bundles (C) with highest ratio value. The new set of bundles should possess all the PCs to validate the process, failing which the updating occurs. The number of bundles created should be equal to the re otherwise, integration of bundles encouraged for this equalization process.

Step 5: Determine the fitness measure using GBR

After assigning the routing elements to the newly generated set of bundles, transmission occurrence is calculated between the bundles using GBR fitness function as in (2).

Step 6: Evaluation of accumulative Best Fitness (BF) and its solution based on the dolphin rules:

In order to determine the best-customized topology, the best fitness measured dependent on the dolphin rules. The fitness dependent on the dolphin guidelines is refreshed for the individual iterations, and the fitness measure is given as (6),

$$BF_{(u+v)w} = \frac{1}{Y} \times (Y - |v|)\, fitness(Fi) + BF_{(u+v)w} \qquad (6)$$

Where $BF_{(u+v)w}$ is the accumulative fitness for (u+v)wth alternative corresponding to wth variable, and Y symbolizes the effective radius that should not exceed the ¼ of the search space.

The best fitness optimal solution (Bopt) obtained from the accumulative fitness has minimum energy utilization and transmission rate that produce a new topology for the AEIT. This topology added into the topology pool. The present newly created bundle topology of TRTD-DE, compared with the previous available topologies in the library to select the best-customized topology that suits the design objectives and update the same in the pool. Otherwise the process of BF computation reoccurs which is given in (7),

$$Best\_sol = \left\{ \begin{matrix} B_{opt_{present}} \,\&\, update, B_{opt_{present}} \geq B_{opt_{past}} \\ recomputeB_{opt}, else \end{matrix} \right\} \textbf{(7)}$$

Step 7: Compute and update γ based on the BF solution

Based on the results obtained in step 6, the predetermined value is updated in this step. Based on the outcomes of BF, compute the (8),

$$\gamma_{xy} = \frac{BF_{xy}}{\sum_{x=1}^{N} BF_{xy}} \qquad (8)$$

And upgrade this value for the picking other optimal solution, given as (9)

$$\gamma_{xy} = \left\{ \begin{matrix} \gamma, ifx = bestsol(y) \\ (1-\gamma)\gamma_{xy}, else \end{matrix} \right\} \qquad (9)$$

The termination iteration happens when met with the best optimal solution or reoccurrence of the stages from fitness calculation using dolphin rules continues. Based on the above algorithmic steps the best solution is picked as an optimal bundle topology using TRTD-DE.

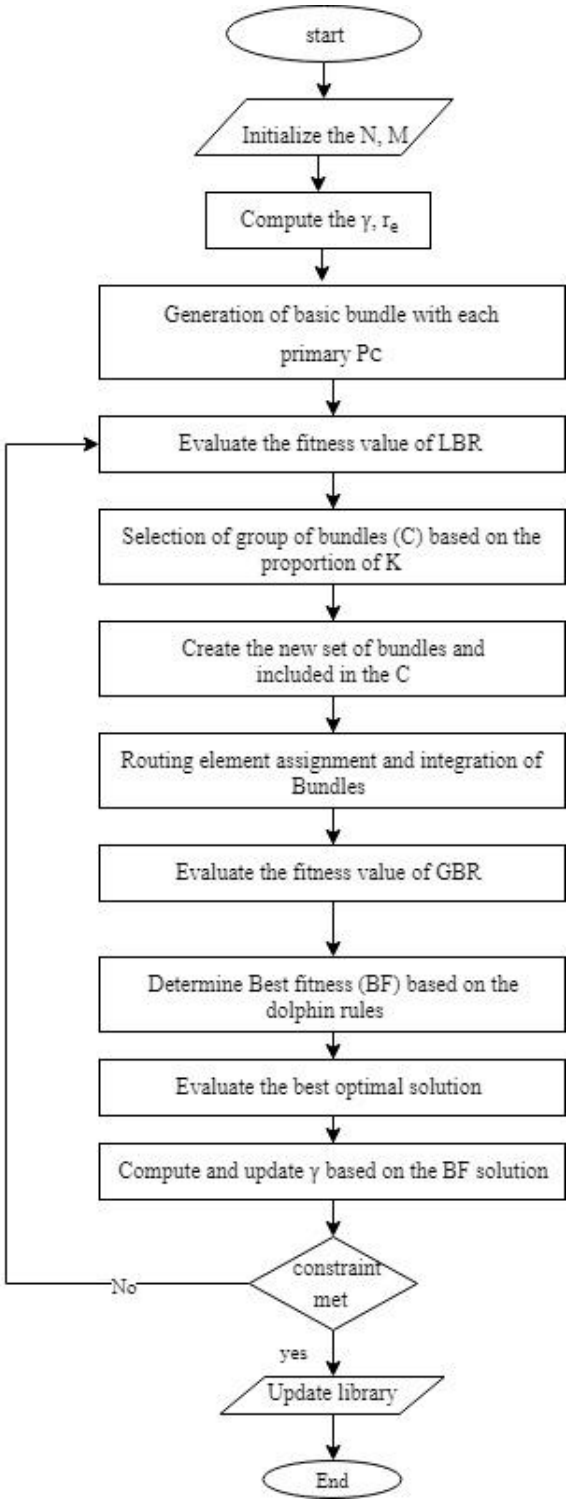

Fig. 2. Flow graph of TRTD – DE

VI. EXPERIMENTAL ANALYSIS AND DISCUSSION

This section compares the analysis of the results of different topologies such as Top Gen [37] and PATC (Power - Aware Topology Construction) [38] along with our proposed Transmission Rate based Topology Design using Dolphin Echolocation algorithm (TRTD-DE).

For the purpose of assessment, we have run the benchmark applications such as Context Adaptive Variable Length Coding (CALVC), Multimedia Window Display (MWD), Picture in Picture (PIP) and Video Object Plane Decoder (VOPD) against other existed topologies with 8, 12 and 16 cores respectively of Vivado 15.1 and implemented in Zynq7000 series xc7z020clg484-1chip.

The Proposed TRTD-DE topology with the incorporation of dolphin echolocation technique rigorously generates customized topology with number of Pc. The results of all along with the throughput, energy, latency and rate is given in the below Table I.

A. *Throughput Analysis*

It is the quantity of information flow from the start to that of end node in a particular given time. i.e. mean number of quantity delivered per second. The throughput of the Proposed TRTD-DE topology has shown in fig.3 an increase of 19.34% compared to that of Top Gen with the benchmark application of PIP with 8 cores while there a considerable increase than PATC in the throughput by 8.41% in CAVLC with 16 cores.

B. *Energy Consumption Analysis*

The main motivating factor for our research is to limit the energy utilization while transmitting the information from Pc to Pc. With our proposed topology, we have achieved the minimal energy utilization for the transmission of information as shown in fig.4.

The topology TRTD-DE generated proved that our topology had outperformed TopGen and PATC topologies with maximum energy saving is witnessed in VOPD with 16 cores by 24.5% of TopGen while the energy utilization reduced to a great extent by 41.3% in CAVLC with 16 cores compared to PATC topology. The reduction in the energy is due to the specific nature of dolphin echolocation as it carefully generates the topology.

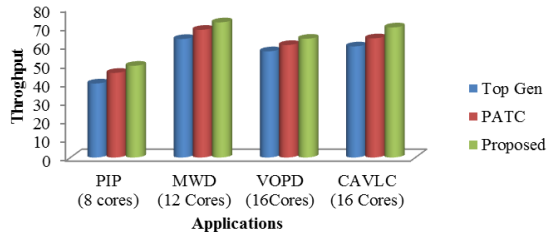

Fig. 3. Throughput Analysis

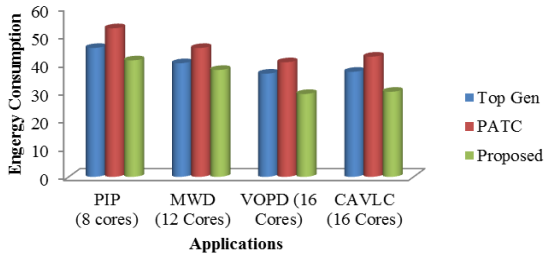

Fig. 4. Analysis of energy consumption

Table- I: Performance comparisons of various applications

Applns.	Topology	Throughput (Mbps)	Energy (µJ)	Latency	Trans. Rate
PIP (8 cores)	Top Gen [37]	39.62	45.65	11.49	1320
	PATC [38]	45.31	52.62	12.95	898
	Proposed	49.12	41.25	10.61	568
MWD (12 ores)	Top Gen [37]	63.42	40.24	15.94	852
	PATC [38]	68.35	45.63	16.21	1054
	Proposed	72.34	37.86	14.23	725
VOPD (16Cores)	Top Gen [37]	56.84	36.54	16.13	1772
	PATC [38]	60.23	40.58	17.24	1890
	Proposed	63.57	29.35	15.25	1600
CAVLC (16 ores)	Top Gen [37]	59.46	37.21	16.34	1845
	PATC [38]	63.78	42.56	19.37	1956
	Proposed	69.64	30.12	15.24	1759

C. *Analysis of Latency*

Latency is one of the factors to analyze the performance of NoC. The travelling of data from the start to that of preferred terminus in a specific time is called latency. It requires the time to reach at the start node, the time to cross from the start node to that of destination node and anticipating time in the buffers and the flit counts in the way of the data. The maximum latency means the maximal delay induced in the travel of flits. The fig. 5 depicts the latency of different topologies at different cores of 8, 12 and 16 respectively.

The customized TRTD-DE topology experiences the desired lesser maximum latency up to 21.74% in VOPD of 16 cores compared to that of Top Gen while it achieved the highest reduction of latency by 22.05% in PIP of 8 cores than PATC topology.

D. *Analysis of Transmission Rate*

In the previous studies though the focus were there to reduce the transmission rate, due to failure to offer the best-optimized solution for transferring the data from one end to another end resulted in high cost. The transmission rate between the node to node from our study is plotted in the below graph fig.6.

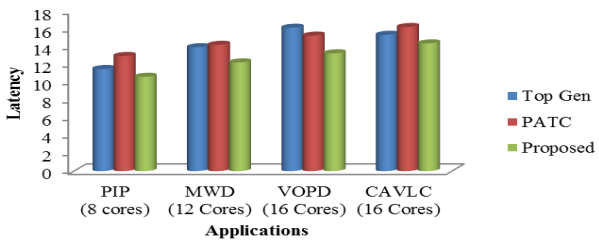

Fig. 5. Latency analysis

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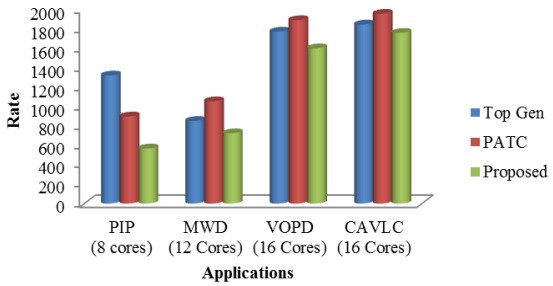

Fig. 6. Analysis of transmission rate

From both the graph and table I, the transmission rate reduced significantly to an average rate of 41.39% for all the applications run of TopGen topology. At the onset when compared to PATC, our proposed work utilized a transmission rate of 33.20% for all the benchmark applications. This is because the generated customized topology let the transmission of information steadily than other topologies.

VII. CONCLUSION

In this work, we present a novel naturally inspired Transmission Rate based Topology Design using Dolphin Echolocation algorithm (TRTD-DE) for the generation of custom topology. Our proposed topology with the incorporation of DFP makes the data to flow parallelly that lead to the effective achievement in latency reduction. Due to the flow of data parallelly the throughput increases as many data flows subsequently. Overall on average the latency is 16.52% lesser in the proposed topology than PATC while the throughput increases on an average of 14.22% than TopGen. The clustering of processing nodes in the topology due to DE concept proved the effectiveness in consuming less energy which subsequently enhances the transmission rate reduction than other topologies. The energy consumption when compared to other topologies decreases to an extent of 31.9% while the topology significantly reduces the transmission rate by 41.39%. As different from previous topologies, our future work focuses on implementation of more applications in the designed NoC architecture and to further study about effect of our topologies with various algorithm so that to know about the consistency.

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