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PWM Technique for Single Phase Asymmetrical Hybrid Multilevel Inverter for Non-linear and Dynamic loads

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Abstract*: A two level VSI has output voltage either equal to positive or negative source voltage. This inverter has more ripple. In order to reduce the ripple content more number of switches are needed to produce many number of stepped voltage waveform. This improves the quality of power. This switching losses depends on the frequency of operation so when a two level inverter is operated at high frequency, the switching losses are predominant. This limits the use of such inverters. Hence, being replaced by Multilevel inverters. They have attracted academician and industry personal for medium and high-power power control. Such attractive features are available in hybrid multilevel inverter. Hence, these are preferred. They provide multi-level operation by using hybrid sources. Moreover, the number of power electronics components needed are less than conventional CMI for same voltage level. Thus, such inverters have more efficiency. In the proposed techniques, an asymmetrical hybrid multilevel inverter has been simulated using MATLAB Simulink. The results obtained have been presented for three different types of load.

Keywords: **ASMI, CMLI, MLI, PWM.**

I. INTRODUCTION

In a single phase Cascaded MLI, equal source voltage is applied in each cell which may be unavailable. This limits the use of CMLI as equal voltage may not be available all time for each independent unit, referred as cell [6,7,11, 13]. In some cases, entire modular structure may be lost if unequal source voltage to the cell is applied or may be the switching pattern design becomes tedious. Such difficulty could be easily eliminated if one uses an asymmetric hybrid multilevel inverter (ASHMI) [1,4]. A simple circuit showing an ASHMI is shown in Fig. 1. It is seen from the figure that each unit has a different values of DC source which is being controlled by two switches. The gate pulse designed to each of the two cell is complimentary to each other. This avoids direct short circuit to dc source. To increase the stepped voltage level, not only the number of cell units need to be increased but also switching needs to be properly designed.

Increasing the number of stepped voltage has advantage that the ripple in the output voltage will decrease; moreover, there will be increase in the output voltage [9, 10]. This improves the nature of the output signal. Thus, the THDs present in the output will be less [12]. This improves the efficiency of the inverter as losses due to odd order harmonics will be less. This is possible with use of ASHMI. This configuration requires less number of controlled devices when compared with CMLI. There by, further reducing the switching losses. The devices in one cell could be operated at higher frequency while devices in other cell could be operated at lower frequency. This also help to reduce losses. As losses is high at higher frequency but low at fundamental frequency.

To switch on the devices in each cell, pulse width modulation technique (PWM) has been used [8] where a reference signal when compared with a carrier signal produces PWM. In this case, a sinusoidal signal has been used as reference while triangular signal has been used as carrier [2]. These signals are so designed to make switching possible for ASMI.

II. ASYMMETRICAL MULTILEVEL INVERTER (ASMI)

In cascaded multilevel inverter, each half bridge has two switches whose switching pattern is complementary in nature. Moreover, the rating of each of these switches varies with increase in voltage level. A major drawback of this inverter is its inability to supply both positive and negative half cycle to an AC load [14]. In order to achieve alternating stepped voltages, two half bridges are connected together. This increases the number of switches.

The ASMI has been derived from a cascaded half bridge inverter. This helps in reducing number of switches along with increased output voltage level [15]. In ASMI each cell has two power switches (S_n; S_{0n}) and a DC source, V_{dcn-1}, which are operated in a complementary manner to either connect the DC sources to the load or to bypass them. Whereas, in the n^{th} cell, asymmetric DC sources, whose magnitude is equal and opposite of the sum of individual "n-1" cells, are utilized to increase the voltage levels in reverse direction. Thereby, increasing possible output voltage levels with minimum number of power switching devices and components. A simple three cell topology has been shown in Fig.1. Each cell has two switches marked as S_1; S_{01}, S_2; S_{02}, S_3 and S_{03}. The source voltage to each cell is V_1, V_2 and V_3 respectively.

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The magnitude of V2 and V3 are calculated on the basis of equation (2) and (3). Here V3 is a reverse polarity DC sources whose magnitude is equal to the sum of V_1 and V_2. This provides the peak negative output voltage whereas the other negative voltage levels can be produced by subtracting V_1 and V_2. The switching pattern starts from cell having source voltage of V_1. When S_1 is triggered then the output voltage V_1 appears across the load and is zero when its complementary switch S_{01} is turned on. Similarly, when S_2 is triggered on, V_2 appears across load. When both S_1 and S_2 are switched on, $V_1+ V_2$ appears across the load during one half cycle. While negative half cycle is obtained by either by adding V_1 or V_2 with V_3. The maximum peak voltage in reverse direction is equal to source voltage of cell, V_3. These voltages are also marked in the Fig. 2, shown in rectangular blocks. This could be expanded for higher level where increase in each cell, increases four level higher from its previous structure. For obtaining 7 level output voltage with three cells, the switching states are as shown in Table I. Proper selection of magnitude of asymmetric DC source, V_n, is must for uniform stepped generation of voltage.

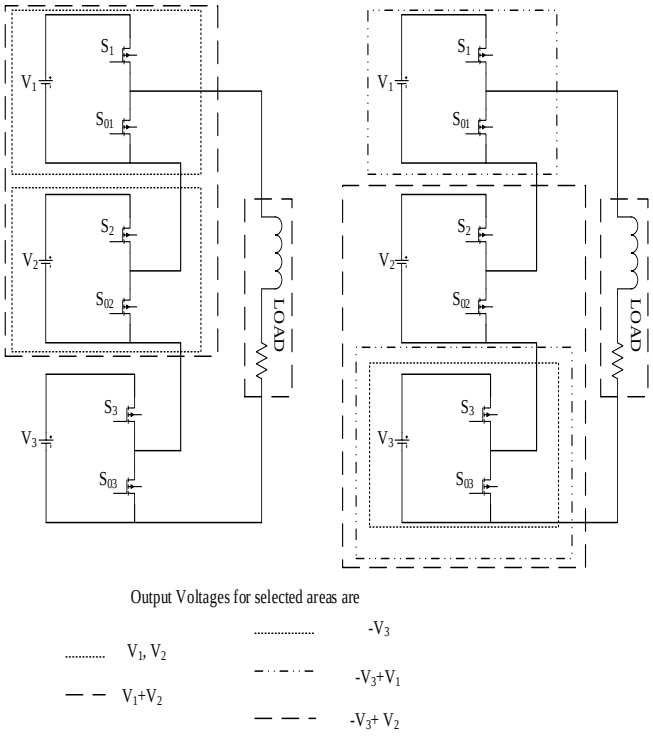


Fig. 1. Stepped Voltage Generation

To determine the voltage for each cell in asymmetric inverter, it is assumed that there are "n" cell available. Each of these cell has a voltage V_{dci} for i=1… (n-1). The equation which relates the magnitude of voltages in such cells are given in equations (1) – (2). While the "n^{th}" cell input voltage is expressed in equation (3).

$$\mathbf{V_{dc1} = V_1} \quad (1)$$

$$\mathbf{V_{dci-1} = (i\text{-}1) * V_{i-1} \quad for\ 2<I<(n\text{-}1)} \quad (2)$$

$$V_{dcn} = \sum_{i=1}^{n-1} V_{dc_i}, i = 1, 2, \ldots . (n-1) \quad (3)$$

The nth cell should have a voltage whose magnitude is obtained from equations (3). This should have connected in such a way that polarity is reversed to that of individual "n-1" cells. This helps in achieving stepped voltage in reverse direction. To determine the total number of levels in one cycle, it may be calculated on basis of equation (4)

$$\mathbf{N_{level} = 2^2 * n\text{-}1} \quad (4)$$

While, the peak to peak output voltage, V_p is found to be:

$$\mathbf{V_{OM} = 2 * V_{dcn}} \quad (5)$$

For each DC sources, there are two switches S_n and S_{0n}. these switches are complementary to each other and in turn connected to load. So, the total number of switches needed, N_{sw}, is expressed in equation (6):

$$\mathbf{N_{SW} = 2n} \quad (6)$$

The peak inverse voltage, PIV_n, for each switch, is expressed in equation (7) as under:

$$\mathbf{PIV_n = V_{dci};\quad i = 1; 2; 3; \ldots\ldots n} \quad (7)$$

III. RESULTS

The entire simulation has been carried out in MATLAB Simulink at NERIST based server. The triggering angle has been generated as per the Table II using sinusoidal based reference signal and triangular based carried signals. These pulses are used for turning on the power electronics devices "S_i" and "S_{oi}", as shown in Fig 1. such that the pulses are complimentary to each other in each cell. To generate seven level, the no of switches needed are 6 while 8 switches are needed for nine level of output voltage. In case of cascaded multilevel inverter, each H-bridge needs 4 switches to generate three level of voltages whereas, only 2 switches are needed in the case of asymmetrical multilevel inverter.

The results obtained are shown through Fig. 2 to Fig. 6 for both types stepped voltages. The rms output voltages are 213.4V and 209.8V respectively as seen in Fig. 2 and Fig. 3. The load currents for different types of loads, namely linear, non-linear and dynamic loads are shown in Fig. 4 while their THDs are shown in Fig. 5 and Fig. 7.

TABLE I. SWITCHING STATES FOR SEVEN LEVEL

S_1	S_{01}	S_2	S_{02}	S_3	S_{03}	Output Voltage
1	0	0	1	0	1	V_1
0	1	1	0	0	1	V_2
1	0	1	0	0	1	$V_1 + V_2$
0	1	1	0	0	1	V_2
1	0	0	1	0	1	V_1
0	1	0	1	0	1	0
0	1	1	0	1	0	$-V_3 + V_2$
1	0	0	1	1	0	$-V_3 + V_1$
0	1	0	1	1	0	$-V_3$
1	0	0	1	1	0	$-V_3 + V_1$
0	1	1	0	1	0	$-V_3 + V_2$
0	1	0	1	0	1	0

IV. CONCLUSION

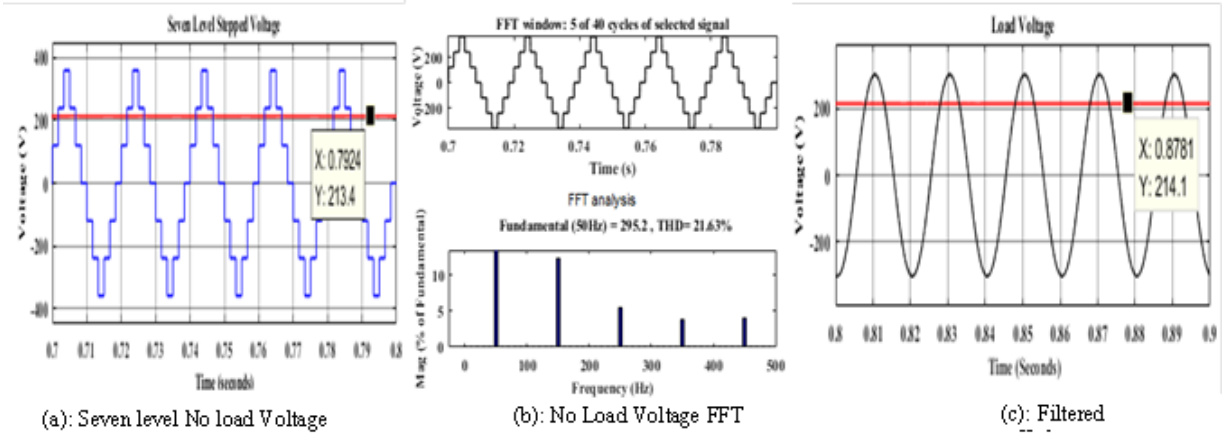
It is seen from Fig. 2 and Fig. 3 that a stepped voltage of seven and nine have been successfully obtained through simulation. These stepped output voltages have been filtered out to make a sinusoidal voltage wave form such that it is under IEEE standard (<5%).

Three different types of loads have been applied to the inverter to analysis current THDs. The current waveforms are shown in Fig. 4.

Their corresponding THDs are shown in Fig. 5 and Fig. 6. The current and voltage THDs are summarized in Table –II. It is seen that there is 14.81% reduction of voltage THD as level shifts from seven to nine. The effect of load may be observed through current THDs for various load. These THDs are tabulated Table II. For a seven step, the non-linear load has a THD 49.91% while it is reduced to 12.33% for nine level. A dynamic load has intermediate THDs irrespective of voltage levels.

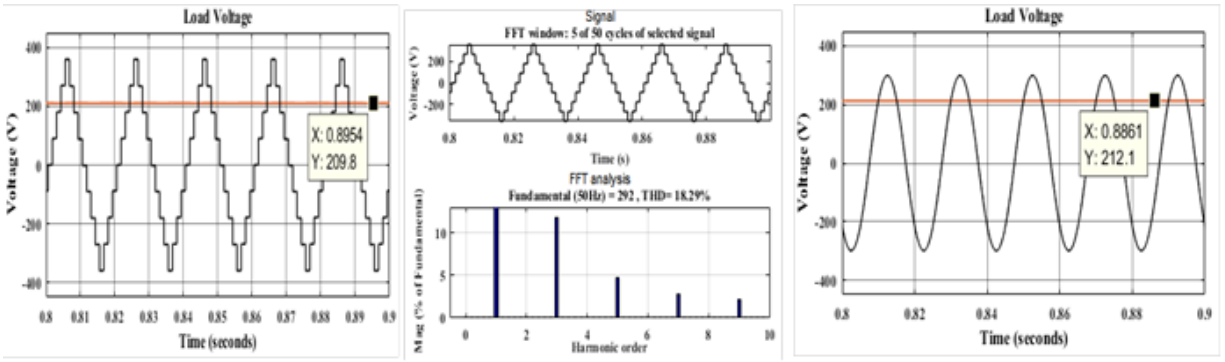
TABEL II THD VALUES

Voltage Level	Voltage THD in %	Current THD in %		
		Linear Load	Non-Linear Load	Motor Load
Seven	21.63	1.02	49.91	15.17
Nine	18.29	0.81	12.33	6.34



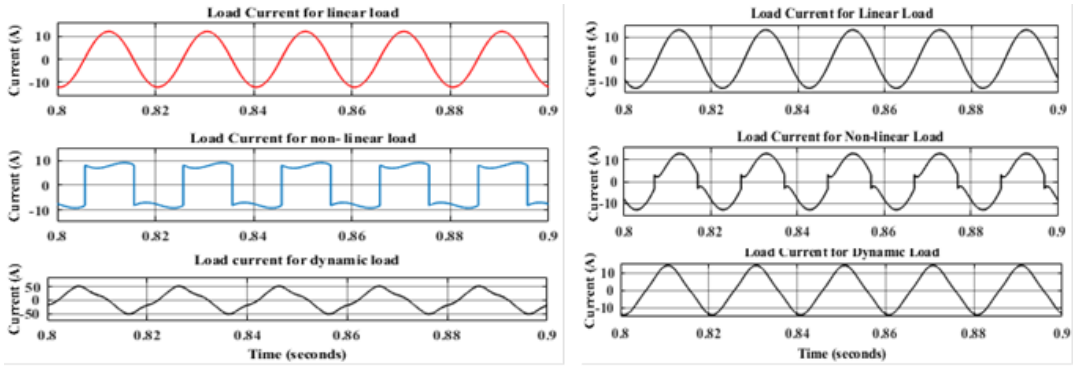
(a): Seven level No load Voltage (b): No Load Voltage FFT (c): Filtered

Fig. 2. No load seven stepped Voltage



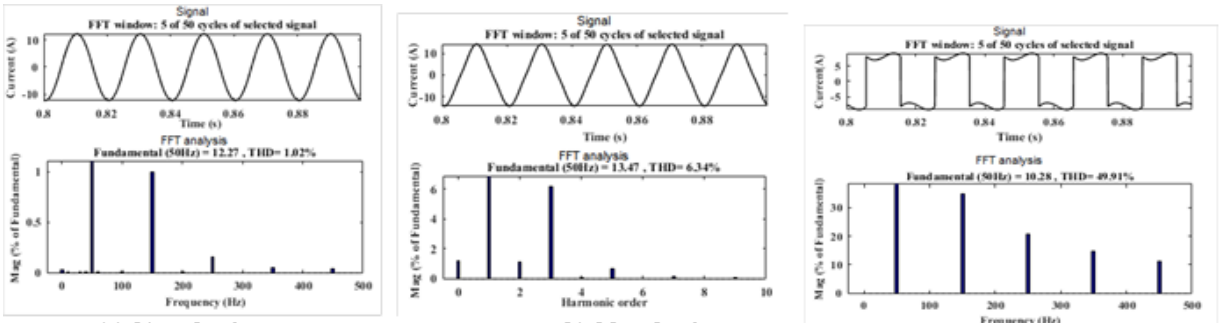
(a): Stepped Voltage (b): Voltage THD (c): Filtered Voltage

Fig. 3. No load nine stepped Voltage with its THD



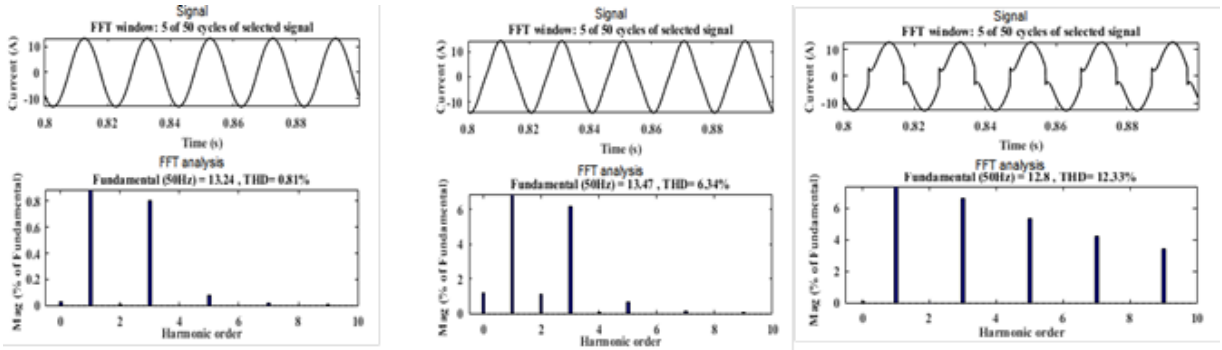
(a): Load current (b): Load current

Fig. 4. Load current obtained through seven and nine level



(a): Linear Load (b): Motor Load (c): Non-Linear Load

Fig. 5. Load Current THD For seven level



(a) Linear Load (b) Motor Load (c) Non-linear Load

Fig. 6. Load Current THD For nine level

Sl No	Parameter	Value
1	RL load	25Ω; 0.02H
2	No of SCR	4
Split phase Induction Motor		
3	Stator winding Resistance & Inductance	2.02Ω; 7.4e-3 H
4	Rotor winding Resistance & Inductance	4.12Ω; 5.6e-3 H
5	Mutual Inducatnace	0.1772 H
6	Inertia (Kgm^2)	0.0146
7	No of poles	6
8	Supply Frequency	50 Hz

TABEL III. LIST OF PARAMETERS

REFERENCES

1. Madan Kumar Das Akanksha Sinha Kartick Chandra Jana, "Hybrid Multilevel Inverter with Reduced Switches Topology", 5th IEEE Conference on Electrical, Electronics and Computer Engineering 10.1109/UPCON.2018.8596873.
2. A. Sharma, D. Singh, P. Devachandra Singh and S. Gao, "Analysis of Sinusoidal PWM and Space Vector PWM based diode clamped multilevel inverter," 5th IEEE Conference on Electrical, Electronics and Computer Engineering, 2018, pp. 1-6. doi: 10.1109/UPCON.2018.8596899.
3. Anil Kumar Yarlagadda ,Vargil Kumar Eate ,Y.S.Kishore Babu Abanishwar Chakraborti, "A Modified Seven Level Cascaded H Bridge Inverter," 5th IEEE Conference on Electrical, Electronics and Computer Engineering, 2018, pp.1-6. doi: 10.1109/UPCON.2018.8597096.
4. Farhana Patel and Bharati Sonavane, "Simulation And Implementation Of Hybrid Multilevel Inverter", Volume 2, Issue 6 JETIR, May 2015 pp 1758-1762.
5. Suman Singh, Mohit Jain and Anuradha Singh , "Performance Evaluation of Asymmetrical Cascaded H-Bridge Multilevel Inverter", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 4, Issue 1, January 2015, pp 222-231.
6. B. Suresh Kumar, Ganta Joga Rao, "Simulation of Single Phase Multilevel Inverter Topology for Distributed Energy Resources Using Multi Inputs", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 12, December 2013.
7. B. Ashok and A.Rajendran, "Selective Harmonic Elimination of Multilevel Inverter Using SHEPWM Technique", International Journal of Soft Computing and Engineering Vol.-3, Issue-2, May 2013, pp-79-82.
8. R. Palanisamy and K. Vijayakumar, "Hardware Implementation of Single Phase Diode Clamped 3-Level Inverter", IJCTA, 2016, pp. 975-981.
9. Fang Zheng Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", IEEE Transactions On Industry Applications, vol. 37, no. 2, pp. 611-618, March-April 2001. doi: 10.1109/28.913728.
10. Mamatha Sandhu and Tilak Thakur, "Multilevel Inverters: Literature Survey – Topologies, Control Techniques & Applications of Renewable Energy Sources" Grid Integration, Mamatha Sandhu et al Int. Journal of Engineering Research and Applications ISSN : 2248-9622, Vol. 4, Issue 3(Version 1), March 2014, pp.644-652.
11. Li Li, Dariusz Czarkowski, Yaguang Liu, and Pragasen Pillay, "Multilevel Selective Harmonic Elimination PWM Technique in Series-Connected Voltage Inverters", IEEE Transactions On Industry Applications, Vol. 36, No. 1, January/February 2000.
12. N. Prashanth, B. Kumar, J. Yadagiri and A.Dasgupta, "Harmonic Minimization In Multilevel Inverters By Using PSO", ACEEE int. journals. On Control System and Instrumentation, Vol. 02, No. 03, October 2011.
13. Ali Ajami, Behrouz Mohammadzadeh, and Mohammad Reza Jannati Oskuee, "Utilizing the Cuckoo Optimization Algorithm for Selective Harmonic Elimination Strategy in the Cascaded Multilevel Inverter", ECTI Transactions On Electrical Eng., Electronics, And Communications Vol.12, No.1 February 2014.
14. Alessandro Luiz Batschauer, Samir Ahmad Mussa, and Marcelo Lobo Heldwein, "Three-Phase Hybrid Multilevel Inverter Basedon Half-Bridge Modules", IEEE Transactions On Industrial Electronics, Vol. 59, No. 2, February 2012.
15. Austin Hughes, Bill Drury, "Inverter-fed Induction Motor Drives in Electric Motors and Drives," Fourth Edition, 2013.