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Implementation of Double Tail Dynamic Latched Architecture for High Speed ADC

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Abstract: ***In this proposed work, a low offset voltage (mV) and high speed voltage comparator circuit is designed and simulated. With the unceasing rise of various wireless portable communication systems, high speed transceiver circuits, and high speed memory circuit design, sensitized sensor technologies, and wireless sensor network design, the design of high speed, low offset voltage and low power operated comparators are indispensable blocks in the design of a very good analog to digital converter architecture. The proposed work does not entail the usage of any pre-amplification stages, which accounts for the direct reduction of current consumption and silicon area. The MOSFETs at the input differential pair stage of the CMOS comparator circuit are designed to operate in near sub-threshold region rather than in saturation region to account for the low power consumption. The proposed double tail dynamic latched comparator in this work is implemented in 90µm CMOS technology with the operating power supply voltage (V_{DD}) of 1.2 V and sampling frequency of 600 MHz using Microwind EDA tool. The simulated results indicate that the total power consumption is calculated to be of the order of 126.3µw with the delay of 876ps. From the obtained results, the proposed double tail dynamic latched circuit has considerably lowered both the propagation delay time and power consumption, when compared to the previous works.***

Keywords: ***Low offset, low power, gain stages latch and pre-amplifier.***

I. INTRODUCTION

High-speed wide-band data transfer is essential in many modern wireless telecommunication applications, or in a CMOS transceiver circuit or in oscilloscopes or in a wireless local area network receiver.

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Apart from these applications, wireless telecommunication, Blu-Ray or DVD readouts are examples of applications requiring high-speed data transmission. In order to design these high reliable systems, it is vital to integrate the required electronics onto an integrated chip of silicon. Analog to Digital Converter (ADC) circuits are found nearly in all electronic systems such as high-speed line receiver circuits, clock and data signal restoration circuit, threshold voltage detection circuits, peak voltage detectors, zero-crossing detector circuits,
high speed instrumentation, logic level shifting circuits, frequency translation circuits, satellite broadband communication systems,
various oscilloscopes and X-band radar system. The key specifications to be considered in the design and implementation of these systems comprise such as high operating seeds, longer battery operating time, low power, high resolution, less noise generation and reduced silicon area. In order to implement wireless portable systems with such specifications, the design of an ADC circuit is very much crucial and very much indispensable. High-speed data converter circuits are considered to be a vital component in these wireless communication applications.
One such important circuit in these systems is the comparator circuit. Basically a CMOS analog comparator is a circuit used to match two signals and generates which of the input voltages are greater. A comparator circuit in its simplest form comprises of a conventional MOS transistor differential pair with a NMOSFET or PMOSFET current mirror circuit as an active-load, an amplifier stage implemented using common source (CS) configuration and one or more CMOS inverter circuits connected at the output side, which work as an additional amplification stage. The performance of a CMOS comparator circuit can be improved by proper scaling of the dimensions of MOS transistors. Nevertheless, the scaling procedure of CMOS transistors are not implemented directly, as it necessitates high channel doping, gate induced drain leakage and band to band tunneling across the junction. Reducing the aspect ratio of the MOS transistor leads to lowering of several important specifications of the comparing circuit. Also it results in the increased values of offset voltage and major changes in the (1/f) noise levels. One of technique to reduce power consumption of a CMOS transistor circuit is to use V_{DD} voltage reduction technique. In a CMOS realization, the power expression is directly proportional to $(V_{DD})^2$. Conversely, dropping the power supply voltage (V_{DD}) will severely enhance the delay time. Also to compensate for the lowering in power supply voltages (V_{DD}), aspect ratio of MOS transistors are further improved and this would source increased currents in the circuit
and large occupied circuit area.

The important specifications to be considered in the design this CMOS comparator circuit are input voltage range, resolution, conversion rate, and circuit area and power consumption. Sometimes a comparator circuit is also called as a one-bit ADC.

The design of a high speed differential clocked comparator employing bandwidth variation method is employed by Y.Okinawa et al. [1]. A comparator with reduced kickback noise which results in overall power reduction by 50% is described in [2].

The design procedure and simulation of multistage preamplifiers for use in high speed comparators is explained by W.Shirai et al. [3].

A comparator based on differential configuration is analyzed and simulated for use in a successive approximation register (SAR) type ADC is presented in [4]. The comparator uses no pre-amplification stage for comparison of bits. P. M. Figueiredo et al. proposed various kick back noise reduction techniques for CMOS latched comparator circuits [5]. A 4-bit comparator for use in pipelined ADC architecture with reduces offset voltage is describes in [6]. J. He et al. presented a novel balanced method to explore the input referred offset voltages in dynamic comparators [7].

The work in this paper is presented as follows. Section-II describes the general architecture of latch type CMOS comparator circuit. The schematic diagram of the proposed and designed double tail dynamic latched type comparator circuit is explained in Section-III. Various specifications of comparator circuit have been found out and shown in section-IV. Lastly, Section-V gives the conclusions of this work.

II. LATCHED TYPE CIRCUIT

Various comparator circuit topologies exists in literature such as high-speed comparators, multistage open-loop comparator circuits, regenerative latched comparator circuit type and the pre-amplifier based latched comparator type. Selection of comparator architecture is particularly based on the type of ADC architecture [8]-[10]. The design and analysis of comparator circuit is the most critical module in the final implementation of any ADC, as the circuit functioning speed and the resolution levels of the ADC architecture is strongly dependent on the CMOS comparator circuit

Figure 1, displays the block diagram of a general latched type circuit. It mainly comprises of three stages such as the input pre-amplifier stage, a regenerative feedback amplification stage and lastly an output voltage buffer circuit. The pre-amplification circuit stage fundamentally comprises of a differential NMOS circuit pair with PMOS active load stage. The next stage is a decision circuit and it should be able to discriminate very low amplitude signals of the range (µV to few mV). Also positive feedback is employed in decision circuit which is achieved by cross coupling of two NMOS transistors.

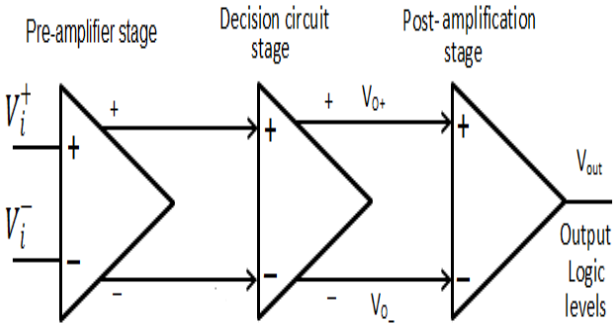

Fig. 1. Comparator block diagram

The last connected stage is an output buffer circuit or post-amplifier circuit. This stage is employed to produce an output logic signal (either high or low).

III. SCHEMATIC OF DOUBLE TAIL LATECHED COMPARATOR CIRCUIT

The purpose of a comparator circuit is to convert input analog signals to output digital signals. The output signal generated is based on the comparison of the two inputs. The schematic diagram of the proposed double tail comparator is shown in fig. 2.The comparator is one of the most commonly used circuits for converting a given input analog signal to output digital signal. In the data conversion process, it is necessary to first sample the input voltages. The performance-specific parameters considered in the design of a comparator circuit are slew rate, input capacitance, speed, kickback noise, offset voltage, power dissipation and input common mode range.

During the reset stage of operation i.e. when CLK=logic low, both tail MOS transistors M_{T1} and M_{T2} are switched off. So the transistors M_3 and M_4 pulls both the nodes F_p and F_n to circuit operating voltage V_{DD}, since transistors M_{C2} and MC1 were switched off. The intermediate stage consisting of transistors M_{R2} and M_{R1} resets both latch stages and connects output to logic zero level. Correspondingly during decision making phase i.e. when CLK=power supply voltage V_{DD}, both the transistors M_{T2} and M_{T1} are turned on. So the drain nodes of transistors M_{C2} and M_C1 i.e. F_p and F_n start to discharge at various rates according to the differential input signals. Now, assume if the input voltage $V_{iP} > V_{iN}$, then the voltage at the node F_n drops faster than F_p, (as transistor M_2 delivers more current than transistor M_1). As long as the voltage at node F_n remains dropping, the corresponding control transistor (M_{C1} in this case) switches on, pulling the voltage at node F_p node back to the operating voltage V_{DD}; so that another control transistor (M_{C2}) switches off, permitting the voltage at node F_n to be discharged totally. Lastly to provide more voltage gain and make the comparator more accurate, simple inverter circuits are connected in cascade at the output side.

IV. SIMULATION RESULTS

The double tail latched comparator circuit design is simulated in CMOS 90nm technology using Microwind EDA tool.

The comparator circuit is operated at 600MHz clock speed and under 1.2V power supply voltage. Generally the delay of the comparator circuit must be less affected by the changes in the input common-mode voltage and thus the comparator circuit is said to possess wider common-mode range.

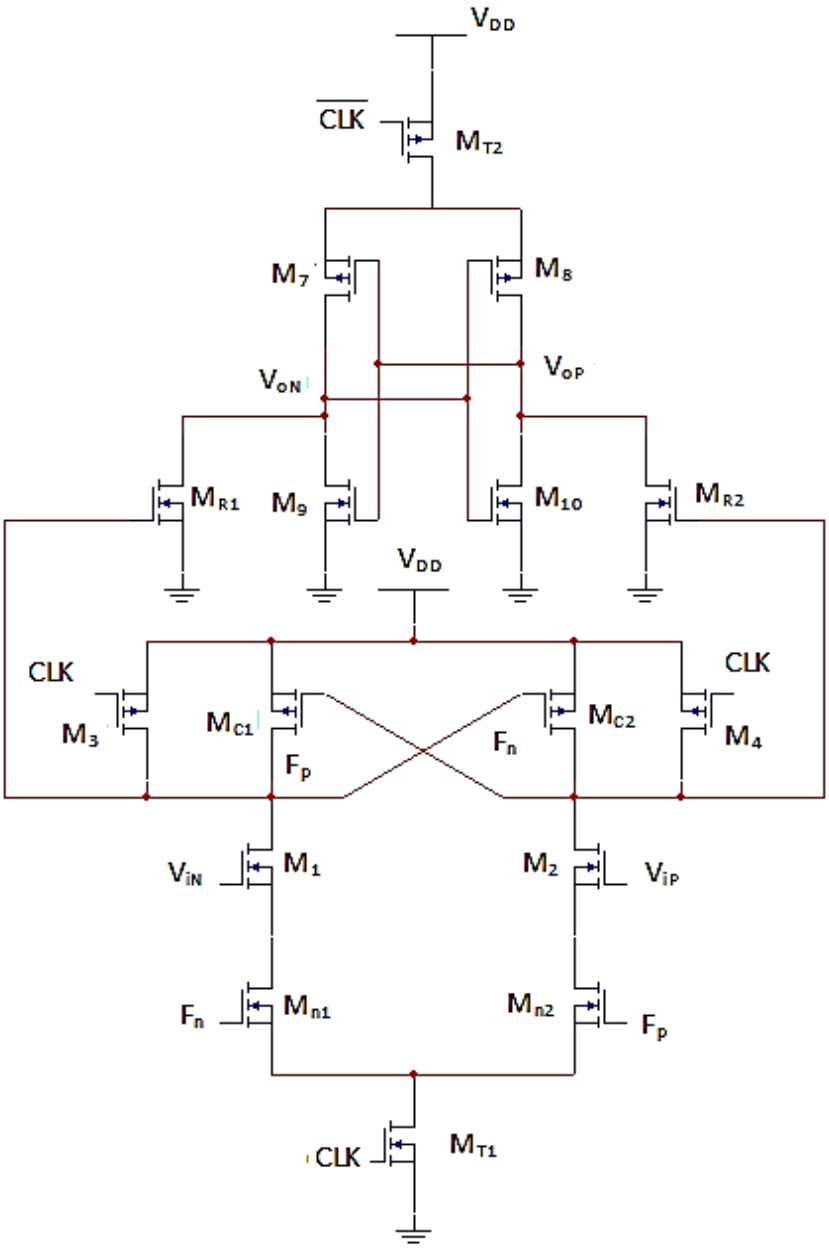

Fig. 2. A double tail circuit

The transient response of double tail latched circuit is presented in Fig. 3.The parameters such as rise time, fall time, propagation delay, operating speed, power consumption and slew rate were measured using transient analysis. The static power dissipation (P_{stat}) of the comparator circuit is calculated mathematically by the product of bias currents in the circuit and the power supply voltage V_{DD}. The calculation of dynamic power dissipation (P_{dyn}) is based on the currents flowing through the transistors, when they are switched between on and off states and vice-versa.

The observed delay is varying between (986-110) ps and it shows a very less variation for wider values of input common mode voltage signals. Fig. 4 shows the results of V_{DD} against propagation delay(ns).

The power-delay product (fJ) is also observed to be lowest and very nearly remains constant for a wide variation in input common signals. Fig. 5 indicates the variation of V_{DD} against power-delay product. The simulation graph for offset voltage curve is presented in Fig. 6.

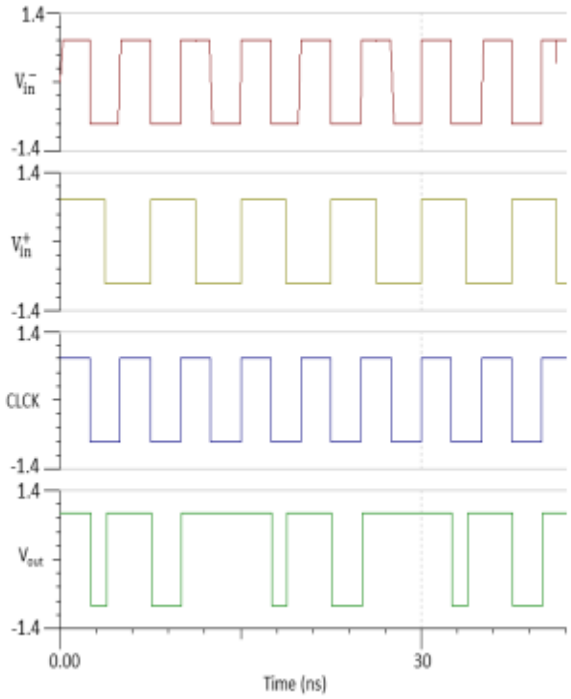

Fig. 3. Transient response

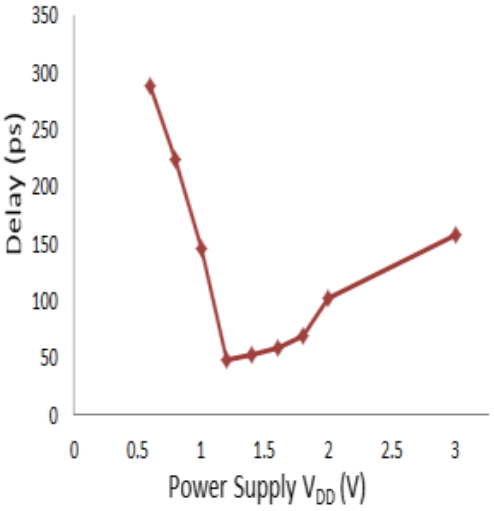

Fig. 4. VDD versus propagation delay

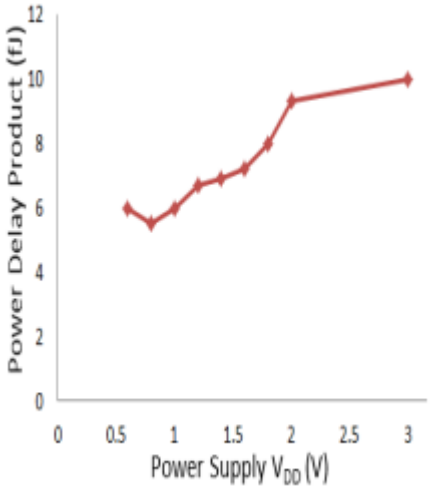

Fig. 5. VDD versus Power delay product

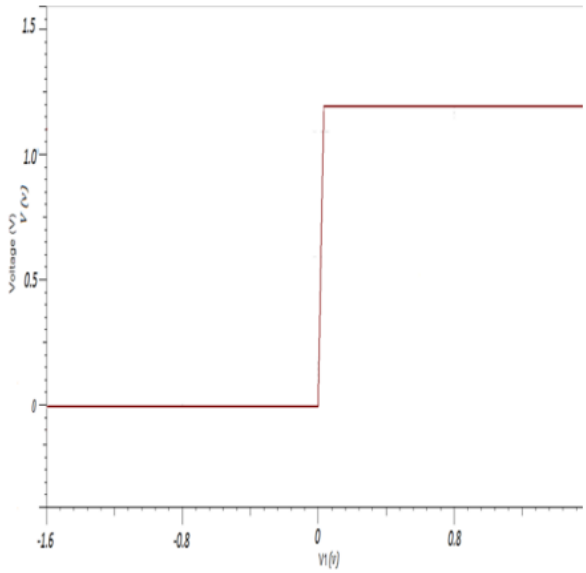

Fig. 6. Offset voltage curve

The obtained values of the simulated double tail latched comparator circuit are presented in Table 1.

Table 1. Summary of results

S.No:	Name of the parameter	Double tail circuit
1	Technology (nm)	90
2	Offset voltage (mV)	1.12
3	Gain (dB)	28
4	Power dissipation (µW)	126.3
5	Operating voltage (V)	1.2
6	Propagation delay(ps)	876
7	Speed (Hz)	1.14G
8	Power-Delay product (fJ)	110.37

V. CONCLUSION

This work presents the design and simulation of a low offset voltage (ΔV_{io}) and low delay CMOS latched comparator circuit architecture. The MOS differential input transistors at the first stage are made to operate in near sub-threshold region reasonably than in the active region in order to achieve low power consumption. The proposed design of double tail latched circuit is simulated and verified in Microwind tool in 90nm CMOS technology. From the obtained simulation results, the latched comparator exhibits a maximum offset voltage of about 1.12mV. The circuit shows an operating delay of 876ps when operated at a DC supply of 1.2V and power consumption is found to be 126.3µw.

From the results obtained, it can be inferred that the latched dynamic comparator circuit can be used in medium resolution and high speed converter architectures such as in successive approximation register and in pipelined architectures.

REFERENCES

1. Y. Okaniwa et al., "A 40Gb/s CMOS clocked comparator with bandwidth modulation technique," in IEEE Jour. of Solid-State Ckts, vol. 40, no. 8, pp. 1680-1687, Aug. 2005.
2. T. Sundstrom and A. Alvandpour, "A Kick-Back Reduced Comparator for a (4-6) bit 3GS/s Flash ADC in a 90nm CMOS Process," Proceedings of the Fourteenth Interl. Conf. on Mixed Design of Intgd. Ckts and Sytms., Ciechocinek, 2007, pp. (195-198).
3. 3. E. Shirai, "CMOS Multistage Preamplifier Design for High-Speed and High-Resolution Comparators," in IEEE Trans. on Ckts. and Systms. - II: Exp. briefs, vol. 54, no. 2, pp. 166-170, Feb. 2007.
4. Krishna K.L., Anuradha K., Murshed A.M., "A 6-bit Low Power SAR ADC", Communication, Networks and Computing-CNC 2018; Springer: Communications in Computer and Information Science, Vol. 839.
5. P. M. Figueiredo and J.C. Vital, "Kickback noise reduction techniques for CMOS latched comparators", Circuits and Systems II: Express Briefs IEEE Transactions on, vol. 53, no. 7, pp. 541-545, 2006.
6. K.Lokesh Krishna and T. Ramashri, "VLSI Implementation of 4-bit 50Gbps High Speed Pipelined ADC architecture for I-UWB Receiver", International Journal of Computer Appls., vol.57, no.15, pp. 32-37, November 2012.
7. He, J., Zhan, S., Chen, D., and Geiger, R.L.: Analysis of Static and Dynamic Random Off-set Voltages in Dynamic Comparators. In IEEE Trans. on Ckts. and Sysms-I: Regular Papers, 56 (5), 911-919, May 2009.
8. Phillip E.Allen and Douglas R. Holberg, 2013, "CMOS Analog Circuit Design", Second edition, Oxford University Press.
9. B. Razavi, Principles of Data Conversion System Design. New York: IEEE Press, 1995.
10. 10.R. Jacob Baker.: CMOS Circuit Design, Layout and Simulation. 3rd Edition, IEEE press, A John Wiley & Sons, USA (2014).

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