Abstract: Historically, travelling wave tube amplifier (TWTA) has been a common type of Microwave amplifier used commonly in terrestrial and space application due to their high efficiency and power handling capacity. However due to their bulky nature and also being very expensive, it is difficult to use them commercially in a large scale. Inspired by the advantage such as very less development cost, minimum supply voltage, gradual degradation and numerous commercial applications, Solid State Power Amplifier (SSPA) has been the replacement to vacuum tube Technology. The efficiency of the amplifier is one of the most important task in the microwave engineering research. An important figure of merit, power-added efficiency (PAE), is the main focus. Hence in this paper, class F Power amplifier is designed for 2.4GHz frequency. Class F Amplifier is also called as wave shaping amplifier since the harmonics generated helps the amplification process. The class f PA is biased nearer to the class B amplifier (close cut-off area) so the transistor can move back and forth rapidly to produce the harmonics. The efficiency of class F amplifier depends on how many harmonics are used for the amplification process. Here, the amplification process is performed up to the third harmonics which provides 41.606 dBm output power with 27dBm input power. Also a gain of more than 20.277dBm is achieved when the input given is 27dBm. Several other results like reflection Coefficient and transmission coefficient simulations has also been provided with the power added efficiency (PAE) of 75.402 achieved has also been simulated.

Keywords: class F, CGH40010, PAE, S-band, third harmonics.

I. INTRODUCTION

In the commercial microwave communications arena, the communication systems are making use of complex modulated schemes to accommodate increased bandwidth demands. Hence this schemes are characterized by highly varied envelopes which are operated at less than their peak of foot power commonly referred to as back of condition which usually requires power amplifiers. The power amplifier’s effectiveness is thus drastically decreased, requiring a bigger heat sink with extra dissipated power. The power amplifier is basically characterized by the parameter called Power Added Efficiency (PAE). This parameter measures the capability of converting direct current power to radio frequency power by a power amplifier.

There are several methods employed to increase the power added efficiency in the back of operation conditions hence by boosting the efficiency of the radio frequency PA in all conditions like envelope Estimation and restoration (EER) and digital pre-distortion. Power amplifier involves classes like class F, class D, class S, class E, inverse F to engineer the different current and voltage waveforms such that there is a minimum drain of the transistor hence minimizing power dissipation and boosting effectiveness[1]. Class F RF power amplifiers uses multi-harmonic resonators in the input side of the circuit to model the \( V_D \) as shown in fig1.1, thereby reducing loss in the transistor and increasing efficiency. Class F power amplifier circuits are also called highly efficient power amplifiers due to their nature of polyharmonic or multi-resonant design methodology. The current in the drain part of the transistor starts flowing when the \( V_D \) is flat and small, and when the drain stress is zero.

Fig 1.1: Basic design block diagram of class F power amplifier [2]

The first process starting with the PA requirements and electrical specifications with the selection of the technology with which the amplifier is going to be designed, then subsequently the selection of the transistor type. The targeted implementation and the necessary operating frequency select the latter.

II. DESIGN METHODOLOGY

This section gives a broad overview of the design methodology of the power amplifier along with the block diagram. Here the design flow of the power amplifier is explained with the flowchart. After properly selecting the active device, the subsequent step is to select the preliminary PA structure needed to meet the electrical requirements. Such broadband buildings are connected by the active device transconductance, enabling the signal traveling on the TL to be amplified into the signal traveling on the TL drain.

The steps involved in this process of designing an class F power amplifier is as follows [5],

- Device selection
- DC bias point selection
- Device characterization
  - I-V characterization
  - S-parameter measurement
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- Power amplifier measurements

Figure 2.1 flowchart demonstrates the Class-F power amplifier design flow and measure different parameters. The Cree CGH40010F GaN transistor is a 10-W instrument with outstanding output and corresponding features at frequencies up to 6 GHz and has been chosen for this purpose.

Typically, for moderate to big bandwidths, the corporate solution is featured and hence its nonlinear broad signal. Appropriate PA design strategies are introduced based on load-line ideas. In reality, a single-ended solution is the most natural option if the chosen device can execute the necessary output signal level, efficiency and gain. If the single unit is unable to deliver the necessary gain, a solution that implies a driver (gain) phase becomes compulsory, moving to a multi-stage single-ended solution.

### III. DESIGN OF POWER AMPLIFIER

This section explains the class F power amplifier design for 2.4GHz along with the specifications. The transistor is biased for Vds=28V, Id=205mA, Vgs=-2.7V. This section also gives the information about the load analysis, technique to match the transistor, schematic and the layout of the Radio frequency power amplifier.

Here resistor of 28ohms is added at the base of the voltage divider circuit to increase the stability of the circuit. From the figure 3.2, it is clearly evident that stability factor obtained is 1.56 which is more than the required value of 1.5 for a transistor to be stable for the applied voltage. Also the gain of the small signal analysis of an amplifier is calculated by (1) by substituting output power and input power specified in the data sheet as 40dBm and 27dBm respectively resulting in the gain of 16 dB which is shown in the figure 3.2.

\[
\text{Gain} = 10 \log_{10} \frac{P_{\text{out}}}{P_{\text{in}}} \tag{1}
\]

Similarly stability of the small signal analysis of an amplifier is calculated by (2) and (3) by substituting the s-parameter values which can be obtained in the data sheet of the transistor whose values are given in the table 3.2 resulting in the stability factor is 1.556 which is more than the required threshold value of 1.5 required for the transistor to work in the stable condition which is shown in the figure 3.2.

\[
K = \frac{1-S_{11} S_{22} + d}{2 S_{12} S_{21}} \tag{2}
\]

\[
\text{Where, } d = S_{11} S_{22} - S_{12} S_{21} \tag{3}
\]

Figure 3.3 and 3.4 is the simulation for the input and output reflection co-efficient and transmission co-efficient obtained through s-parameter smith chart. S-parameter provided from the simulation is shown in table 3.2. From the table 3.2, we can that the values obtained from the smith chart at Vds 28V and Idq 200mA are S(1,1)= 0.912/163.971, S(1,2)=0.021/-32.869,S(2,1)=0.049/44.520, S(2,2) =0.387/-158.630. From the above two tables, we can come to conclusion that even though the simulated and data sheet values are closer but they are not equal.
Figure 3.3 shows the schematic for S-parameters. There are S parameters provided in the datasheet under 3 different DC bias conditions. Here the stability is verified for the range of 100MHz to 6GHz. When the load and source impedance is pointed on the right-side of the smith chart, then the system is unconditionally stable as shown in fig 3.3. Here the stability is verified for the range of 100MHz to 6GHz. The simulated S-parameters from the ADS model including the magnitude and phase are nearer to the experimental S-parameters provided in datasheet.

It can be assumed that the CGH40010 transistor model using S-parameters for computation is accurate enough so that the simulated results will be able to accurately describe the actual PA performance as shown in fig 3.4.

Figure 3.5 is a schematic for the load pull analysis to find out transistor load matching. From the table 3.1, it can be seen that different source and load impedances are obtained along with power and PAE counter by repetitive iteration. In the fourth iteration, power and PAE is obtained for load impedance 6.109+j21.719. From the figure 4.8 we can observe that the load is matched for (6.109+j21.719) to get the maximum power counter level of 40.37dBm with the maximum power added efficiency counter level of 66.847%. This process is achieved by the iteration method till we find out the exact matching of the transistor.

Table 3.1- S-parameters values from the data sheet [7]

<table>
<thead>
<tr>
<th>Vds and Idq</th>
<th>S11</th>
<th>S12</th>
<th>S21</th>
<th>S22</th>
</tr>
</thead>
<tbody>
<tr>
<td>28V and 100mA</td>
<td>0.889/169.48</td>
<td>0.026/-28.08</td>
<td>3.97/45.24</td>
<td>0.418/-144.45</td>
</tr>
<tr>
<td>28V and 200mA</td>
<td>0.895/166.96</td>
<td>0.021/-22.08</td>
<td>4.20/46.33</td>
<td>0.393/-155.54</td>
</tr>
<tr>
<td>28V and 500mA</td>
<td>0.900/165.49</td>
<td>0.019/-17.95</td>
<td>4.21/46.94</td>
<td>0.390/-162.93</td>
</tr>
</tbody>
</table>

Table 3.2- S-parameters values from the simulation

<table>
<thead>
<tr>
<th>Vds and Idq</th>
<th>S11</th>
<th>S12</th>
<th>S21</th>
<th>S22</th>
</tr>
</thead>
<tbody>
<tr>
<td>28V and 100mA</td>
<td>0.880/163.48</td>
<td>0.026/-26.68</td>
<td>3.90/65.74</td>
<td>0.423/-154.75</td>
</tr>
<tr>
<td>28V and 200mA</td>
<td>0.912/163.971</td>
<td>0.021/-32.869</td>
<td>4.049/44.520</td>
<td>0.387/-158.630</td>
</tr>
<tr>
<td>28V and 500mA</td>
<td>0.910/146.79</td>
<td>0.019/-19.925</td>
<td>4.37/49.04</td>
<td>0.395/-179.73</td>
</tr>
</tbody>
</table>

Figure 3.6 is a schematic for the load pull analysis to find out transistor load matching.
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Fig 3.7- Schematic of load-pull analysis result values

Table 3.1- Source and load impedance reading at different iteration in load-pull analysis

<table>
<thead>
<tr>
<th>Z_source</th>
<th>Z_load</th>
<th>Power counter level(dBm)</th>
<th>PAE counter level (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.041+j8.283</td>
<td>-</td>
<td>32.62</td>
<td>22.019</td>
</tr>
<tr>
<td>0.283+7.375</td>
<td>6.109+j21.719</td>
<td>35.41</td>
<td>41.186</td>
</tr>
<tr>
<td>0.661+6.43</td>
<td>6.109+j21.719</td>
<td>38.32</td>
<td>57.126</td>
</tr>
<tr>
<td>0.916+5.507</td>
<td>6.109+j31.719</td>
<td>40.37</td>
<td>66.847</td>
</tr>
<tr>
<td>0.977+5.303</td>
<td>-</td>
<td>41.21</td>
<td>40</td>
</tr>
</tbody>
</table>

The schematic shown in the fig 3.8 is the third harmonics type of resonator used in the class F power amplifier. It consists of a transistor, load network, and RF choke (RFC). Three capacitors of value 4.5pF, 10pF, 33pF are used to block the gate power and drain power to pass through the input terminal which results in the reflection loss.

Fig 3.8- Design of the tank circuit for the third harmonics

Fig 3.9- capacitor used to block the spurious generated in the gate and the drain source connected to the transistor

Having said with all the above section of the PA, the complete schematic of the power amplifier can be seen in figure 3.10. The incoming signal is given through p_tone with 27dBm input signal power along with drain and gate source and output is drawn at the load terminated with TERM_G. From the schematic, the layout is generated which is shown in figure 3.11. Figure 3.12 shows the generated layout along with all the elements associated with it.

Fig 3.10- Schematic of the complete power amplifier design

Fig 3.11- Layout generated from the schematic

Fig 3.12- Layout of the complete power amplifier design
IV. RESULTS

This section provides the complete results of small scale signal and large scale signal simulation of the class f PA for 2.4GHz frequency. The results includes stability analysis, 1dB compression, power added efficiency (PAE), harmonic balance analysis, transmission coefficients (S12, S21) and reflection coefficients (S11, S22).

![Stability analysis](image1)

**Fig 4.1- Result of the small signal Stability analysis**

Figure 4.1 is the result of the stability analysis of the transistor at the given drain to source voltage 28V. Here the analysis is done by varying the gate voltage. At 2.4GHz, the stability factor is 1.556 which is more than the required threshold value of 1.5 required for the transistor to work in the stable condition. Figure 4.2 shows the gain and the noise figure analysis in which the gain obtained is 16.266 also the noise figure is very less at 2.4 gigahertz frequency.

![Gain and Noise figure analysis](image2)

**Fig 4.2- Small signal Gain and Noise figure analysis of transistor**

![Output voltage vs input power](image3)

**Fig 4.3- Graph of Vout vs Pin**

Figure 4.3 is the graph to show the output voltage versus the input power provided. From the marker1, it can be observed that the output power obtained is 41.606dBm for input 27dBm power with the gain obtained by this power amplifier is 20.277. Figure 4.4 is the curve for the PAE of this power amplifier which is 75.402 which means 75% of the drain power it is used for the amplification process. Figure 4.5 is the result of the harmonic balance simulation of the power amplifier to find out the maximum output power at 2.4 gigahertz frequency. From the marker7, we can verify that the output power obtained is 41.606dBm.

![Harmonic balance analysis](image4)

**Fig 4.4- Curve of PAE (Power Added Efficiency)**

![Output power of EM simulated final layout](image5)

**Fig 4.6-Output power of the EM simulated final layout**
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Fig 4.7- Power added efficiency (PAE) of the EM simulated Final Layout

Figure 4.9 and 4.10 shows the performance of the power amplifier layout with the generated output power and the efficiency respectively. From the figure, we can analyze that the layout performance is slightly less than that of a schematic performance.

V. CONCLUSION

Due to the broad band gap, GaN is selected for high power applications and high electron mobility compared to Silicon and GaAs. Amplifier Class-F offers better efficiency but bad linearity. The Efficiency, Output Power, Gain, Return Loss, Insertion Loss, 1-dB Compression Point, Better Efficiency and Power are accomplished by completely biasing the transistor to the appropriate application.

The amplifier Class-F is designed and simulated in ADS using Lumped elements. Maximum output, gain and power added efficiency of 41.606dBm, 20.277dB and 75.402 percent were achieved by the lumped elements Class-F PA circuit at 2.4GHz operating frequency, 27 dBm input power and Vds=28V and Vgs=−2.8V bias point respectively.

A series or parallel transmission lines or Taper can be included as a compensation circuit in the output network to absorb the impact of the packaged transistor's internal parasite parts. This in turn increases the complexity of the output network, but enhances Class-F PA's efficiency. The insertion loss obtained is around-4 which can be enhanced to achieve better efficacy. It is possible to increase output power and efficiency by using distinct harmonic circuits such as 5th harmonics or infinite harmonics (Transmission Lines).

REFERENCES

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