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Conducted Emi Model for Flyback PFC Converter

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Abstract*: Power Factor Correction (PFC) units are used at the front end of Switched Mode Power Supply (SMPS) to improve the input power factor. However, they generate Electromagnetic Interference (EMI) which needs to be mitigated to compliant levels prescribed by International Standards. The Electromagnetic Compatibility (EMC) standards have set regulations which require expensive instruments and environment for their measurement. Hence there is a need for predicting Conducted EMI by simulation before the product is tested for full compliance to reduce the complexity of the circuit design and cost. To estimate the Conducted EMI, it is important to identify the main noise sources and their conduction paths. This can be achieved by simulating the circuit using the exact models of the transformer, capacitor, PCB trace, and the switching semiconductors. In this paper these components of PFC flyback converter are modelled using SPICE models, datasheet defined component parameters and experimental measurements. The theoretical analysis and simulation results show that the method discussed can predict and analyse the Conducted EMI. This is tested experimentally on a Flyback PFC converter working in Critical Conduction Mode. A line filter is designed and used to bring the noise to compliant levels. Simulation and Experimental results after using the line filter are also presented.

***Keywords*: EMI, LISN, Power Factor Correction (PFC) converters, Differential Mode (DM) Conducted EMI, Common Mode (CM) Conducted EMI, Flyback converter.**

I. INTRODUCTION

Most of the consumer electronic appliances and computers connected to utility mains are powered by Switched Mode Power Supply (SMPS). The SMPS is popular because of its lightweight, efficient, small size, economical but they offer low power factor, high harmonics and Electromagnetic Interference (EMI). To improve the power factor of the SMPS, power factor correction (PFC) circuits are used in their front end. Currently, these circuits use dc-dc converters and special integrated circuits working as active Power Factor Controller (PFC). These circuits maintain the power factor and reduce the harmonics. Flyback PFC working in low power is used in many consumer electronics such as LED drivers and power adapters. But they switch at very high switching frequency generating EMI.

The trend in power electronics is to minimize the size of the energy storage elements by adapting to high switching frequency converters. Therefore, high switching frequency and fast semiconductor devices is a basic requirement for power supply designing. However, noise current and voltage (high dv/dt and di/dt noise), is increased due to the increased in switching frequency. This will have a disadvantageous effect on the EMI performance. Commercial electronic appliances powered by SMPS cannot be permissible on the market until certain Electromagnetic Compatibility (EMC) regulations are met. In up to date, EMC regulations have turned to be more stringent. [1]

There are two modes of EMI: Conducted and Radiated. CISPR 22, IEC 2003 [1-2] standards describe the Conducted EMI frequency range from 150 kHz to 30 MHz and Radiated EMI frequency range from 30 MHz to above 1GHz. Conducted EMI is divided into Differential Mode (DM) Conducted EMI and (2) Common Mode (CM) Conducted EMI.

DM noise currents flowing through line or neutral and returning through line or neutral wires are recognized as Differential Mode Conducted EMI. They flow in opposite directions in the line and neutral with equal in magnitude. Differential Mode Noise is mainly caused by the harmonics of the switching current, if the slope of the switching current di/dt is high, the amplitudes of various harmonics are high.

CM noise current flowing among line and neutral and returning by means of ground are recognized as CM Conducted EMI. Their directions are the same in line and neutral wires. They are measured between line or neutral and earth. CM Conducted EMI is predominantly precipitated due to the displacement current flowing through transformer parasitic capacitances and parasitic capacitance between high dv/dt nodes to ground [3]. EMI problems in offline power converters are strongly related to the high dv/dt and di/dt electrical noise.

Modelling and Simulation are common tools in designing power converters. Development of accurate models allows one to analyse the converter features such as Power Factor Correction (PFC), efficiency and also EMI properties. In designing a converter noise model there is always a trade-off between accuracy and cost.

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Therefore, finding an optimized model is necessary so that this trade-off is surpassed. Parameter extraction by using manufacturer datasheet, supported by laboratory equipment is relevant to reduce the model cost and to maintain accuracy. Therefore, exact models of components are developed and its values are calculated. After assembling the entire module of the converter, simulation is done using LTspice software to obtain the noise voltages. By performing the FFT conversion of this noise voltage the Conducted EMI is obtained in the frequency spectrum between 150kHz to 30MHz.

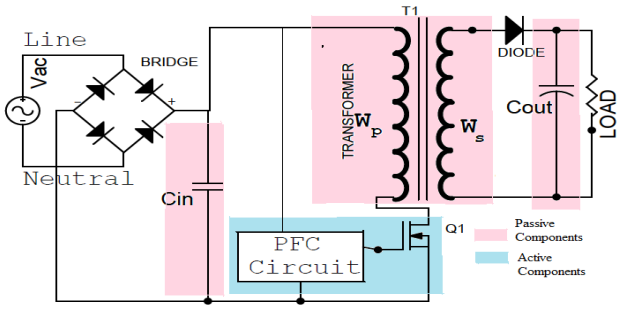

Fig. 1. Flyback PFC Converter

In order to assess the Conducted EMI in a PFC flyback converter, it is necessary to characterize voltage potential and parasitic capacitances in the converter circuit. The converter components can be divided into active and passive components as shown in Fig.1. In active components, the high dv/dt noise generated by high switching MOSFET is the main source of the noise. The passive components include input/output capacitor and transformer. The transformer poses inter-winding and layer to layer parasitic capacitance. The Equivalent Series Inductance (ESL) of the Input and output capacitor plays a crucial role in High Frequency (HF) performance of the converter. The ESL and capacitance can resonate and make a capacitor perform like an inductor at HF range; therefore, it is important to measure the ESL of input/output capacitors.

The organization of this paper is distributed into three sections. In section II, a brief introduction is given about the model adopted, in section III, the simulation of the EMI model of the conventional flyback converter is discussed. LTspice software tool is employed to estimate the Conducted EMI levels in the frequency range of 150kHz to 30MHz and EMI filter design procedure is presented.

II. MODEL OF FLYBACK CONVERTER

In order to perceive an effectual and economical method to mitigate Conducted EMI in power converters, there is a need for predicting Conducted EMI. Modeling the power converter circuit is one of a reasonable way to predict the Conducted EMI. In this section, the principles of Conducted EMI modeling are employed on PFC flyback converter. Noise sources, propagation path, and LISN are modeled separately and then combined as a complete Conducted EMI model of a PFC flyback converter. The PCB traces affecting EMI is also investigated.

A. Transformer model

The parasitic parameters have a major influence on the Conducted EMI. The CM Conducted EMI is caused due to the displacement current flowing through the transformer parasitic capacitances. A normal conventional wound transformer used in a typical flyback SMPS is considered for the study as shown in Fig. 2 and Fig. 3. Usually, such transformer offers primary leakage inductance (l_{w1}), secondary leakage inductance (l_{w2}), distributed parasitic capacitance such as,

1. Primary layer-layer parasitic capacitance (C_{l1}),
2. Secondary layer-layer parasitic capacitance (C_{l2}),
3. Inter-winding parasitic capacitance (C_w).

The winding resistances r_{w1}, r_{w2} are also considered as shown in the equivalent circuit of the flyback transformer in Fig.4.

The conventional flyback transformer is employed with EE core. Fig. 2 shows the cross-sectional view of the flyback transformer, further a half window of the transformer is considered for investigation as shown in Fig. 3. The flyback transformer windings are divided into three windings: W_p is the primary, W_a is auxiliary and W_s is the secondary winding. For every two layers in the W_p and W_s there is distributed parasitic capacitance. Those parasitic capacitances in W_p is C_{l1} and W_s is C_{l2}. The C_{l1} contributes to CM Conducted EMI but the displacement current generated by it is confined within the primary side of the converter. The distributed parasitic capacitance C_w between W_p and W_s yield the major path for the CM Conducted EMI from primary to secondary side of the PFC converter. As the impedance of the core is smaller than the winding to core parasitic capacitance. Therefore, parasitic capacitance between W_p to core and W_s to core can be neglected.

The leakage inductance of transformer resonates with the parasitic capacitances which form a major source of CM Conducted EMI. The CM Conducted EMI propagation path has a low impedance which results in relatively high CM noise peak. The parasitic capacitance and leakage inductance resonate with the junction capacitance of the transformer secondary side fast switching diode. It also introduces high-frequency CM noise peak.

The displacement current of the primary can come to secondary through parasitic capacitance C_w. The turn to turn capacitances are very small and hence it can be neglected. The value of C_w, C_{l1} and C_{l2} capacitance can be measured by using Vector Network Analyzer (VNA). The transformer primary impedance is measured with secondary open circuited as shown in Fig.5.

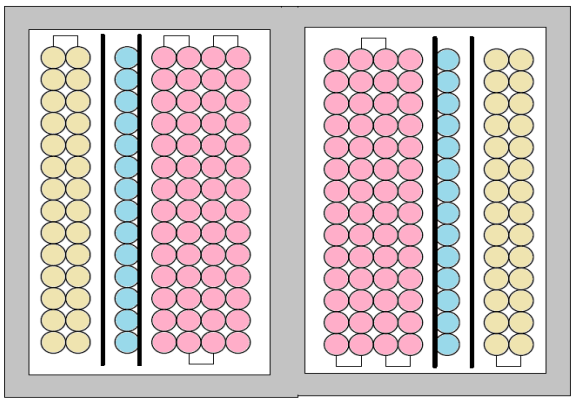

Fig. 2.A cross-sectional view of the flyback transformer

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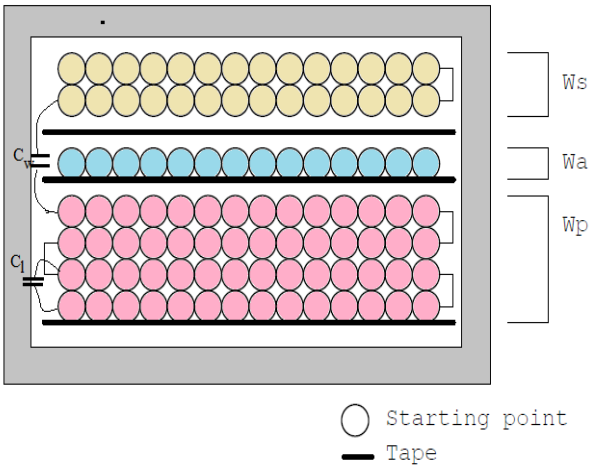

Fig. 3.The half window of the flyback transformer represented in Fig.2

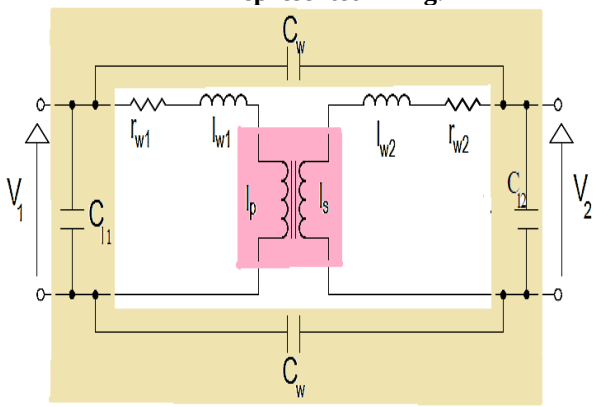

Fig. 4.Flyback transformer model

There are two peaks f_1, f_3 and one valley f_2 of resonance frequency measured across transformer primary impedance with the secondary open circuit as shown in Fig. 5. From these peaks and valley, the resonant frequency equations [4-5] are as follows;

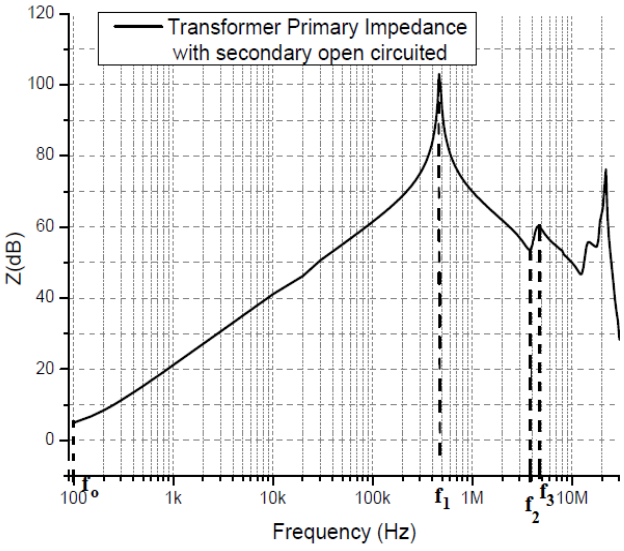

Fig. 5.Primary resonance frequency measured using VNA

$$f_0 = \frac{r_1}{2\pi L_0} \rightarrow (1)$$

$$f_1 = \frac{1}{2\pi\sqrt{L_0(C_1 + C_2)}} \rightarrow (2)$$

$$f_2 = \frac{1}{2\pi\sqrt{l_w(C_2 + C_3)}} \rightarrow (3)$$

$$C_{l1} = C_1 + C_2$$

$$C_{l2} = C_2 + C_3$$

$$C_w = C_1 + C_3$$

In Table1, the results of the parasitic capacitance and leakage inductance calculated is presented.

Table1: Parasitic Capacitance and leakage inductance values of the flyback transformer

Notation	Description	Values
L_0	Primary Inductance	800uH
l_w	Leakage Inductance	25uH
r_{w1}	Equivalent Series Resistance	0.5Ω
C_{l1}	Primary layer-layer parasitic capacitance	156pF
C_{l2}	Secondary layer-layer parasitic capacitance	82.7pF
C_w	Inter-winding parasitic capacitance	73pF

B. MOSFET model

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a popular type of transistor used in power converters. Extraction of model parameters to match the real MOSFET features is a crucial issue in model optimization. Here parameter extraction is done from the manufacturer datasheet.

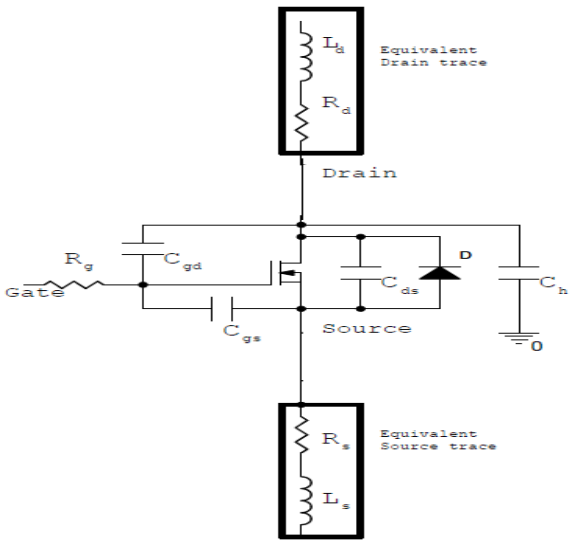

Fig. 6.MOSFET model and heat sink to MOSFET capacitance Ch

As addressed in the preceding section, active elements such as the switch and diode are critical noise sources in converters. Therefore, an accurate model of active elements to estimate the Conducted EMI magnitude is needed.

This model contains complete characteristics such as C_{gs}, C_{gd}, and C_{ds} for MOSFET. In addition to the component parameters considered in the SPICE model, drain and source terminal inductances are added to the switch model.

A traditional MOSFET model as in Fig. 6, with parasitic capacitance C_{gs}, C_{gd}, C_{ds} and resistance R_g, R_d, R_s are considered. The gate input resistance R_g increases the switching speed of the MOSFET, which directly has an effect on the voltage pulsating [6]. That means smaller the value of R_g, CM noise current will increase. The charging and discharging behaviours of C_{gs}, C_{gd} and C_{ds} may influence the switching stress of MOSFET. The SPICE model of the MOSFET is based on the values given in the datasheet which is tabulated in Table 2. Power MOSFET is STP8NM60 is used.

Table 2: MOSFET Datasheet extracted parameters

		Typ	max
C_{iss}	Input capacitance	925pF	1210pF
C_{oss}	Output Capacitance	130pF	175pF
C_{rss}	Reverse transfer Capacitance	32pF	45pF
V_{ds}	Drain-source voltage	25V	600V

To simplify the analysis, the MOSFET SPICE model parameters are tabulated in Table 3 and the parameters calculated can be formulated as follows;

$$C_{gd,max} = C_{rss,\max} - C_{rss,avg} \rightarrow (4)$$

$$C_{gd,min} = C_{rss,avg} \rightarrow (5)$$

$$C_{gs} = C_{iss} - C_{rss} \rightarrow (6)$$

$$C_{ds} = C_{oss,avg} - C_{rss,avg} \rightarrow (7)$$

$$C_{rss,avg} = 2C_{rss,\max}\sqrt{\frac{V_{ds}}{V_{ds,\max}}} \rightarrow (8)$$

$$C_{oss,avg} = 2C_{oss,\max}\sqrt{\frac{V_{ds}}{V_{ds,\max}}} \rightarrow (9)$$

Table 3: MOSFET SPICE model parameters

Parameter	Model Index	Value	unit
V_{to}	Threshold voltage	5.3	V
R_d	Drain resistance	650m	Ω
R_s	Source resistance	50m	Ω
R_g	Gate resistance	4	Ω
lambda	Channel length modulation	0.05	1/V
K_p	Transconductance parameters	1	A/V^2
C_{gdmax}	Gate-drain overlap capacitance maximum	27p	F
C_{gdmin}	Gate-drain overlap capacitance minimum	18p	F
C_{gs}	Gate-source overlap capacitance	1165p	F
C_{ds}	Drain-source overlap capacitance	53p	F
C_{jo}	Zero bias bulk junction bottom capacitor per sq meter of the junction area	0.3n	F/m^2
I_s	Bulk junction saturation current	13p	A
V_{ds}	Drain to source voltage	600	V
R_{on}	Static Drain-Source on resistance	1.6	Ω
Q_g	Total gate charge	13	nC

The heat generated due to the high switching action of MOSFET is dissipated through the heat sink connected to it through an insulating material. There will be a parasitic capacitance C_h between the MOSFET and heat sink and it is at a high dv/dt point to the ground. This parasitic capacitance is determined by equation 10 [7],

$$C_h = \frac{\mu_o \mu_r S}{d} \rightarrow (10)$$

S is the surface area of the MOSFET body,
d is the thickness of the insulating materials AL_2O_3, μ_r=8.5
In equation (10) the surface area of the device is 2.5 cm and 0.01 cm AL_2O_3 is the insulator, the parasitic capacitance is calculated to be C_h = 89pF. For fast switching diode and rectifiers, the junction capacitance (Cj) value is employed in SPICE model. Therefore, a separate diode model is not discussed here.

C. LISN model

Line Impedance Stabilization Network (LISN) is an equipment used for measuring the Conducted EMI as specified by CISPR 22 standards. There are three main functions of LISN. Firstly, LISN acts like a filter which isolates the noise from the power grid such that the EMI receiver measures only the noise received from the EUT (Equipment Under Test) [8].

Secondly, to maintain the 50Ω impedance to EUT throughout the working frequency range and finally to couple the Conducted EMI noise signal from EUT to the EMI Receiver. The SPICE model of the LISN used here for experimentation is shown in Fig. 7 [9].

D. Trace Model

Most EMI issues in switching electronic circuits are firmly associated to the parasitic elements introduced by the Printed Circuit Board (PCB) traces. The parasitic inductor of the PCB trace at high frequency makes the electrical behaviour of the capacitor more like that of an inductor. Thus to accurately describe a PCB trace model, the parasitic inductance can be lumped together as Equivalent Series Inductance (ESL).

However, for PCB traces, only critical values of Inductances are considered. Critical traces are those involved in high switching points like high dv/dt and di/dt loops [10]. The capacitive coupling between the traces are ignored as it has been assumed that the trace distance is large [10].

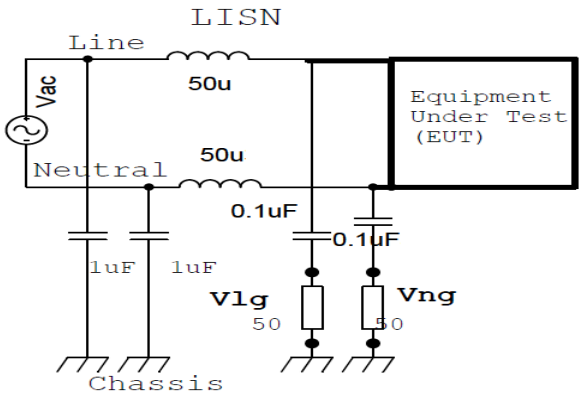

Fig. 7.LISN model used for simulation

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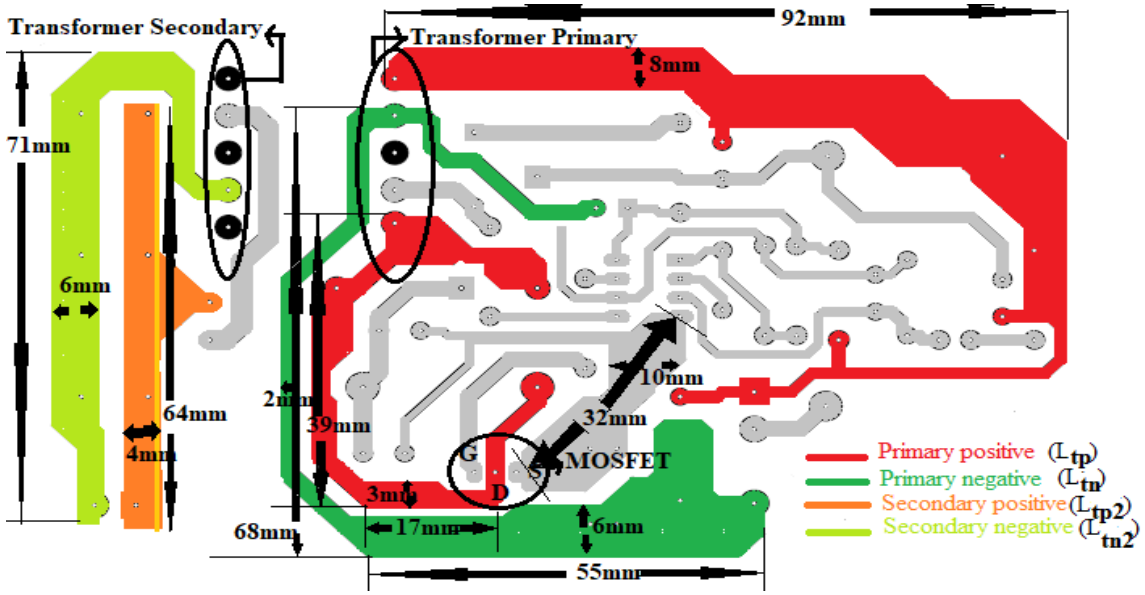

Fig. 8.Model of PCB Trace

The empirical formulae used here to calculate parasitic parameters of PCB trace is as mentioned in [10]. In the Fig. 8 the ESL for a rectilinear trace of thickness t=0.0347mm length *l* and width *w* is given by Equation 11 and the values are tabulated in Table 4.

$$L_{self} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right)+\frac{1}{2}+\frac{0.2235(w+t)}{l}\right] \rightarrow (11)$$

In Table 4 the parasitic inductance of trace calculated analytically is represented.

Table 4: Trace parasitic inductance calculated

	Length (l)	Width (w)	Inductance (H)
L_{tp}	114mm	8mm	88n
L_{tn}	68mm	2mm	64n
L_{tn}*	55mm	6mm	38n
L_{tp2}	64mm	4mm	50n
L_{tn2}	71mm	6mm	52n
L_d	56mm	3mm	46n
L_s	32mm	10mm	15.5n

E. Capacitor Model

The ESL of the capacitor plays a very important role in the high frequency Conducted EMI generation. Therefore, it is very important to measure ESL of the capacitor which is done using VNA as shown in Fig. 10 and Fig. 11.

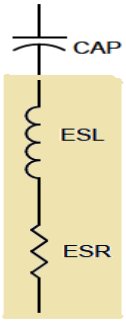

Fig. 9.Model of capacitor

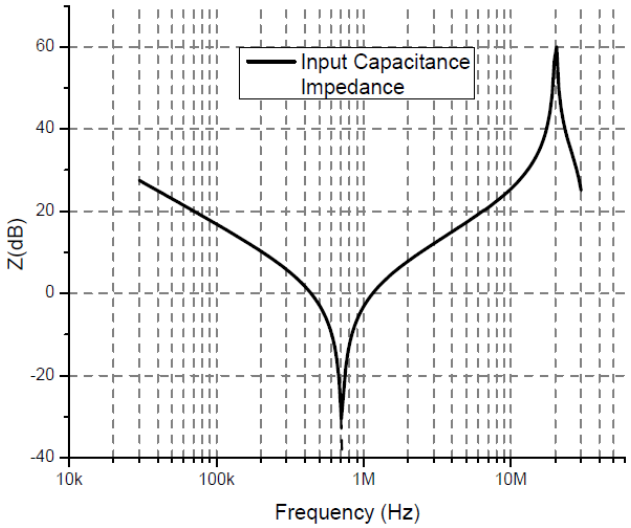

Fig. 10. Impedance characteristics of the input capacitor

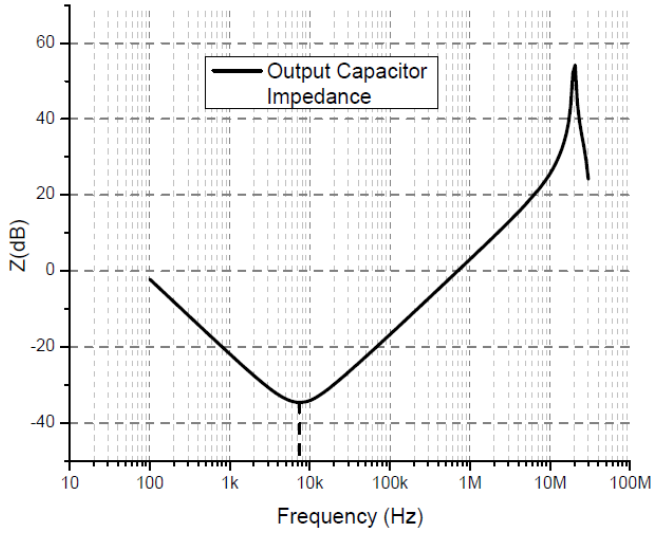

Fig. 11. Impedance characteristics of the output capacitor

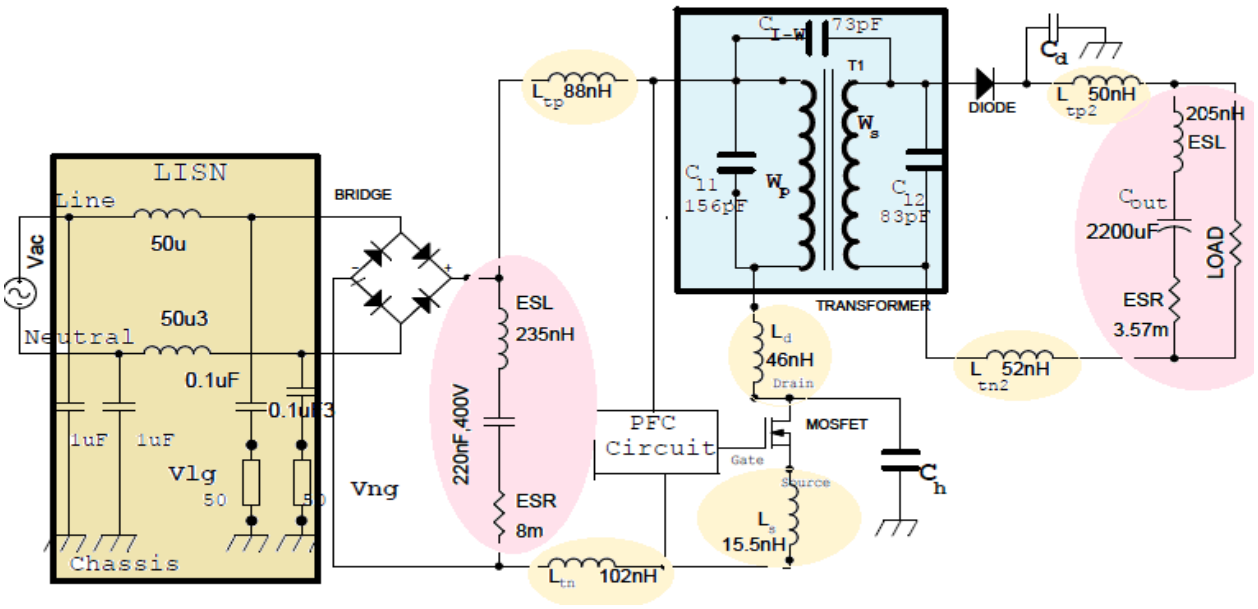

Fig. 12. Model of a PFC Flyback Converter

The series resonant frequency equation 12 and transfer gain equation 13 of the capacitor is given by;

$$f_c = \frac{1}{2\pi\sqrt{ESL \times C}} \rightarrow (12)$$

$$T_c \approx 20 \times \log\left(\frac{ESR}{25}\right) \rightarrow (13)$$

In Table 5 the calculated value of ESL and ESR for input and output capacitor are listed.

Table5: Capacitance parasitic inductance calculated

	Capacitance	ESL	ESR
Input Capacitor	220nF	235nH	8mΩ
Output Capacitor	2200uF	205nH	3.57mΩ

III. VALIDATION BASED ON SIMULATION AND EXPERIMENTATION

The models described in Section II are combined together to form a single system model which is used to predict Conducted EMI of the PFC flyback converter as shown in Fig.12 [11-13]. Accordingly, the simulation is carried out using the LTspice simulation software. The flyback converter considered here is working in CrCM mode with an input voltage of AC 280V, the output voltage and current of 15V,2A. A flyback transformer offers 800uH primary inductance and secondary inductance of 40uH.

The three important elements in Conducted EMI prediction are the noise sources, noise path and Conducted EMI measurement. The noise sources and its effect on the generation of Conducted EMI are discussed in the previous section. The Conducted EMI noise path for CM and DM is as represented in Fig. 13 and

Fig. 14. The EMI measurement from a PFC flyback converter is configured as shown in Fig.12. The utility mains are connected through a LISN to flyback PFC converter. These LISN provides defined impedance for Conducted EMI noise generated from the converter. The voltage measured across the two 50Ω resistors V_{lg} and V_{ng} as shown in Fig.12 gives the Conducted EMI. The dotted lines in Fig. 13 indicate CM noise coupling path and dotted lines in Fig. 14 indicates the DM noise coupling path. According to the conventional theory, DM and CM Conducted EMI is defined as follows.

$$V_{cm} = \frac{\left(V_{lg} + V_{ng}\right)}{2}$$

$$V_{dm} = \left(V_{lg} - V_{ng}\right)$$

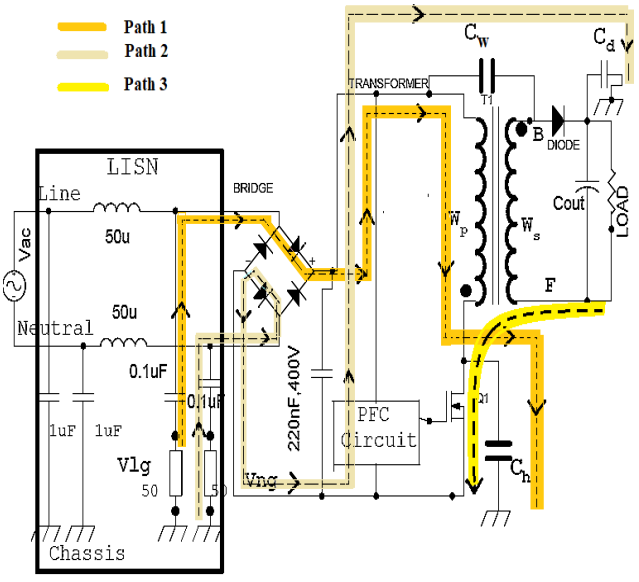

Fig. 13. CM Conducted EMI noise path

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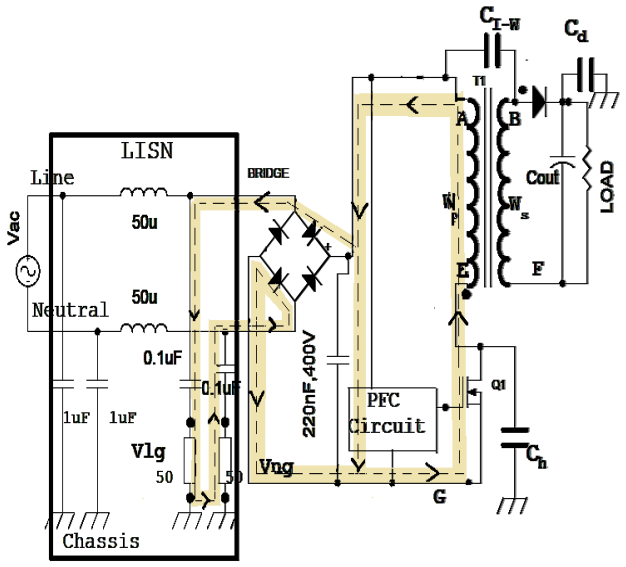

Fig. 14. DM Conducted EMI noise path

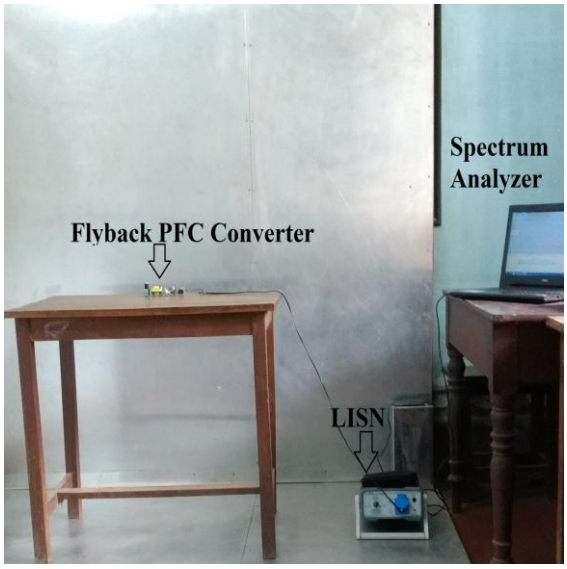

Fig. 15. Conducted EMI pre-compliance test setup

A. EMI filter design

The model and the predicted Conducted EMI spectra will be used to calculate the EMI filter values. The Conducted EMI limits specified by CISPR is the red line shown in Fig. 17 & 18 which is used for designing the CM filter and DM filter components. The EMI filter design method [11-12] is followed here. Firstly, the attenuation needed for the CM and DM noise to meet the standards is found out. Here, the DM amplitude measured from simulated Conducted EMI is 102dBuV and CM amplitude EMI is 94dBuV. The required filter attenuation considering Conducted EMI noise limit is;

$$A\left[dB\mu V\right] = A_n - L_{QP} + m$$

The filter corner frequency for the second-order filter f_{cdm}=13kHz and f_{ccm}=12.5kHz. Therefore, the C_y capacitor is assumed to be 10nF and the CM inductance is calculated to be

$$L_{cm} = \left(\frac{1}{2\pi f_{ccm}}\right)^2 \frac{1}{2C_y} = 8.1mH$$

$$C_x = \left(\frac{1}{2\pi f_{cdm}}\right)\frac{1}{L_{dm}} = 2.2\mu F$$

The leakage inductance of CM inductor is 65uH which acts as DM inductor. The calculated values are employed in the simulation. The results after incorporating the filter are as shown in Fig. 17 and Fig. 18 for CM and DM respectively. It can be inferred that the filter designed has brought down the DM and CM noise to compliant limits.

B. Experimental Results

The pre-compliance Conducted EMI test set up shown in Fig. 15 consists of a Spectrum Analyser with LISN. The PFC flyback converter has a input voltage AC voltage 240V, output voltage of DC 20.7V and a power factor of 0.92. This Flyback PFC converter was tested for Conducted EMI and results are presented in Fig. 17 and Fig.18.

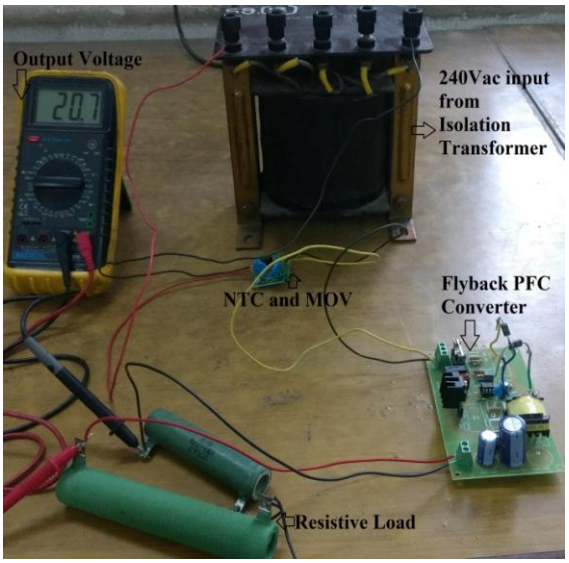

Fig. 16. Output volatage of Flyback PFC Converter

From the comparison illustrated in Fig.17 and Fig.18 the observation can be made that the simulation and experimental envelope match quite well in the frequency range of 150kHz to 30MHz. An accurate match with 5dB error above 4MHz to 10MHz is observed in CM Conducted EMI without EMI filter. At the frequency higher than 10MHz there is a mismatch with maximum error of 10dB is observed in CM Conducted EMI plot without EMI filter. In case of DM noise without filter an accurate match till 1MHz was observed and above 1MHz there was a 10dB mismatch. With EMI filter employed there is a mismatch of more than 10dB error from simulated to experimental reading of CM and DM noise. But both simulated and experimental readings are within the compliance limit.

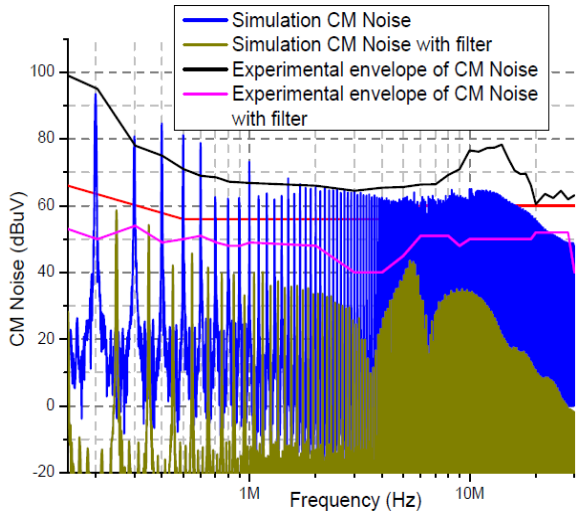

Fig. 17. CM Noise spectrum with and without line filter

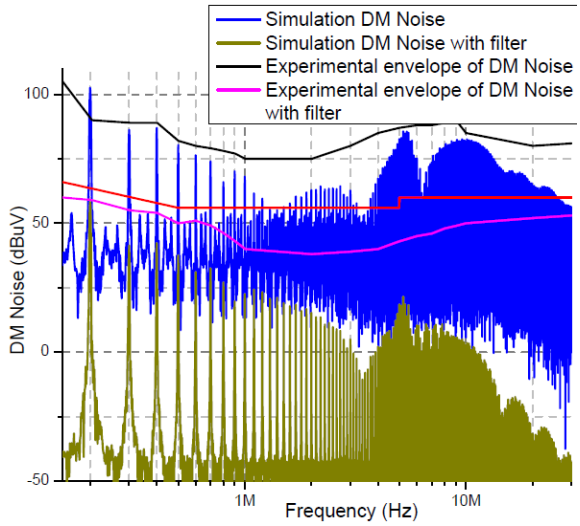

Fig. 18. DM Noise spectrum with and without line filter

IV. CONCLUSION

This paper presents a systematic method for estimating the Conducted EMI of a Flyback PFC converter. The noise sources in the converter and the paths of propagation of noise is identified and modelled. Separate equivalent model of transformer, capacitor, PCB trace and semiconductor switches are used. The complete model for Conducted EMI flyback PFC Converter is obtained from these equivalent models. Simulation and analysis is carried out using this model. The method for obtaining the values of parameters of this model are also presented. A 30W flyback PFC working in CrCM fed from the 230V utility supply is considered and the analysed. The simulation of this converter is carried out in SPICE software using the parameter value obtained from the formulae given. The simulation and the experimental result are in close agreement validating the model presented. This method can be used by the designers to estimate the Conducted EMI noise and to optimize the line filters to reduce the emission to Compliance level at the design stage itself.

REFERENCES

1. CISPR 22 © IEC 2003, Information Technology Equipments – Radio Disturbance Characteristics – Limits and Methods of Measurements.
2. C.R.Paul, *Introduction to Electromagnetic Compatibility*, New York: Wiley, 1992.
3. M. M. Jha, K. B. Naik and S. P. Das, "Types of electromagnetic interferences in SMPS and using Y-capacitor for mitigation of Mixed Mode noise," *2010 International Conference on Power, Control and Embedded Systems*, Allahabad, 2010, pp. 1-6.
4. P. Kong and F. C. Lee, "Transformer structure and its effects on common mode EMI noise in isolated power converters," *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, 2010, pp. 1424-1429.
5. B. Cogitore, J. P. Keradec, J. Barbaroux, "The two-winding transformer: an experimental method to obtain a wide frequency range equivalent circuit", IEEE Trans. Instruct. Meas., vol. 43, no. 2, pp. 364-371 (1994).
6. Q. Liu, F. Wang and D. Boroyevich, "Model conducted EMI emission of switching modules for converter system EMI characterization and prediction," *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, Seattle, WA, USA, 2004, pp. 1817-1823 vol.3.
7. Li Longtao, Wang Lixin, Lv Chao and Sun Chao, "A simulation of conducted EMI in flyback converters," *Proceedings of The 7th International Power Electronics and Motion Control Conference*, Harbin, 2012, pp. 1794-1798.
8. D. Sakulhirirak, V. Tarateeraseth, W. Khan-ngern and N. Yoothanom, "Design of High Performance and Low Cost Line Impedance Stabilization Network for University Power Electronics and EMC Laboratories," *2007 7th International Conference on Power Electronics and Drive Systems*, Bangkok, 2007, pp. 284-289.
9. H. Li *et al*., "Conducted EMI simulation of switched mode power supply," *2009 IEEE International Symposium on Electromagnetic Compatibility*, Austin, TX, 2009, pp. 155-160.
10. A. R. Rivera-Ramos and M. Jimenez, "Analytical models for estimating parasitic components in power electronics PCBs," *48th Midwest Symposium on Circuits and Systems, 2005.*, Covington, KY, 2005, pp. 1235-1238 Vol. 2.
11. M. Ashritha and M. L. Sudheer, "Low conducted EMI in NUPF converters," *2016 International Conference on ElectroMagnetic Interference & Compatibility (INCEMIC)*, Bangalore, 2016, pp. 1-4.
12. H. Li *et al*., "Conducted EMI simulation of switched mode power supply," *2009 IEEE International Symposium on Electromagnetic Compatibility*, Austin, TX, 2009, pp. 155-160.
13. S.Reeba Rex, D.M.Mary Sythia Regis Praba, "Analysis of EMI Reduction in Optimised Boost Converter Using Analogue PWM Chaotic Technique," *International Journal of Recent Technology and Engineering (IJRTE)*, Volume-7 Issue-5S2, Jan 2019.
14. Sandeep Tammana, Siva Yellampalli, "EMI Design for DC-DC Converters," *International Journal of Recent Technology and Engineering (IJRTE)*, Volume-7 Issue-ICETESM, March 2019.

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