International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-3, September 2019

Performance Evaluation of New Adder Designed for Electronic Circuits

R.Gowrishankar, N.Sathishkumar, B.Senthilkumar

Abstract*: *Arithmetic and Logic Unit (ALU) is the important module in any digital system utilized in the current world applications. Adder plays major role in the construction of any ALU. Multipliers can also be designed with the help of continuous addition. The efficient design of adders is very much needed for the efficient ALU design. Parallel prefix adder has been chosen in this research because of its fastest computation and efficiency. Kogge Stone, Sklansky, Ladner Fischer, Brunt Kung, Han-Carlson and Knowles are the adders discussed in this research. Further, the combinations of any two adders have also been tested for the best efficiency in terms of power consumption and delay utilisation. From the many combinations, it is found that the proposed combination of Bruntkung and SKlansky (BSK) adder performs excellent with the power consumption of 25011.22 nW and delay of 1243 pS.

Keywords* : *Adder, Delay, Multiplier, Power.

I. INTRODUCTION

Adders play major role in the construction of ALU and other important electronic designs. The bit by bit slow operation for addition increases the time consumption in serial adder even though its architecture is very simple to design [1]. This draw back forces the design of parallel prefix adders for parallel processing and completing the addition operation with less time consumption [2]. The efficient and well utilised parallel prefix adders in ALU are Kogge Stone, Sklansky, Ladner Fischer, Brunt Kung, Han-Carlson and Knowles adders. Less power consumption with less delay is the main task for any adder design [3]. All the mentioned adders are advantageous in either power consumption or in time consumption (delay). Further, a new logic for the addition can be possible by combining any two adder logic for the improvement in power consumption and delay efficiency. Hence the study and comparison of given adders have been presented in this research along with the possible new combination.

II. MATERIALS AND METHODS

The existing Kogge Stone, Sklansky, Ladner Fischer, Brunt Kung, Han-Carlson and Knowles adders and the proposed combinational adder (Brunt Kung with Sklansky) have been designed and tested with the help of Xilinx ISE and Cadence tool.

III. EXISTING PARALLEL PREFIX ADDERS

The main blocks in the parallel prefix adders are pre processing unit, carry network and the post processing unit. Here, the carry generation and propagation has been handled by pre processing unit [2]. The carry network may include the logic gates as per the required architecture for addition. The generated carry as per the given input can be propagated to next stage in a parallel processing. The carry network is having the combinations of black, grey and buffer cells. The grey and black cells are used for group generation and propagation as per the given input and the buffer used to prevent the overloading between the cells while performing the parallel operation of addition. Then the final stage is post processing for the complete result with sum and carries. All the parallel prefix adders have been taken for consideration in this article functions with the above given architecture. And the difference is the logic chosen for the addition operation. Kogge-Stone Adder is a carry look ahead adder and it functions with the basic units of parallel prefix adders [4]. Its architecture utilises more area with $\log2^n$ carry stages and number of cells defined by $n(\log2^n-1)+1$. Brunt Kung Adder architecture consists of alternative black cells and buffers along with the grey cells [5]. Other functionalities are almost same as that of Kogge-Stone adder. Because of alternative cell structure the size of the adder is reduced. If the number of stage increases the number of black cells decreases and reduces the wire too. It has $2\log2^n-1$ carry stages and $2(n-1)-\log2^n$ number of cells. Han Carlson Adder is the combination of Kogge-Stone and Brunt Kung Adder. It also has the same number of stages with modification in the architecture [6]. Number of cells can be measured by log(N+1). Ladner Fischer Adder is a tree structured carry look ahead adder and utilises more area than the previous adders [7] – [9]. The stages and cell count can be measured by using log(n). Sklansky Adder is a N stage adder and uses less number of buffers. Hence the size of the adder is reduced compared to the other adders [8].

Manuscript published on 30 September 2019
* Correspondence Author
R.Gowrishankar*, Department of Electronics and Communication Engineering, KIT-Kalaignarkarunanidhi Institute of Technology, Coimbatore, India. Email:gowrikit2008@gmail.com
Dr.N.Sathishkumar, Department of Electronics and Communication Engineering,, Sri Ramakrishna Engineering Collegey, Coimbatore, India. Email:nsk20022002@gmail.com
Dr.B.Senthilkumar, Department of Electronics and Communication Engineering, KIT-Kalaignarkarunanidhi Institute of Technology, Coimbatore, India. Email:senthilkit2016@gmail.com

Knowles Adder is the combination of Kogge Stone and Sklansky adders. Both the adders has large number of black cells than the grey cells [10]. And the cell count is defined by log(n). Performances of all the six adders have been compared and tabulated in Table 1 as follows. From the Table 1, it is clearly evident that the Brunt Kung adder is good in terms of power consumption with a value **25761.713 nW** and area utilization with a value **184**. The Kogge Stone adder is good in delay with a value **1481pS**. The Sklansky adder is good in cell count with a value of **76** and delay value of **1295pS**. Power and delay are the important parameters to be considered for an efficient adder design. Hence, Brunt Kung and Sklansky adders have been taken in to consideration for the new efficient adder proposal. The two adders have been combined based on the requirements and designed new efficient adder named **B**RUNTKUNG and **SK**LANSKY (BSK) adder. The description about BSK adder is presented in the following section.

IV. PROPOSED BSK (BRUNTKUNG AND SKLANSKY) ADDER

Considering the advantages of all the adders discussed in the above section, a new adder has been proposed by combining the existing two adders. The name of that adder is BRUNT KUNG and SKLANSKY (BSK) adder. The detailed description of BSK adder is as follows. The proposed BSK adder also includes 3 Levels such as pre-processing unit, Carry-Network and Post–processing unit. In this new adder the design is carried out by making use of Sklansky adder and Brunt Kung adder. In Sklansky adder, the first stage of Carry Network resembles the Brent Kung Adder, which has been replaced by Sklansky adder with same logic of Brunt Kung adder and named as BSK adder. The ranges of black cells are reduced in each step and the numbers of grey cell are being increased, which ends up in reduced area and connection inside the carry network. The output of the Carry network is fed into XOR gate which constitutes the Post-processing unit to produce the sum and Carry. The BSK adder is shown in Fig.1. The modified carry network has the cell count with a value of 84, power consumption with a value of 25011.224nW and the delay achieved with a value 1243pS.

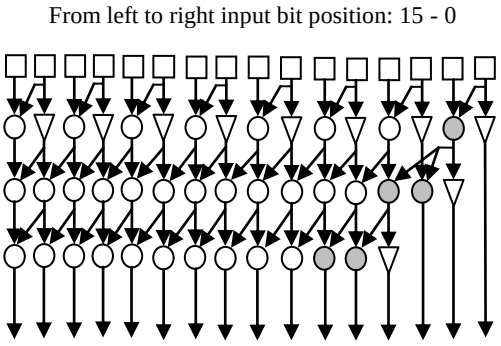

Fig.1. Proposed BSK Adder

V. RESULTS AND DISCUSSION

The following are the results produced by the adders while adding two 16 bit digital numbers (Data 1: AAAA and Data 2: 1425 the resulted Sum : BECF and Carry : 0). The Fig. 2 is the result produced by the Sklansky Adder, Fig. 3 is the result produced by the Brent Kung Adder, Fig. 4 is the result produced by the Han Carlson Adder, Fig. 5 is the result produced by the Knowles Adder and Fig. 6 is the result produced by the BSK Adder. From the above results, it is clearly known that, all the existing and proposed adders have produced the same results while performing addition. But, the speed of delivering the output, power consumption for the processes and the area utilization for the particular design are the main parameters to be considered for evaluating any adder towards the design and implementation of an efficient adder. While analyzing the above said factors, the BSK adder performs well and produced excellent results. The results are tabulated and plotted.

From Table 2 and Fig 7 (a), (b), (c) and (d) it is clearly observed that the Han Carlson has the power consumption with a value of 25791.430 pS which is 0.11% lesser than that of Brunt Kung adder and the total area utilization achieved with a value 207 which is 11.11 % higher than that of Brunt Kung adder. The modified carry network in BSK adder leads to reduction in cell count with a value of 84 which is same as that of Brunt Kung adder, power consumption with a value of 25011.224nW which is 2.91% lesser than that of Brunt Kung adder and 3.02 % lesser than that of Han Carlson adder, the delay achieved with a value 1243pS which is 4.01 % lesser than that of Sklansky adder and 25.26% lesser than that of Knowles adder and the total area utilization is reduced with a value of 179 which is 2.72 % lesser than that of Brunt Kung adder and 6.28 % lesser than that of Knowels adder. Hence, the proposed BSK adder performs excellent in all aspects.

VI. CONCLUTIONS AND FUTURE SCOPE

The new adder along with the existing adders have been designed and discussed for power and delay efficiency. The cell count is valued as 84 which is 9.52% higher than the Sklansky adder. The power consumption obtained with a value of 25011.224nW which is 2.91% lesser than that of Brunt Kung adder and 3.02 % lesser than that of Han Carlson adder, the delay achieved with a value 1243pS which is 4.01 % lesser than that of Sklansky adder and 25.26% lesser than that of Knowles adder and the total area utilization is reduced with a value of 179 which is 2.72 % lesser than that of Brunt Kung adder and 6.28 % lesser than that of Knowels adder. The proposed BSK adder performs well in all aspects except the cell count. It is planned to reduce the cell count in future. The proposed and existing adders have been designed for 16 bit processing. Further, it is planned to design all the adders for 32 bit and N bit processing and to utilise those for multiplier like applications in future.

Table – I: Comparison of Existing Adders

Description	Name of the Adder					
	Kogge Stone	Brunt Kung	Sklansky	Ladner Fischer	Han Carlson	Knowles
Cell Count	130	84	**76**	86	96	130
Power in nW	29020.902	**25761.713**	28169.501	25998.346	25791.430	26008.400
Delay in Ps	1481	2196	**1295**	1934	1707	1663
Area	271	**184**	197	188	207	191

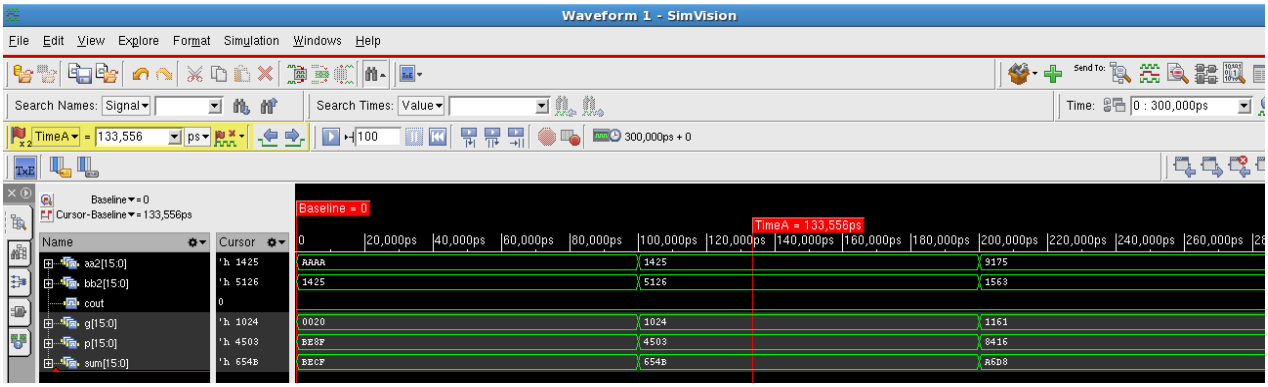

Fig.2. Simulated Result of Sklansky Adder

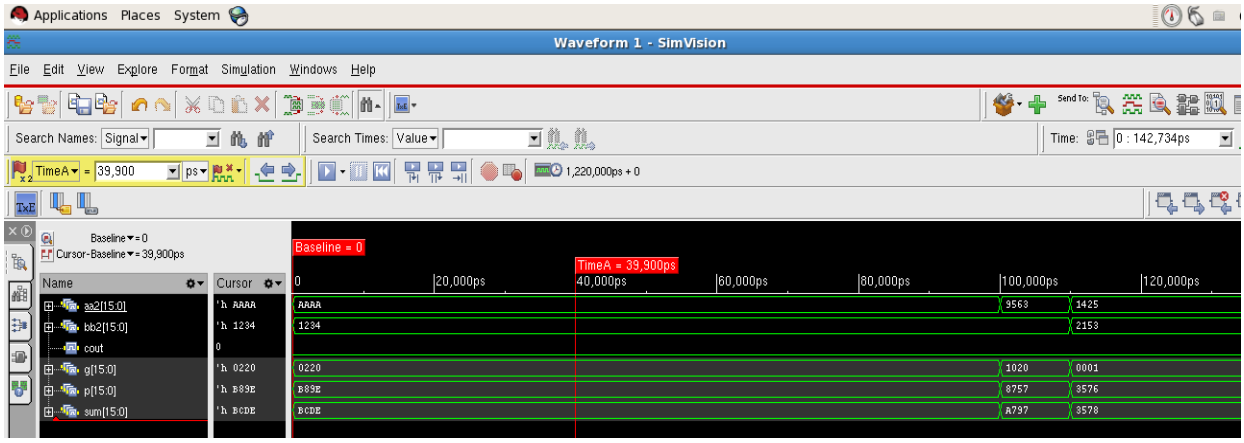

Fig.3. Simulated Result of Brent Kung Adder

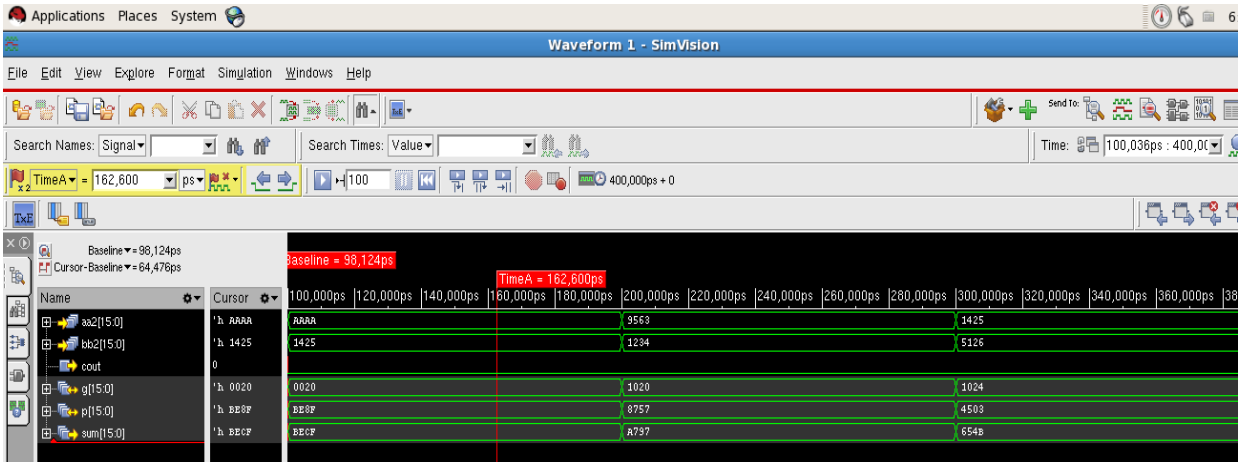

Fig.4. Simulated Result of Han Carlson Adder

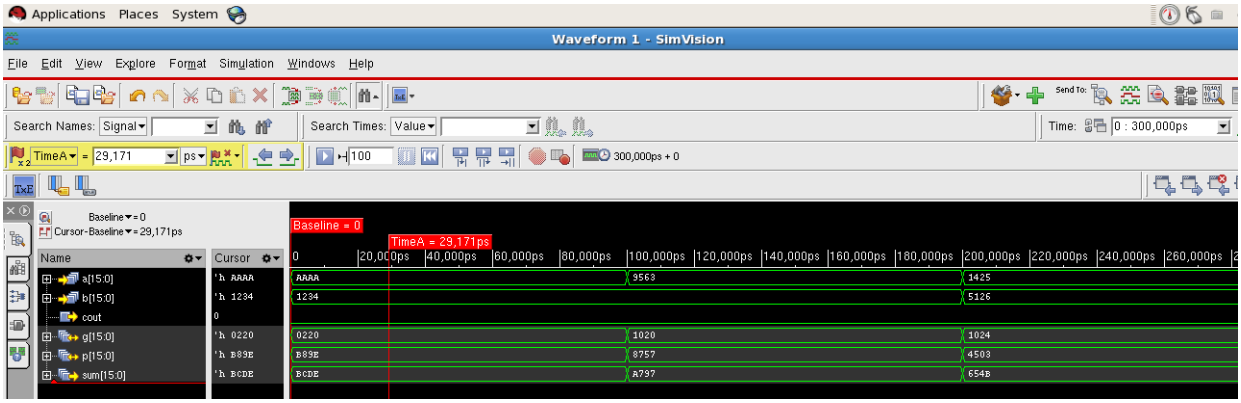

Fig.5. Simulated Result of Knowles Adder

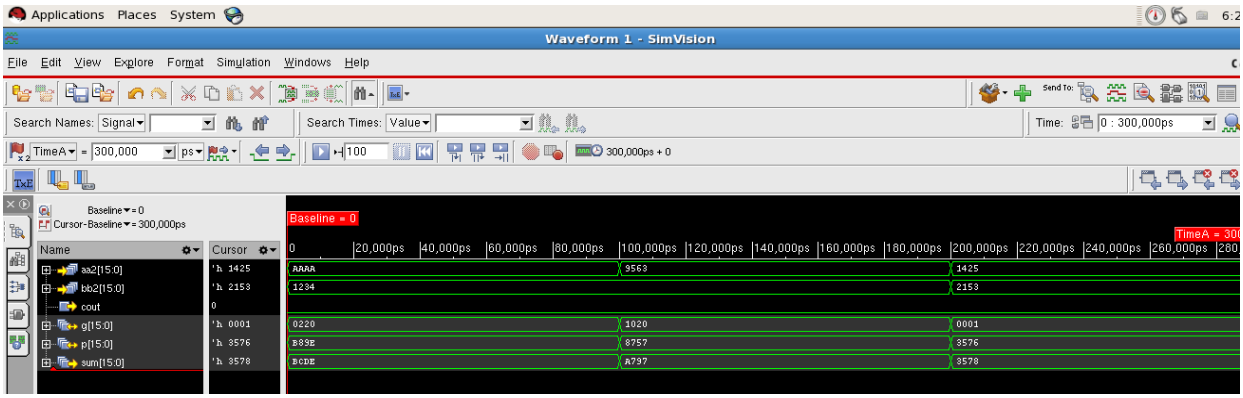

Fig.6. Simulated Result of BSK Adder

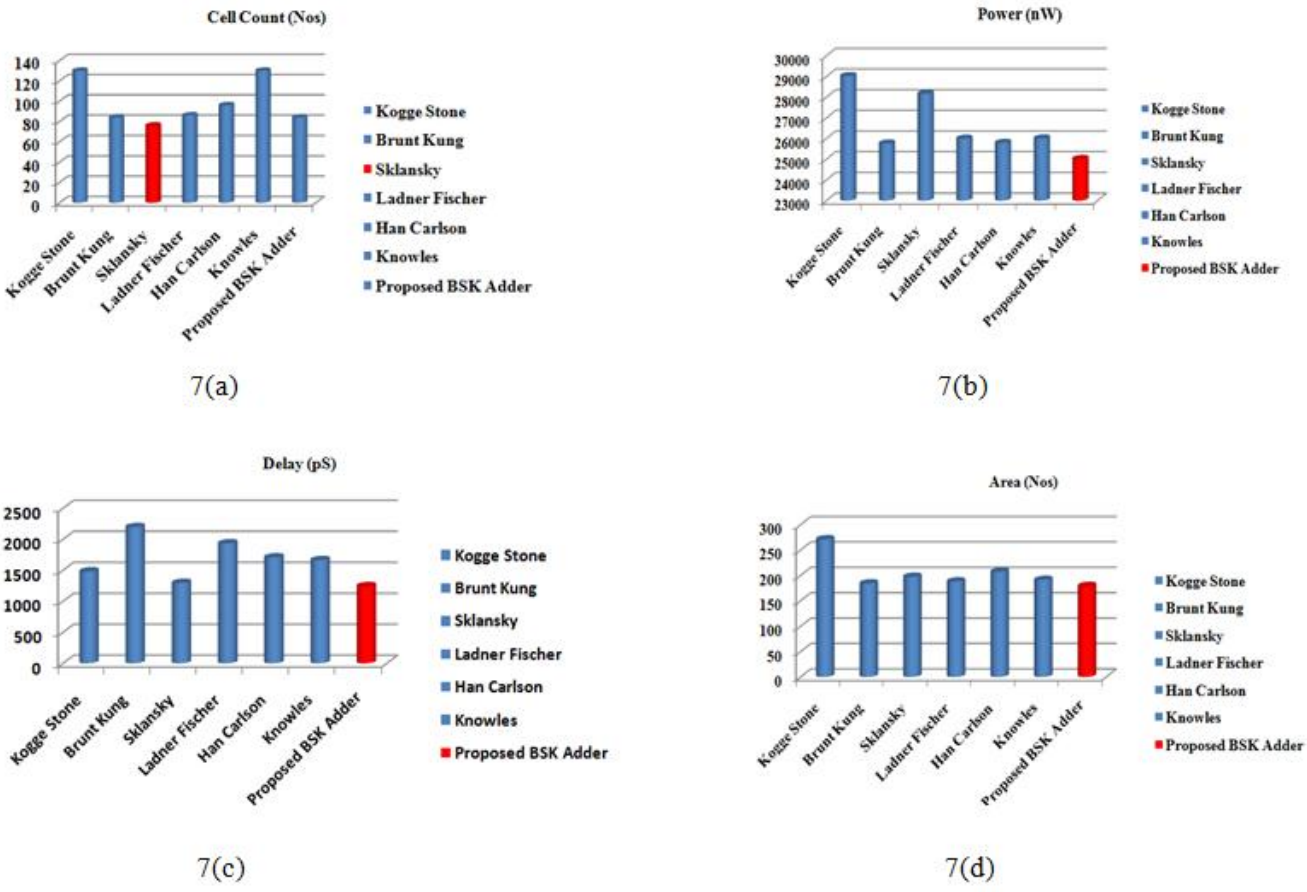

Fig.7. Performance of Adders

Table- II: Name of the Table that justify the values

Name of the Adder	Description			
	Cell Count (Nos)	Power (nW)	Delay (pS)	Area (Nos)
Kogge Stone	130	29020.902	**1481**	271
Brunt Kung	84	**25761.713**	2196	**184**
Sklansky	**76**	28169.501	1295	197
Ladner Fischer	86	25998.346	1934	188
Han Carlson	96	25791.430	1707	207
Knowles	130	26008.400	1663	191
Proposed BSK Adder	**84**	**25011.224**	**1243**	**179**

REFERENCES

1. Ashivani Dubey and Jagdish Nagar, "Comparison between Serial Adder and Parallel Adder", International Journal of Engineering Sciences & Research Technology, 2013, 2, (9), pp 2570-2572.
2. P.Kowsalya, M.Malathi and Dr.P.Ramanathan, "Low Power Parallel Prefix Adder", Applied Mechanics and Materials, 2014, 573, pp 194-200.
3. Keivan Navi, Mehrdad Maeen, Vahid Foroutan, Somayeh Timarchi and Omid Kavehei, "A Novel Low-Power Full-Adder Cell For Low Voltage", Integration, the VLSI Journal, 2009, 42, (4), pp 457-467.
4. Peter M Kogge and Harold S Stone, "A Parallel Algorithm for the Efficient Solution of s General Class of Recurrence Equations", IEEE Transactions on Computers, 1973, C22, (8), pp 786-793.
5. Richard P Brent and H T Kung, "A regular layout for parallel adders", IEEE Transactions on Computers, 1982, C31, (3), pp 260-264.
6. Subha Jayamala K. and Aswathy B S, "Performance Enhancement of Han Carlson Adder", International Journal of Advanced Research in Electronics and Communication Engineering, 2016, 5, (2), pp 226-230.
7. Pakkiraiah Chakali and Madhu Kumar Patnala, "Design of High Speed Ladner Fischer Based Carry Select Adder", International Journal of Soft Computing and Engineering, 2013, 3, (1), pp 173-176.
8. Sklansky J, "Conditional-Sum Aditional Logic", IEEE Transactions on Electronic Computers, 1960, EC9, (2), pp 226-231.
9. Richard E Ladner and Michael J Fischer, "Parallel Prefix Computation", Journal of the ACM, 1980, 27, (4), pp 831-838.
10. Pawan Kumar and Jasbir Kaur, "Design of Modified Parallel Prefix Knowles Adder" , International Journal of Science and Research, 2014, 3, (7), pp 199-201.

AUTHORS PROFILE

R.Gowrishankar received the B.E and M.TECH degrees in Electronics and Communication Engineering from Bharathiar University and SASTRA University in 2001 and 2004, respectively. During 2004-2008, he has been employed in Tamilnadu College of Engineering as Assistant Professor. Now he is working in KIT-Kalaingarkarunanidhi Institute of Technology as a Professor. He has filed 04 patents in IPR India and published 10 papers in refereed journals. He is also a life member in ISTE and IAENG. His research Interest includes VLSI Design, Networking and Communication Engineering.

Dr.N.Sathish Kumar is a Professor in Electronics and Communication engineering Department is an accommodating and versatile individual with over 15 years of teaching in both UG and PG courses and 09 years of research experience with a solid commitment to the social and academic growth and development. He received his Ph.D degree from ANNA University, Chennai in the Field of MIMO Receivers-Wireless Communication, in year 2012. He completed his Master degree (Applied Electronics) programme from Government College of Technology, Coimbatore. He has published 08 papers in National conference and 3 in the international conference and 18 papers in reputed national and international journals. He has wonThree ' Best Paper' awards for his research. He is a life member in various professional societies like IEEE (USA), IETE, ISTE,SSI.

Dr.B.Senthilkumar received the B.E and M.E degrees in Electronics and Communication Engineering from Bharathiar University and Anna University Chennai in 2001 and 2006, respectively. During 2001-2015, he has been employed in Tamilnadu College of Engineering as Professor. Now he is working in KIT-Kalaingarkarunanidhi Institute of Technology as a Professor with more than 18 years of teaching and more than 10 years of research experience. He has filed 06 patents in IPR India and published 14 papers in refereed journals. He is also a life member in ISTE and IAENG. His research Interest includes Circuit Optimization and Communication Engineering.