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FDTD Modeling with Passive Shielding for Crosstalk Reduction in Coupled RLC Interconnects

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Abstract— This paper presents passive shielding technique for crosstalk noise and delay reduction in resistive driven RLC interconnect. FDTD technique is used for modeling proposed geometry. The worst case delay and noise induced due to crosstalk in passive shielded interconnects are compared with unshielded lines and is validated using HSPICE simulations for 32nm global interconnects. From the results it has been demonstrated that the proposed model results and HSPICE simulations differ by 8% and by using proposed geometry crosstalk noise and delay has come down by 90% and 52% when compared to unshielded line.

Index Terms—Crosstalk noise, Delay, Passive shielding RLC interconnects, FDTD

I. INTRODUCTION

Crosstalk which is the coupling of energy from one line to another will occur whenever the electromagnetic fields from different structures interact, is of considerable importance in high-speed digital circuits. In multi-conductor systems, crosstalk can cause two undesirable effects. First effect is the performance of transmission lines in a bus change due to crosstalk by changing the effective impedance delay, inter-wire capacitance, mutual inductance.

Second effect of crosstalk is it will induce noise on the interconnect lines in the form of glitches, resulting in degradation of signal integrity and reduction of noise margin. Earlier mutual inductance was less significant but due to emerging high speed VLSI designs and decrease in spacing between the interconnects mutual inductance has also become a predominant factor .Current from Aggressor to victim line is induced due to mutual inductance which leads to crosstalk between interconnect lines. Hence accurate modeling of RLC interconnects has become important for proper timing and signal integrity analysis in VLSI designs .If not considered in early stages of design , Crosstalk effect in interconnect leads to design failures

Many techniques for Crosstalk noise and delay reduction on lossy transmission lines has been modeled [6-10]. Continuous sizing of wire, increasing space between interconnects, insertion of buffers, Encoding data on interconnect lines, Inducing shield lines between interconnect lines etc.

Algorithms for transient response on lossy transmission lines was proposed by Roychowdhury et al. [8]. Wang and Dai has adopted S parameter macro delay model for minimization of delays.In this paper we have proposed Shielding techniques for reducing crosstalk effects. Shielding involves placing of extra lines as shields between interconnects There are two possible ways of shielding 1) Passive Shielding and 2) Active Shielding [11][12]. In active Shielding shield lines switch in the same direction as that of signal lines .Due to Active Shielding reduction in delay can be observed but at the cost of increase in power consumption due in increased switching activity and area overhead. As a result we have come up with Passive shielding techniques for reducing crosstalk effects in energy efficient chips. These coupled RLC interconnect lines, Shielded with passive shielding are modeled by FDTD technique and validated using HSPICE. The error found in transient response of interconnects using FDTD and HSPICE is very less about 8%.

The paper is organized as follows: section II describes proposed Passive shielding geometry for coupled interconnect lines. FDTD model for coupled interconnect lines is described in Section III. In section IV the proposed exemplar is validated by HSPICE and proposed model is concluded in section V

II. PASSIVE SHIELDING PROPOSED MODEL FOR COUPLED INTERCONNECT LINES

Shielding is mainly used in interconnects to reduce crosstalk between coupled interconnect lines. A Distributed RLC interconnect model driven by resistive drivers is shown in Fig.1 and with Passive shielding inserted between aggressor and victim lines is shown in Fig. 2. A grounded Shield line is inserted between the Aggressor and Victim line. Rs is source resistance, R,L,C represent line parameters, C_L represents load capacitance.L_{12},L_{23},C_{12},C_{23} are mutual inductance and capacitance values between Victim and Shielded lines. The center line in proposed geometry is used for transmission of signal and the peripheral lines above and below the middle line which are grounded act as shields.

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For proper Synchronization between the interconnects parasitic on all the lines are maintained same.

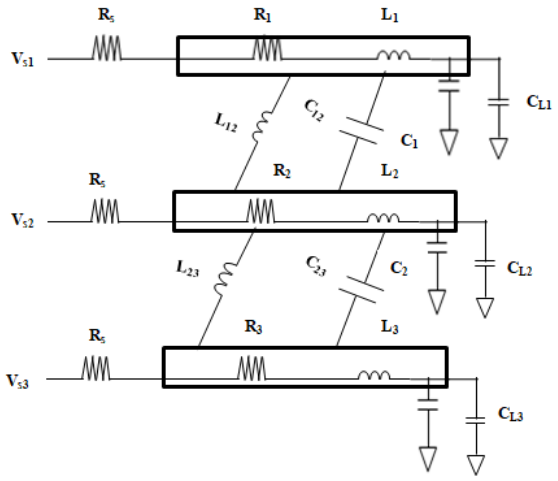

Fig.1.Coupled three line RLC Interconnects with resistive driver

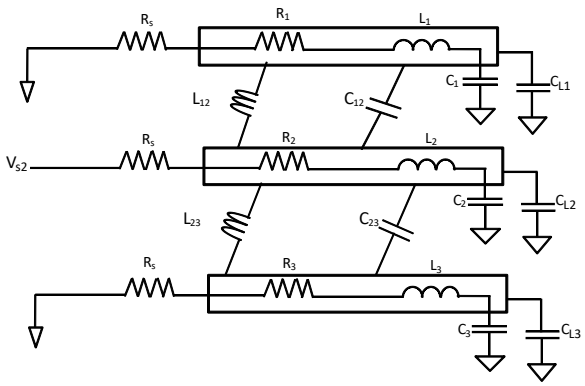

Fig.2.Coupled RLC Interconnects with Passive shielding

III. FDTD MODEL PROPOSED

One of the facts with Distributed RLC interconnects is that the Partial differential equations are used for describing transmission lines and are solved in frequency domain. But nonlinear elements are solely described in time domain .Hence frequency to time domain conversion problem arises, which can be overcome by using FDTD technique[5]. Interconnect lines with passive lines can be expressed using Telegraphers equations as

$$\frac{d}{dx}V(x,t) + RI(x,t) + L\frac{d}{t}I(x,t) = 0 \qquad (1)$$

$$\frac{d}{dx}I(x,t) + \frac{d}{dt}CV(x,t) + GV(x,t) = 0 \qquad (2)$$

Where V,I represent line voltages and current in 3 x1 column vectors and the parasitic elements are also represented in 3 x3 matrix for p.u.l as

$$V = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \quad I = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}, \quad R = \begin{bmatrix} R_1 & 0 & 0 \\ 0 & R_2 & 0 \\ 0 & 0 & R_3 \end{bmatrix},$$

$$L = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix},$$

$$C = \begin{bmatrix} C_{11} + C_{12} & -C_{12} & C_{13} \\ -C_{21} & C_{22+}C_{12} + C_{23} & -C_{23} \\ C_{31} & -C_{32} & C_{33+} \end{bmatrix}$$

Central differential approximations are used for analyzing the Telegrapher equations. For better accuracy With FDTD modeling the voltages and currents nodes are positioned however are separated by Δx/2 instances in Space and by using Δt/2 instances on time axis as shown in Fig.3.

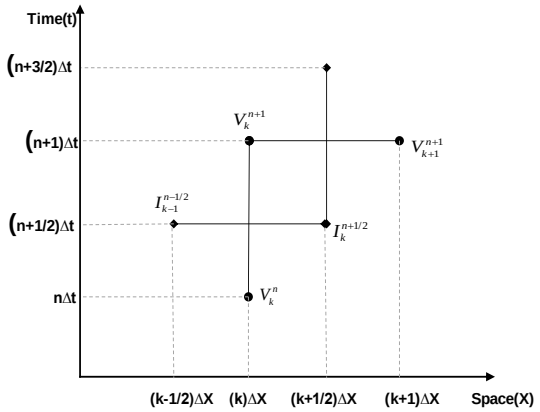

Fig.3.Discritized relation between voltage and current nodes in space and time domain

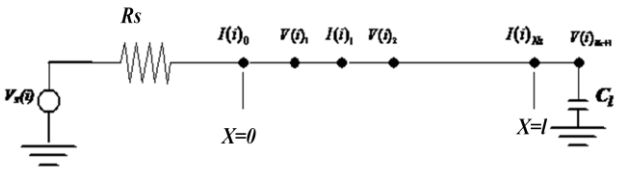

Fig.4. Discretization of line for FDTD analysis in space

The Fig.4 represents the interconnect line of size L driven by resistive driver at X=0 and terminated through capacitive load at X=l. Differential equations (1) and(2) are discretized with respect to time and space to put in force FDTD analysis. Size of transmission line is divided into Nl sections, each of Δx size and complete time into Nt segments, each of Δt size. Relation between currents and voltages with appreciate to space and time is as shown in Fig.3

On applying finite difference approximations to (1) and (2) we get

$$\frac{V_{k+1}^{n+1} - V_k^{n+1}}{\Delta X} + L\frac{I_k^{n+3/2} - I_k^{n+1/2}}{\Delta t} + R\frac{I_k^{n+3/2} + I_k^{n+3/2}}{2} = 0 \qquad (3)$$

for K =1, 2, 3, ……., Nl

$$\frac{I_k^{n+1/2} - I_{k-1}^{n+1/2}}{\Delta X} + C\frac{V_k^{n+1} - V_k^n}{\Delta t} + G\frac{V_k^{n+1} + V_k^n}{2} = 0 \qquad (4)$$

for K= 2, 3, 4, …….., Nl, where voltage and current are represented as

$$V_i^j = V[(i-1)\Delta x, j\Delta t],\ I_i^j = I\left[\left(i-\frac{1}{2}\right)\Delta x, j\Delta t\right] \quad (5)$$

By re-organizing the equation (3) and (4) the recursive relation between voltage and current at interior nodes on interconnect can be given as

$$V_k^{n+1} = ABV_k^n + \frac{A}{\Delta X}\left[I_{k-1}^{n+1/2} - I_k^{n+1/2}\right] \quad (6)$$

(6)

for K =1, 2, 3, ……., Nz and

$$I_k^{n+3/2} = EFI_k^{n+1/2} + \frac{E}{\Delta X}[V_k^{n+1} - V_{k+1}^{n+1}] \quad (7)$$

for K= 2, 3, 4, ……., Nz, where

$$A = inv\left[\frac{C}{\Delta t} + \frac{G}{2}\right],\ B = \left[\frac{C}{\Delta t} - \frac{G}{2}\right],$$

$$E = inv\left[\frac{L}{\Delta t} + \frac{R}{2}\right],\ F = \left[\frac{L}{\Delta t} + \frac{R}{2}\right]$$

The Voltage and current at the source end connected to resistive driver in Fig.4 can be given as

$$V_1 = V_s - I_s R_{eq} \quad (8)$$

$$I_s = \frac{V_s - V_1}{R_{eq}} \quad (9)$$

For applying FDTD analysis equation (6) is discritized in time domain as

$$V_1^{n+1} = V_s^{n+1} - I_s^{n+1} R_{eq} \quad (10)$$

Recursion relations at source interface for V1 can be given as

$$V_1^{n+1} = k_1k_2V_1^n + k_1k_3(V_s^n + V_s^{n+1}) - 2k_1k_3R_{eq}I_1^{n+1/2} \quad (11)$$

Where

$$k_1 = inv[U + k_3],\ k_2 = [AB - k_3],\ k_3 = \frac{A}{\Delta X R_s}$$

At the Far-end on the interconnect line the load current I_l and load voltage V_{NX+1} terminated with capacitive load can be given as

$$I_l^{n+1} = C_l \frac{V_{NX+1}^{n+1} - V_{NX+1}^n}{\Delta t} \quad (12)$$

$$V_{NX+1}^{n+1} = k_1k_2V_{NX}^n + \frac{2A}{\Delta X}\left[I_{NX}^{n+1/2}\right] \quad (13)$$

The relation between load current I_l related to load voltage V_{NX+1} is given as

$$I_l = C_l \frac{d}{dt} V_{NX+1} \quad (14)$$

Where $k_1 = inv\left[1 + \frac{2AC_l}{\Delta X \Delta t}\right],\ k_2 = \left[AB - \frac{2AC_l}{\Delta X \Delta t}\right]$

Assessment begins with evaluating voltage along the line starting from X=0 at precise time steps in phrases of voltage and current values at earlier nodes. Current at present node is evaluated from voltage and current values from earlier time step. Using FDTD method accurate results can be obtained only when courant condition is satisfied i.e $\Delta t \leq \frac{\Delta x}{V}$ Where V is velocity on signal on interconnect line and good resolution is obtained if spacial increments are very small[4]

IV. PROPOSED MODEL VALIDATION

HSPICE simulations, carried out in W element simulation tool are used for estimating the results of the proposed model. Parasitic used for modeling the interconnects lines with passive Shielding in HSPICE are maintained same as that of in proposed model. Delay and crosstalk noise are estimated on the victim line which is the middle line in the proposed geometry with resistor as the driver and capacitor as load as shown in Fig.4

Crosstalk effects are also compared on middle line of proposed passive shielded coupled interconnect with unshielded coupled interconnects based at the far end terminal of line2, using various other methods for crosstalk reduction such as increasing the length of interconnect and increasing the space between interconnects

V. RESULTS

As can be seen from the responses shown below crosstalk noise has reduced by 90% and delay reduction is 52% when compared which unshielded lines. The improvement using shielding is considerably good when compared to other reduction techniques like increasing width and length of interconnects

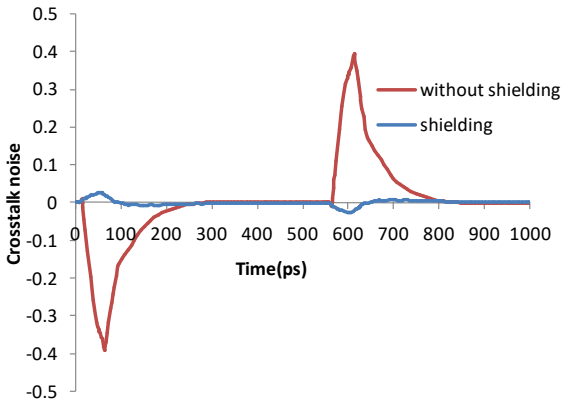

Fig.5. Crosstalk noise on interconnects

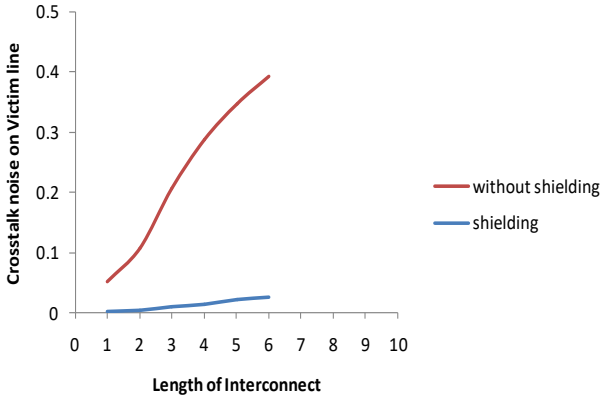

Fig. 6.Delay on interconnects

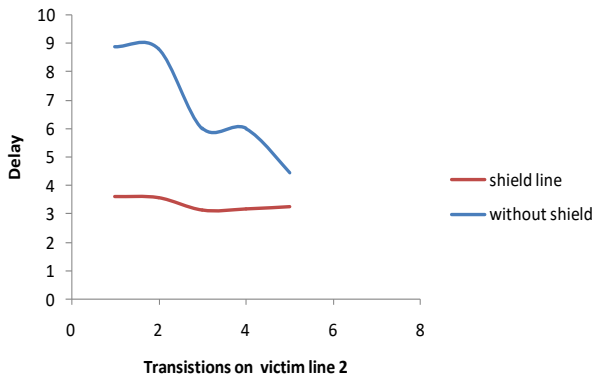

Fig. 7.Crosstalk noise peak for global interconnects

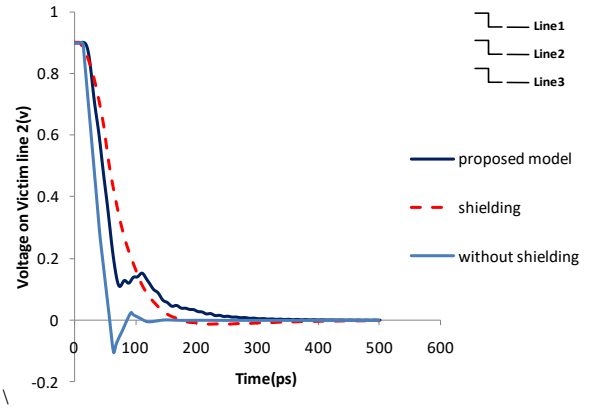

Fig:8(a)

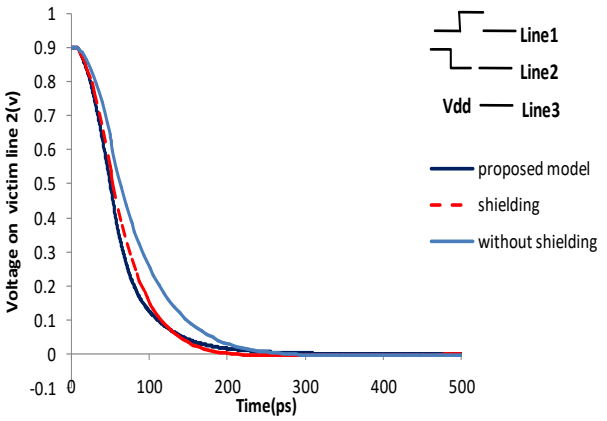

Fig:8(b)

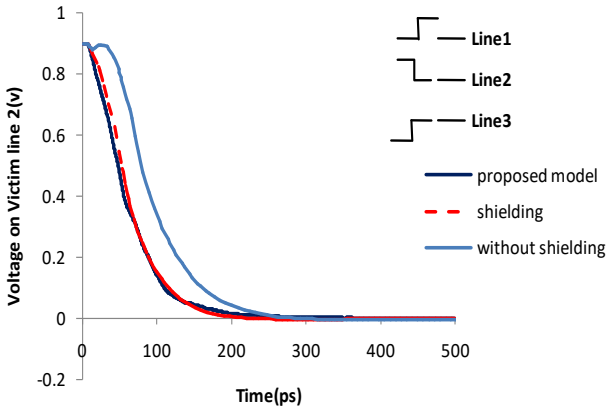

Fig:8(c)

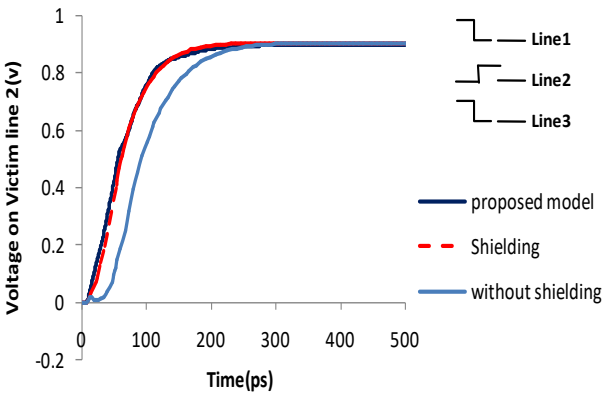

Fig: 8 (d)

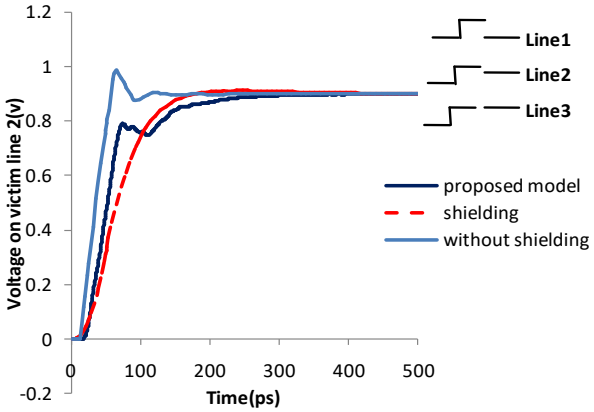

Fig:8(e)

Fig. 8. Transient responses on victim line 2 (a) Case-1 (b) Case-2 (c) Case-3 (d) Case-4 (e) Case-5 input switching

TABLE I: PROPAGATION DELAY ON VICTIM LINE 2 FOR DIFFERENT SWITCHING CASES

Input Switching modes				Propagation Delay on victim line 2			
Case mode	line1	line2	line3	Delay on line 2 with shielding		Delay on line 2 without shielding	%error between proposed model and HSPICE
				HSPICE(ps)	Proposed model(ps)		
Case-1	1-0	1-0	1-0	3.62	3.45	8.88	4.6

Case-2	0-1	1-0	Vdd	3.26	3.18	4.44	2.4
case-3	0-1	1-0	0-1	3.13	2.95	6.05	5.7
case-4	1-0	0-1	1-0	3.17	2.93	6.01	7.5
case-5	0-1	0-1	0-1	3.58	3.42	6.00	4.4

Table II: In-Phase and Out-Phase Delay on Line 2

Delay on line 2 (ps)	With Shielding	Without Shielding
In-phase Delay	3.62	8.88
Out-phase Delay	3.17	6.05

Functional crosstalk noise between shielded and unshielded lines is shown in Fig.5.functional crosstalk is measured by keeping the victim line quiet and switching aggressor lines

Functional crosstalk has been improved by 90% using shielding when compared with unshielded lines. For different switching cases the delay on victim line for shielded and unshielded lines in as shown in Fig.6. Crosstalk noise is measured by varying the interconnect length in Fig.7 and the effect increase in length is minimum on shielded lines. Transient responses for different switching cases on victim line from both shielded and unshielded lines is analyzed in Fig.8(a)-8(e).The variation in the responses considered in Fig.8 obtained using HSPICE and proposed model is very less around 8% as shown in Table 1

In-phase and out-phase delays have been provided in Table II for shielded and unshielded lines and a drastic decrease in delays as been observed using passive shielding when compared to unshielded line

VI. CONCLUSION

A Constructive geometry using passive shielding in coupled RLC interconnects for crosstalk induced delay and noise reduction as been suggested in this paper .Passive shielded lines have been modeled using FDTD technique. Considerable improvement in performance of shielded lines has been observed when compared with unshielded lines. The results obtained using proposed model are compared with HSPICE simulation and observed a very little difference of 8%

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