International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-3, September 2019

Effective Analysis of an Iterative Median Filter-Hardware and Software Perspective

Archana H R, C R Byra Reddy, Narendra C P

Abstract* : *Image quality enhancement is a very predominant domain of discussion as the complexity of system increases, the software implementation becomes a key factor but it is not always reliable to use the approach for adaptable applications such as medical, military or real time purpose. In order to address such scenarios it is necessary to have a reconfigurable and an adaptable implementation. In this paper we have addressed the hardware modeling of a median filter using double iteration process. The iterative median filter is implemented on an Artix-7 FPGA.

Keywords: Median Filter, FPGA, Sorter, error detection, PSNR, Noise

I. INTRODUCTION

Most commonly images are impacted by impulsive noise during its transmission after the capture. There are multiple strategies which can be incorporated in order to implement the different filtering techniques. The type of filtering can be decided based on the severity of the application. Many industrial automation applications require real time results where the predetermined features of the image are analyzed to identify the defects and process variations during manufacturing [1].

Median filtering involves a sliding window spatial filter. It functions more effectively than the other types of convolution filters since it not only eliminates the impulse noise but also helps to retain the edges used in order to provide a better quality of image. Authors discuss about the adaptive window size using modified PCNN model. The steps implemented are used to calculate the pollution level for a standard image [2].Salt and pepper noise exists in most of the image transmissions. Sukhwinder Singh et. al [3] discuss a Rank Ordered Absolute Difference statistic which detects the impulse noise in corrupted image. ROAD statistics is used to calculate a specific value of selected window.es that window is noisy and applies MAMF on the selected window.

Manuscript published on 30 September 2019
***** Correspondence Author
Archana H R *, Department of ECE, BMSCE , Bangalore. Email: archhr@gmail.com
Dr C R Byra Reddy, Department of ECE , BIT, Bangalore. Email: byrareddycr@yahoo.co.in
Dr Narendra C P , department, Name of the affiliated College or University/Industry, City, Country. Email: narendracp@rediffmail.com

II. EXISTING WORKS

Rashmi et.al [4] discusses the concept of switching median filters (SMF) which is a type of nonlinear image filter. It comprises of four blocks mentioned below:

- Forward moving window block.
- Median calculation block
- Arithmetic operation block
- Output section block

Here sorting architecture is designed for horizontal data first, vertical data next and finally diagonal sorting is done in ascending order. The second element represents the new median value. Ismaeil et.al [5] has implemented an adaptive decision based median filter. They discuss the utilization of hardware for implementation of their design namely the slice registers, LUTs, flip flops, BUFG. The iterative approach in our design clearly shows a reduction in the hardware utilization.

Hanumantharaju et.al [6] indicate the various derivatives of median filters such as weighted median filter, switched median (SM), Iterative median and center weighted median. Median filtering offers low computational complexity and preserves edges predominantly. Sometimes fine details of the image are removed. The window size adjusts depending on the noise density in an AMF. Greater the noise density, greater will be the window size to clean up the noise. AROF proposed eliminates the drawback of AMF. This method replaces the center noisy pixel with any other non-median pixel which is not noisy. Hardware architecture employs pipelining to reduce the computation time and parallel processing helps to accelerate the tasks. The noise detection unit checks if the pixel value is 0 or 255 and gives the output as zero. Sorting network employs a bitonic sorter and further concatenates the pixels using Batchers Odd-even merge sorting and the median value is computed. Parinita et.al [7] have adopted a comparator based approach which requires 19 comparators and 30 multiplexers for a window size of 3x3. Dr. K. Bikshalu et.al [8] have proposed an AMF which works at two levels. First level to fix the window size using comparators and an algorithm indicating the median value. Priyanka has proposed a new algorithm to remove the noise in the retina image. The methodology proves a better approach by preserving the predominant edges using 3 x 3 sliding window for extended median filtering. The triple input sorter module takes the input from a comparator. The comparator is in turn designed using D flip flops which comprises of single stage calculation of median value.

III. DESIGN OF ITERATIVE MEDIAN FILTER

Our design aims in determining the median value with the help of iterative sorter module, an adaptive computation and error detection module as shown in figure 1.

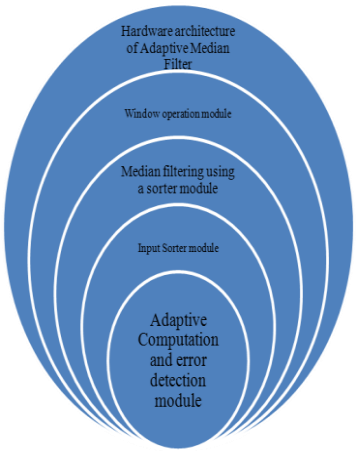

Fig 1: Iterative-AMF Overview

The various internal blocks and sub blocks are shown in figure 2. We are considering the window operation for 3x3 size. Nine D-FF's (DFF1-DFF9) are used to determine pixels W0-W8.

A. Sorter module

Sorter module comprises of three comparators and six multiplexers to generate the Max, Min and Med pixel values. The noisy image text file contains the 8-bit input image pixels data which is serially fed based on a clock signal. DFF-1 holds the 8-bit one-pixel value and forward next DFF2 and continue the operation till DFF-9 with a latency of 9 clock cycles. The DFF-9 stores the first-pixel output 'w0'.Similarly, DFF-1 stores the 9th-pixel output 'w8' and same operation continues till 65536 pixels. The 'w4' is the partial median value centre pixel (CP) for the 3x3 window operation which is used further in adaptive computation and error detection modules.

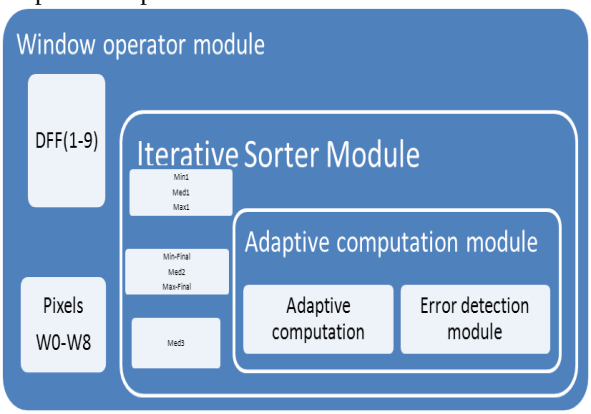

Fig 2: Internal architecture of I-AMF

3.2 Partial Median Filtered value using 3-Input Sorter Module

The median filtering is designed to find the median value using 3-input sorter module, also can see the maximum and minimum values which help to find the error pixels which is affected by the noise.

The median filtering module mainly includes nine 3-input sorter module which is connected according to the sorting order. The window w0-w8 outputs are inputted to the median filtering three 3-input sorter SM1, SM2, and SM3 modules and generate the three different output Minimum, median and maximum values which are connected in sorting order and are fed to SM4, SM5, and SM6. The maximum outputs of SM1, SM2 and SM3 are fed as inputs to SM4. This in turn generates the final Maximum value (Max).Similarly the minimum pixel values generated from SM1,SM2 and SM3 are given as inputs to SM6.SM6 generates the final minimum amount (min) and again continue the sorting operation in SM7, SM8, and SM9. SM-9 obtains the partial median filter values as indicated in fig2. Further these median values are fine tuned for more precise median value in adaptive computation and error detection process.

The 3-input sorter module mainly includes the three comparators and 6- Multiplexors. The window outputs 'w0' and 'w1' are applied to comp-1 to find the select line to mux-1 and mux-2. The comparator-1 works, if the 'w0 is greater than 'w1'then output is zero and if it is , then output is '1'.The mux-1 selects the inputs based on the select line which is generated by the comp-1. If the select line is zero, it will select the 'w0' else it will select 'w1'. The mux-2 output is input to the comp-2 along with input 'w2' and select line to mux-3 and mux-4. Mux-4 generates the minimum value (min). The mux-3 output is input to comp-3 along with mux1 output and chooses the line to mux-5 and mux-6. The mux-5 generates the maximum (max) value and mux-6 create the median (med) value.

3.3 Adaptive computation Module and Error detection

Adaptive computation is the main module works with adaptive nature. The outcomes of this module are the centre pixel (CP) output of the window module or median value of 3x3 window output and it depends on the adaptive decision. The adaptive computation module mainly includes four comparators, three-AND gates, and one Multiplexor. The median filtering outputs like minimum value (Min1), a maximum value (Max1) median value (Med1) and also centre pixel (w4) from window module input to four comparator modules followed by AND operations, and it gives the select line to MUX module. The centre pixel (w4) and Median value are inputted to the MUX module and obtain the filtered output represented in.

The error detection module gives the information of corrupted (error) and uncorrupted pixels of the filtered output image. It mainly contains two comparators and OR gate. The error signal is high when any one of the comparator outputs is high.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The design proposed for the implementation of the I-AMF is designed using verilog on hardware platform-Artix-7 board and simulated using Model Sim 6.5f. The various PSNR values are analysed for various standard images by keeping the noise level 10%.Figure 3 and Table 1 signifies the utilization of the hardware resources on the board. The implementation cost is directly proportional to the number of resources utilized like the slice registers, LUTs and the flip flops. I-AMF utilizes 74, 480 and 36 registers, LUTs and the flip flops respectively. The runtime is estimated to be 0.754ns with the device operating frequency of 1325.45 MHz. The dynamic power dissipated is 0.019W and the total power for the design is found to be 0.101W.

Table 1: Resource Utilization of I-AMF on Artix-7 FPGA

Resource Utilization-Artix-7 FPGA	Obtained
Area	
Slice Registers	74
Slice LUTs	480
LUT-FF pairs	36
Time	
Minimum period (ns)	0.754
Maximum Frequency (MHz)	1325.452
Power	
Dynamic Power (W)	0.019
Total Power (W)	0.101

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	74	126800	0%
Number of Slice LUTs	480	63400	0%
Number of fully used LUT-FF pairs	36	518	6%
Number of bonded IOBs	19	210	9%
Number of BUFG/BUFGCTRLs	1	32	3%

```
Minimum period: 0.754ns (Maximum Frequency: 1325.452MHz)
Minimum input arrival time before clock: 0.743ns
Maximum output required time after clock: 38.580ns
Maximum combinational path delay: No path found
```

Fig 3: Screenshot of Resource utilization for I-AMF

Table 2: PSNR and MSE values

Noise Level- 10%		
Images	**PSNR(dB)**	**MSE**
Cameraman	34.644	22.318
Lena	35.076713	20.202682
Peppers	34.869813	21.188
coins	36.130284	15.85083
Average	35.18	19.88

Table 2 indicates the PSNR and the MSE values for various standard image inputs. MSE signifies the cumulative squared error between the compressed and the original image. If the value of MSE is low then the error will be less. To determine PSNR, MSE value has to be computed which is given as:

$$MSE = \frac{1}{MN} + \sum_{y=1}^{M} \sum_{x=1}^{N} [I(x,y) - I'(x,y)x(n)]^2 \quad \ldots(1)$$

$$PSNR = 10\log_{10}(R^2/MSE) \quad \ldots\ldots\ldots\ldots\ldots\ldots(2)$$

M, N signifies the dimensions of an image. I(x, y) is the original image I'(x, y) is the compressed image. The various PSNR and the MSE values generated through hardware implementations for standard images are found to be sufficiently good for image processing applications.

Table 3 gives the exact number of corrupted pixels, uncorrupted pixels and percentage error of generation of a corrupted pixel after I-AMF is applied. The difference of the total number of pixels and the number of uncorrupted pixels indicate the corrupted pixels

Table 3: Percentage pixel Error calculation

Images	Uncorrupted pixels	Corrupted pixels	% Pixel Error
Cameraman	64951	585	0.89
Lena	65410	126	0.192
Peppers	65001	535	0.816
Coins	64394	1142	1.742
Average	64939	597	**0.91**

The corrupted and the uncorrupted pixels are generated through simulation results indicated in Figs 4 and 5. These figures also show the different standard images in original form, noisy form and filtered image. The spikes in the simulated output waveforms indicate the errors in the corresponding pixels after filtering. On an average 0.91% error is observed for various standard images shown below.

Fig 4(a)

Fig 4(e)

Fig 4(i)

Fig 4(b)

Fig 4(f)

Fig 4(j)

Fig 4(c)

Fig 4(g)

Fig 4(k)

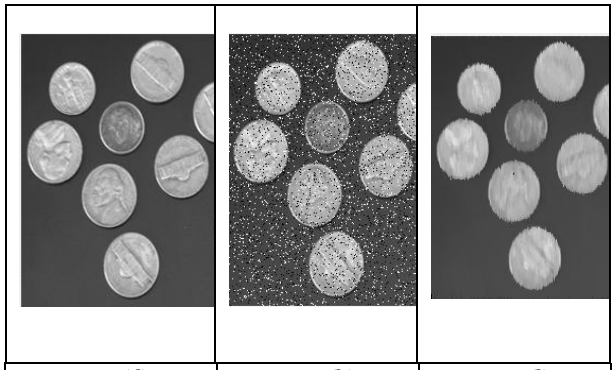

Fig 4(d)	Fig 4(h)	Fig 4(l)

Figure 4: Hardware results after Filtering, Original images (a-d), Noisy Images (e-h) and Filtered images (i-l)

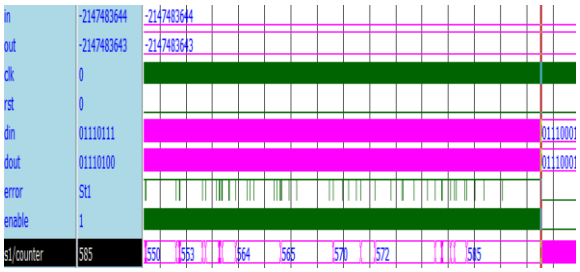

Figure 5: Simulation results indicating the error pixels

V. CONCLUSION AND FUTURE WORK

The paper proposes one of the technique to achieve median filtering and has some significant results which indicates that greater PSNR values cannot be attained using the hardware approach unlike the software implementations. The spikes in the error waveform indicate the corrupted pixels transmitted. The need for hardware implementation arises in various image and video transmission applications and hence by considering the type of application the method may be decided. The work is extended to be implemented on a SoC environment using various high speed transmission protocols in a chip.

REFERENCES

1. Chun-mei WANG and Tian-yi LI," An Improved Adaptive Median Filter for Image Denoising" 3rd International Conference on Computer and Electrical Engineering (ICCEE 2010) IPCSIT vol. 53 (2012) © (2012) IACSIT Press, Singapore DOI: 10.7763/IPCSIT.2012.V53.No.2.6.
2. Zhiying Song, Huiyan Jiang, and Siqi Li, **"***A Novel Fusion Framework Based on Adaptive PCNN in NSCT Domain for Whole-Body PET and CT Images***"** https://doi.org/10.1155/2017/8407019
3. Sukhwinder Singh, Dr. Neelam Rup Prakash *" Modified Adaptive Median Filter for Salt & Pepper Noise" International Journal of Advanced Research in Computer and Communication Engineering Vol. 3, Issue 1, January 2014*.
4. Bisht, Rashmi, and Ritu Vijay. *"Hardware implementation of real time window based switching median filter." International journal of Engineering sciences & Research technology 6.7 (2017): 732-40. Web. 25 July 2017.*
5. Mohammad Ismaeil, Keisham Pritamdas, Kh. Jilen Kumari Devi and Samarth Goyal *"Performance Analysis of New Adaptive decision based median filter on FPGA for Impulsive Noise Filtering" 978-1-5386-1703-8/17/$31.00 ©2017 IEEE*
6. M. C Hanumantharaju, M. Ravishankar, D. R Rameshbabu, and S. B Satish, "A Novel FPGA Implementation of Adaptive Rank Order Filter for Image Noise Removal" International Journal of Computer and Electrical Engineering, Vol. 4, No. 3, June 2012
7. Parinita Walivadekar, Dr. D. S. Bormane , "Hardware and Software Implementation of Median Filter in Image Processing Application") International Journal of Engineering Sciences & Research Technology [2904-290]
8. Dr. K. Bikshalu, R. Srikanth, "Nonlinear Filter Based Restoration of Compressed Medical Image Using AMF", International Journal of Advanced Research in Computer Science and Software Engineering 6(1), January - 2016, pp. 50-56.
9. Jiafu Jiang, Jing Shen, "An Effective Adaptive Median Filter Algorithm for Removing Salt & Pepper Noise in Images" 978-1-4244-4964-4/10/$25.00 ©2010 IEEE

AUTHORS PROFILE

Archana H R, Assistant Professor, Department of Electronics & Communication Engineering, BMSCE, Bengaluru. She has completed her B.E and Mtech degrees from VTU. She has around 10 years of Experience in Teaching and 1 year Industrial Experience. She has published her papers in 2 international journals, presented in 7 international conferences and 2 national conferences. She is pursuing her Ph.D. from VTU. Her Research area is VLSI and Imaging SOC.

Dr C R Byra Reddy graduated from Bangalore University with B.E degree in Instrumentation technology and M E degree in Electronics in 1990 and 1999 respectively. He is currently professor in Department of Electronics & communication Engineering, BIT, Bangalore. He got his PhD from SV University of Engineering, Tirupati. His research areas include Microwave communication, Antennas & Wave propagation with a keen interest in Analysis & design of patch antenna for wireless communication. He has published more than 36 papers in national/International journals. He has also presented paper at ICONSPACE 2011 in Malaysia.

Dr C P Narendra graduated from Bangalore University with B.E degree in Electronics & Instrumentation from Bangalore University ,Mtech in Electronics and digital communication and PhD in Signal Processing from VTU. He is currently Associate Professor in Department of Electronics & communication Engineering, BIT, Bangalore. His research areas include Image, signal processing and VLSI . He has published more than 10 papers in national/International journal and has presented papers at various international conferences .

.