An Improved Area Efficient 16-QAM Transceiver Design using Vedic Multiplier for Wireless Applications

S. Dhanasekar, P. Malin Bruntha, C. Arunkumar Madhuvappan, K.Martin Sagayam

Abstract: ***In this research article, an improved area efficient 16-Quadrature Amplitude Modulation (QAM) transceiver design is introduced using Vedic multiplier. The 16-QAM design is transmitted using Pseudo Random Binary Sequence (PRBS) and modulated by changeable clock frequencies. The Vedic multiplier uses Urdhva Tiryakbhyam (Vertical and Crosswise) method of multiplication to reduce the undesirable steps and generates parallel partial products. Compressor adders are used in the Vedic multipliers, which helps to increase the speed of multiplication process and reduces the carry delay. Four Compressor adders namely 5-3, 10-4, 15-4 and 20-5 are used in a 16-bit Urdhva Tiryakbhyam Vedic multiplier to add its partial products. The proposed 16-QAM design is implemented using Spartan-3 XC3S200-5 pq208 Field Programmable Gate Array (FPGA) device which occupies 672 slices, 1102 4-input Look up Tables (LUTs) and 39 mW of power consumption. The Vedic multiplier based 16-QAM transceiver design reduces 17.2% slices and 4.5% 4-input LUTs. The 16-QAM is a preferred digital modulation method in the Orthogonal Frequency Division Multiplexing (OFDM) system, which reduces bit errors and noise effects during data transmission. The OFDM transceiver design is used in the high-speed wireless communication by excellence of its Multi-carrier modulation method.***

Index Terms: **BPSK, OFDM, OQSK, PRBS, QAM, QPSK**

I. INTRODUCTION

Today, the growth of wideband wireless communication system has been raised due to customer interest towards high-speed wireless communication in which OFDM transceiver design plays vital role. The OFDM system used for high speed data transmission by virtue of its Multi-carrier modulation techniques and intended for high spectral efficiency. The orthogonal subcarriers in an OFDM system offer narrow bandwidth. The different modulation techniques, such as Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), Offset Quadrature Phase Shift Keying (OQPSK), QAM etc., are used for transmitting the subcarriers of the OFDM system. For modulating the information signals towards carrier signals, QAM is one of the extensively used modulation technique. QAM is also used for radio communications [1]. QAM provides various advantages over other modulation techniques, as it carries data on both amplitude and phase. There are various forms of QAMs available namely 16-QAM, 32 QAM, 64 QAM, 128 QAM and 256 QAM [2].

In 16-QAM modulation method, two carrier signals shifted by 90 degree phase difference are used to modulate data and the resultant output signal has both phase and amplitude variations [3]. There are various 16-QAM transceiver designs achieve an area efficient architecture in FPGA has been studied [4]–[7].The 16-QAM is a preferred digital modulation technique in wireless communication, which reduces noise effects and bit errors during data transmission. The 16-QAM design is used in digital terrestrial television using Digital Video Broadcasting (DVB) and Wireless Fidelity (WIFI) Networking Standards.

The QAM modulated signal is multiplied with sine and cosine carriers using Vedic multiplier. Urdhva Tiryakbhyam (Vertical and Crosswise) multiplication method used in the Vedic multiplier, which helps to reduce hardware complexity as studied [8]-[12]. The compressor adders based Vedic multiplier is used to add the parallel partial products and reduce the propagation delay in the multiplier circuit [13].

Several 16-QAM transceiver designs have been reviewed for acquiring area efficient architecture. The existing 16-QAM transceiver designs occupied more hardware area in the silicon chip. Hence, there is a requirement for implementing an area efficient QAM transceiver design. An improved area efficient 16-QAM transceiver design has been proposed. In this paper, a 16-QAM transceiver design is selected for transmitting digital information towards band-pass channels to reduce bandwidth and increase the data rate. The proposed 16-QAM design is transmitted through Pseudo Random Binary Sequence and it is modulated by variable clock frequencies (150 Hz to 19.2 KHz). Urdhva Tiryakbhyam Vedic multiplier used in 16-QAM design provides an area efficient architecture. For accuracy in simulation, testing and implementation of the proposed design in the hardware, FPGA technology can be used which is more flexible and reliable [14].

Manuscript published on 30 September 2019
* Correspondence Author
S. Dhanasekar*, Department of Electronics and Communication Engineering, Sri Eshwar College of Engineering, Coimbatore, India. Email:dhanasekar.sm@gmail.com
P. Malin Bruntha, Department of Electronics and Communication Engineering, Karunya Institute of Technology and Sciences, Coimbatore, India. Email:malin@karunya.edu
C. Arunkumar Madhuvappan, Department of Electronics and Communication Engineering, Vinakaya Misson's Kirupanada Variyar Engineering College, Salem, India. Email:amadhuvappan@gmail.com
K. Martin Sagayam, Department of Electronics and Communication Engineering, Karunya Institute of Technology and Sciences, Coimbatore, India. Email: martinsagayam.k@gmail.com

The Vedic multiplier based 16-QAM transceiver design implemented using Spartan 3FPGA, describes the step by step journey of signal transmission from source to destination with serial bit patterns.

This paper methodized the Quadrature Amplitude Modulation in Section II. Section III discusses an Urdhva Tiryakbhyam based Vedic multiplier using compressor adders. Section IV portrays a proposed 16-QAM design using Vedic multiplier. The results of 16-QAM transceiver design are discussed in Section V. Finally, a conclusion is presented in Section VI.

II. QUADRATURE AMPLITUDE MODULATION

The Quadrature Amplitude Modulation is widely used in many digital communication applications. In 16-QAM modulation technique, the two sinusoidal carrier signals are modulated independently by 90 degree phase shift and demodulated separately at the receiver. A 16-QAM is the band pass digital modulation, which modulates both the amplitude and phase of the carrier signal and provides better error performance in the receiver. The two carrier signals In-phase (I) and Quadrature phase (Q) in 16-QAM design are represented as

$$I(t) = a_i \cos(2\pi f_c t) \quad (1)$$

$$Q(t) = b_i \sin(2\pi f_c t) \quad (2)$$

where I (t) and Q (t) are modulating signals and f_c represents the carrier frequency.

In 16-QAM, a total of 16 possible states (symbols) and each symbol consist of four bits (i.e.) two bits for I and two bits for Q components. There are 16 symbols in the QAM design and each symbol has two gray coded bits of I and Q .A Constellation diagram is used to plot those symbols in rectangular space. The 16-QAM design has 4 amplitudes and 12 phases. The discrete amplitudes used for 16-QAM design are ±3 and ±1. A Constellation diagram of the 16-QAM design is shown in Fig. 1. In symbol mapper, transition will occur between states at each symbol time [4].

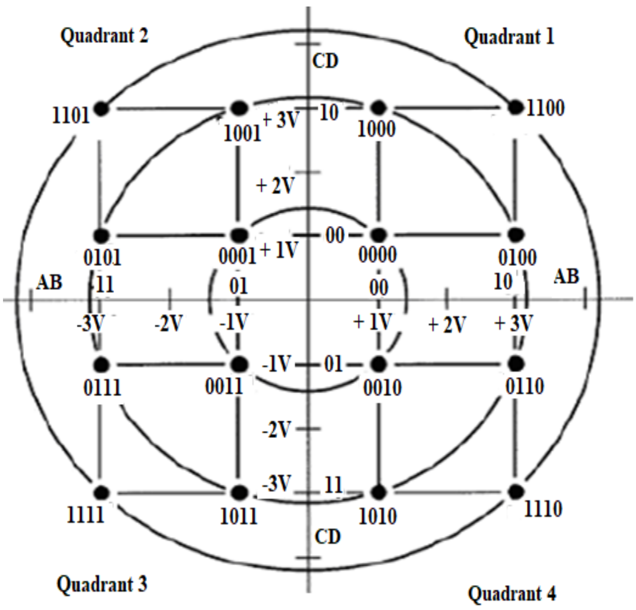


Fig. 1. Constellation diagram of 16-QAM

The general form of a 16 QAM signal is expressed as [15]

$$T_x(t) = \sqrt{\frac{2E_{min}}{T_s}}\, a_i \cos 2\pi f_c t + \sqrt{\frac{2E_{min}}{T_s}}\, b_i \sin 2\pi f_c t$$

$$0 \le t \le T_s;\ i = 1, 2, 3, 4 \ldots 16 \quad (3)$$

where, E_{min} gives the energy of the signal having the least amplitude, f_c as carrier frequency, T_S as symbol period and a_i and b_i represents a pair of independent integers which will be chosen as per the location of a particular signal point.

In the 16-QAM constellation diagram, rectangular pulse shapes are pretended, the signal T_x (t) can be expanded into a pair of basis function represented as

$$\varphi_1(t) = \sqrt{\frac{2}{T_s}}\cos(2\pi f_c t);\ 0 \le t \le T_s \quad (4)$$

$$\varphi_2(t) = \sqrt{\frac{2}{T_s}}\cos(2\pi f_c t);\ 0 \le t \le T_s \quad (5)$$

III. URDHVA TIRYAKBHYAM VEDIC MULTIPLIER

Vedic multiplication is an ancient form of mathematics reconstituted from the old-fashioned Indian scriptures named as Vedas [16]. Vedic mathematics has sixteen mathematical formulas which are named as Sutras. The Vedic sutra provides unique approach of solving the mathematical calculation, such as trigonometry, algebra, arithmetic and calculus into a simpler form [17]. Urdhva Tiryakbhyam (Vertical and Crosswise) sutra is used in the Vedic multipliers to reduce the repetitious multiplication steps and generates parallel partial products. This Vedic sutra is used in the digital multiplication which helps to reduce the hardware complexity and propagation delay in the multiplier circuit. Urdhva Tiryakbhyam algorithm rule is used to generate n x n bit multiplications. A simple 4-bit digital multiplier architecture based on Urdhva Tiryakbhyam (Vertical and Crosswise) sutra is shown in Fig. 2.

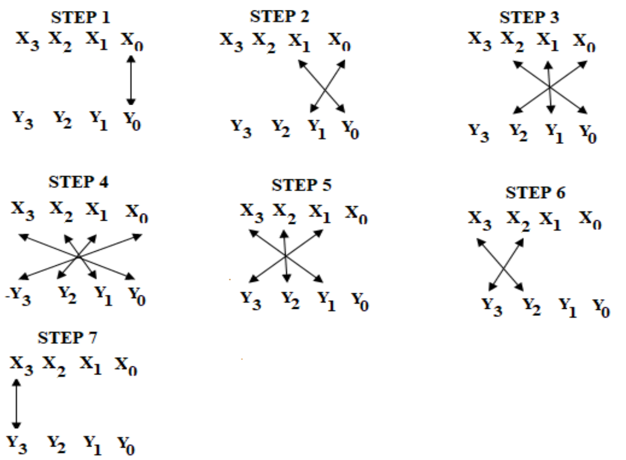


Fig. 2. Urdhva Tiryakbhyam multiplication of two 4-bit binary number

Urdhva Tiryakbhyam multiplication rule used for two binary numbers X and Y made by four bits each, i.e., (X_3 – X_0) and (Y_3 – Y_0) [18].

The final output of Urdhva Tiryakbhyam 4 x 4 Vedic multiplier is expressed in the below equations (6) – (12) accordingly to acquire the ultimate product.

$$P_0 = X_0 Y_0 \quad (6)$$

$$C_1P_1 = X_1Y_0 + X_0Y_1 \quad (7)$$

$$C_2P_2 = C_1 + X_2Y_0 + X_1Y_1 + X_0 Y_2 \quad (8)$$

$$C_3P_3 = C_2 + X_3Y_0 + X_2Y_1 + X_1Y_2 + X_0Y_3 \quad (9)$$

$$C_4P_4 = C_3 + X_3Y_1 + X_2Y_2 + X_1Y_3 \quad (10)$$

$$C_5P_5 = C_4 + X_3Y_2 + X_2Y_3 \quad (11)$$

$$C_6P_6 = C_5 + X_3Y_3 \quad (12)$$

Compressors adders are use to add more than four data bits at a time and achieves less propagation delay over conventional combinational circuits like half adders and full adders [19]. It is used to reduce the gate count and delay while performing addition operation, therefore it is called as compressor. The partial products attained in the Urdhva Tiryakbhyam Vedic multiplier are added using compressor adder. 16-bit Vedic multipliers are used in 16-QAM transceiver design. To add the parallel partial products of 16-bit Vedic multipliers, four compressor adder architectures namely 5-3, 10-4, 15-4, and 20-5 are used. The compressor adders are used to enhance the speed of the multiplication process and reduce the critical delay as compared to existing adder architectures.

A 5-3 compressor adder architecture used in 16-bit Vedic multiplier is shown in Fig. 3 [20].This adder circuit adds five bits [P_0 – P_4] at a time and yields three bit output [S_0 – S_2]. It is designed using logic gates, half and full adders.

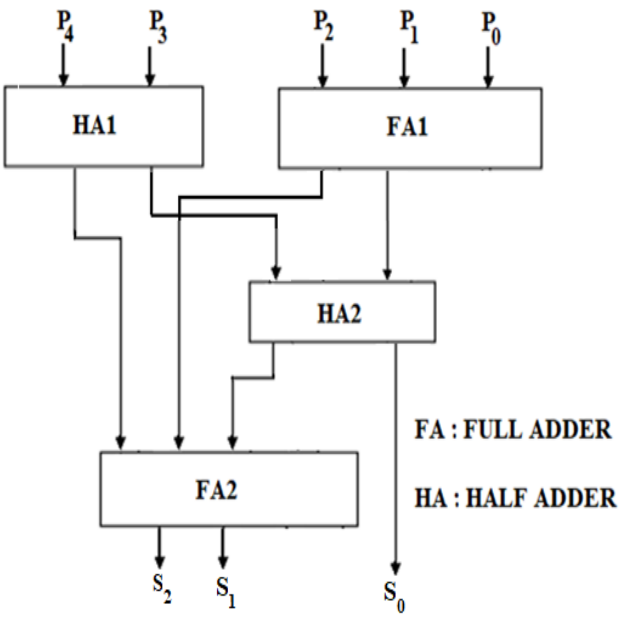


Fig. 3. 5-3 compressor adder with half adders and full adders

A 10-4 compressor adder architecture used in 16-bit Vedic multiplier is shown in Fig. 4 [20].This adder circuit adds ten bits [P_0 – P_9] at a time using two 5-3 compressor adders and yields four bit output [S_0 – S_3] . A 10-4 compressor adder circuit used to reduce delay and enhanced the speed of the multiplier circuit.

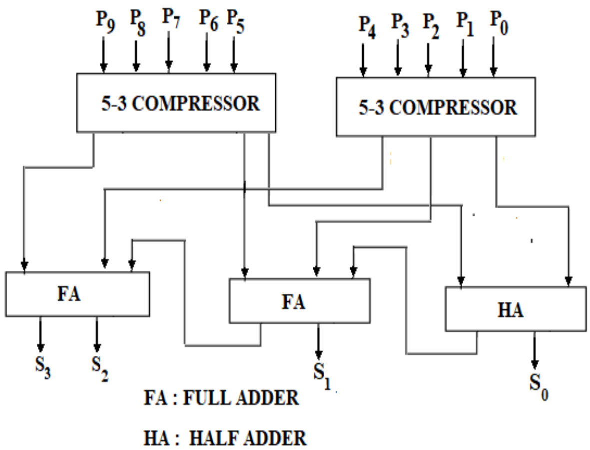


Fig. 4. 10-4 compressor adder using 5-3 compressor adders

A 15-4 compressor adder is used to add 15 bits [P_0 – P_{14}] at a time using two 5-3 compressor adder, four bit parallel adder and obtained four bit output [S_0 – S_3]. A 20-5 compressor adder architecture used in 16-bit Vedic multiplier is shown in Fig. 5 [20]. This adder circuit adds 20 bits [P_0 – P_{19}] at a time using a 15-4 and 5-3 compressor adder, two half and full adders and obtains five resultant bits [S_0 – S_4].

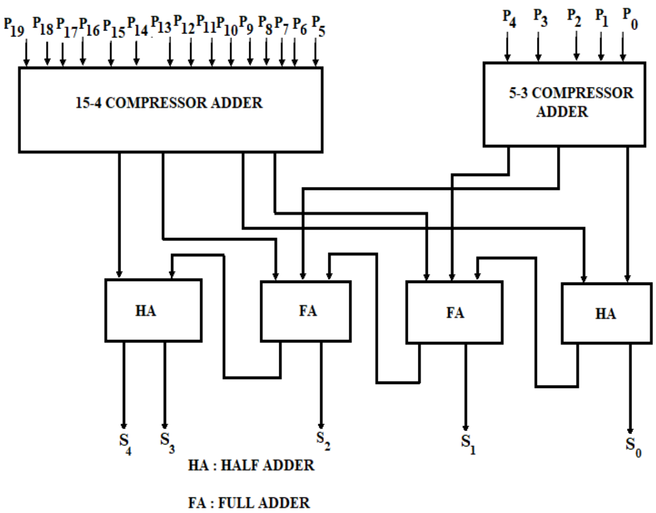


Fig. 5. 20-5 compressor adder using 15-4 and 5-3 compressor adder

The multiplier structures used in the 16-QAM design increases the latency and processing time. The compressor adder based on Urdhva Tiryakbhyam Vedic multipliers are used in the 16-QAM transceiver design improves speed performance and reduced the carry delay as compared to existing multiplier architectures. The parallel partial products obtained in the 16-bit Urdhva Tiryakbhyam are added using 5-3, 10-4, 15-4, and 20-5 compressor adders.

IV. PROPOSED 16-QAM TRANSCEIVER DESIGN USING VEDIC MULTIPLIER

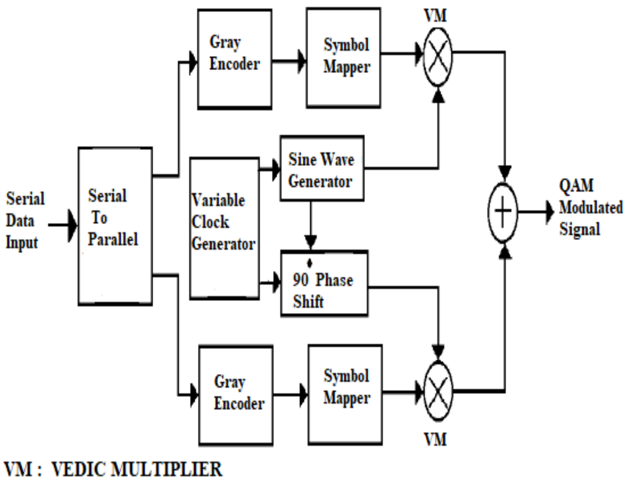


Fig. 6. Block diagram of proposed QAM transmitter

The proposed Vedic multiplier based 16-QAM transmitter is shown in Fig 6. The digital data pattern is generated using Pseudo Random Binary Sequence logic and it flows serially as an input to QAM transmitter. Linear feedback shift register (LFRS) is used to generate Pseudo Random Binary Sequence. LFSR is a shift register logic whose input bit is in XOR feedback with output bit values. The incoming serial data is encoded by means of four bits and it is divided into two streams as In phase (I) & Quadrature (Q). The odd values from the encoded bits are taken for I component and even values are taken for Q component. The I and Q bits flows into gray encoder block to reduce the bit errors during data transmission. The symbol mapper is used to combine gray coded bits of I and Q to form symbols. The gray coded bits of I and Q are modulated by variable clock frequencies (150 Hz to 19.2 KHz) with sine and cosine carriers to attain in phase modulation and Quadrature modulation. Finally, both the modulations are added to form QAM modulated signal. The QAM modulated signal is varied by amplitude and phase.

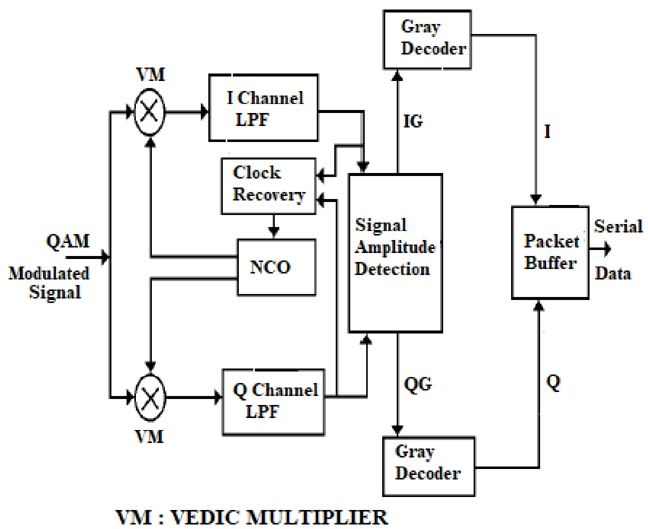


Fig. 7. Block diagram of proposed QAM receiver

The block diagram of the Vedic multiplier based QAM receiver design is shown in Fig. 7. The QAM modulated signal flows as input to QAM receiver. The sine and cosine carriers are generated using Numerically Controlled Oscillator (NCO). The compressor adder based Urdhva Tiryakbhyam Vedic multiplier used to multiply the QAM modulated signal with carrier signals, to obtain I and Q demodulation signals. The word length of carrier signals and QAM modulated signal has taken as 16-bits. The parallel partial products obtained in the Vedic multiplier are added using four compressor adder namely 5-3, 10-4, 15-4, and 20-5 adder circuits. To eliminate the high frequency components in I and Q demodulated signals, it is transmitted into low pass filter blocks. The filtered I and Q demodulated signal flows into signal amplitude detection block, to group data range and attain the transmitted data. Accordingly, the resultant bits IG & QG from the signal amplitude detection block flows into gray decoder block, to obtain the Pseudo Random Binary Sequence transmitted data.

V. SIMULATION RESULTS AND DISCUSSIONS

The proposed Vedic multiplier based 16-QAM transceiver is implemented using Spartan 3 XC3S200-5 pq208 FPGA board. The Spartan 3 FPGA device is fabricated on advance 90 nm technology can withstand up to 5 million system gates with the lowest cost and it is used for data communication applications. The specification of 16-QAM transceiver design is listed in Table 1.

Table-1: Specifications 16-QAM Transceiver design

Master clock	48 MHz
FPGA	Spartan 3 XC3S200-5 pq208
Bit Pattern	Pseudo Random Binary Sequence
Variable Clock Generator	150 Hz to 19.2 KHz
Modulation Techniques	16-QAM
Data rate	12 Mbps
Multiplier	16-bit Vedic Multiplier
Adder	Compressor Adder

The 16-QAM transceiver design has been developed using Verilog HDL and simulated using Modelsim 6.2c simulator. The Pseudo Random Binary Sequence flows serially as an input to 16-QAM transmitter. The simulation results of the bit pattern followed by gray coded bits of I and Q are shown in Fig. 8.

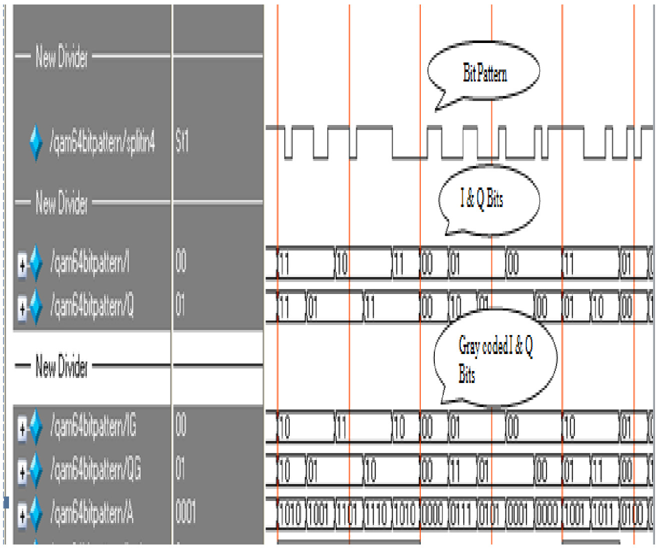


Fig. 8. Simulation results of proposed 16-QAM transmitter

The digital bit pattern is encoded using four bits and it is divided into two streams as Inphase (I) & Quadrature (Q). I stream has odd values of the bit pattern and Q stream has even values of the bit pattern. The Inphase & Quadrature data bits are gray coded, to reduce bit errors during data transmission. The simulation results of the variable clock frequencies used in the proposed 16-QAM design is shown in Fig. 9.

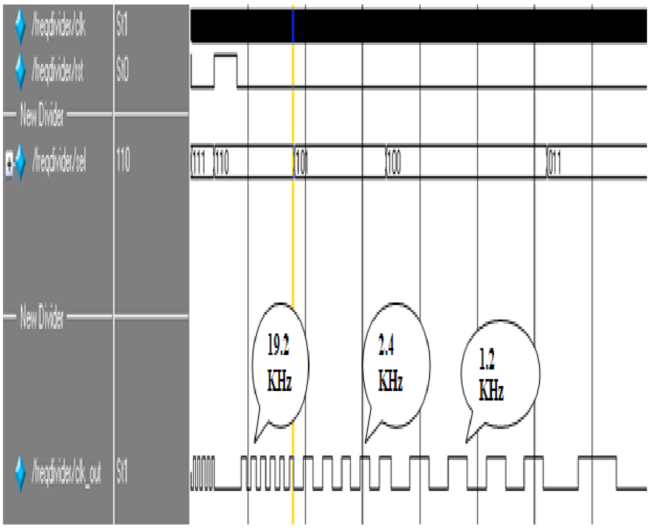


Fig. 9. Simulation results of variable clock frequencies in proposed 16-QAM transceiver

The I & Q signals are modulated by sine and cosine carriers with changeable clock frequencies (150 Hz to 19.2 KHz) to achieve Inphase modulation and Quadrature modulation. Finally, the two modulations are added to form QAM signal. The simulation waveform of QAM transmitter is shown in Fig. 10.

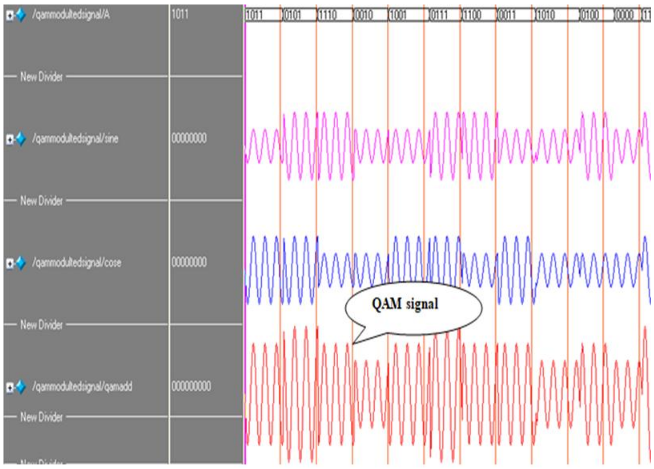


Fig. 10. Simulation waveforms of QAM signal

In QAM receiver, the modulated QAM signal is multiplied with carrier signals using Vedic multiplier, to obtain Inphase (I) and Quadrature (Q) demodulation signal. The simulation result of compressor adder based 16-bit Vedic multiplier which is shown in Fig. 11.

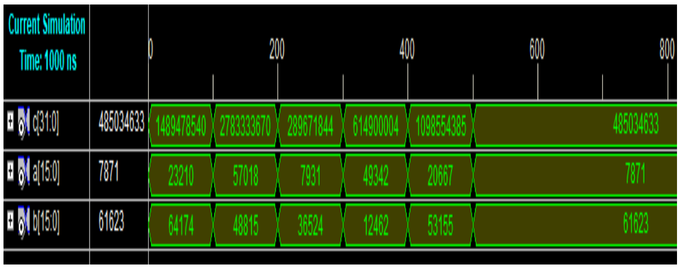
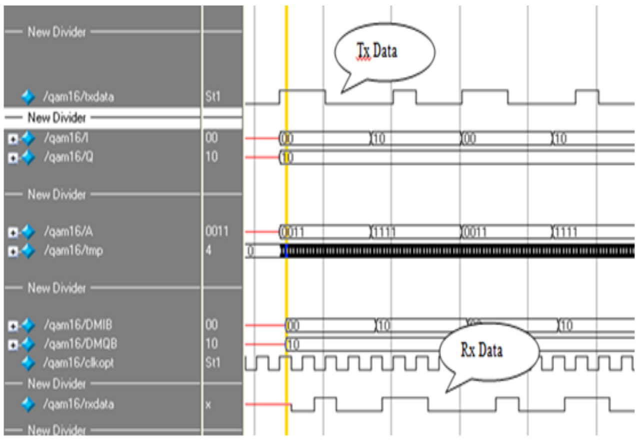


Fig. 11. Functional simulation of 16-bit Vedic multiplier

The blocks like low pass filter and signal amplitude detection are used to demodulate the QAM transmitted signal and decoded using gray coder to achieve serial transmitted data. The transmitted and received bit patterns of 16-QAM transceiver are shown in Fig. 12.



Tx Data - Transmitted Data
Rx Data - Received Data

Fig. 12. Simulation results of transmitted and received bit patterns

The RTL schematic of the Vedic multiplier based 16-QAM transceiver design is shown in Fig. 13. The 16-QAM transceiver design is implemented using Spartan-3 FPGA device occupies 672 slices, 1102 4-input LUTs and 39 mW of power consumption. Table 2 exhibits the comparison results of various 16-QAM designs.

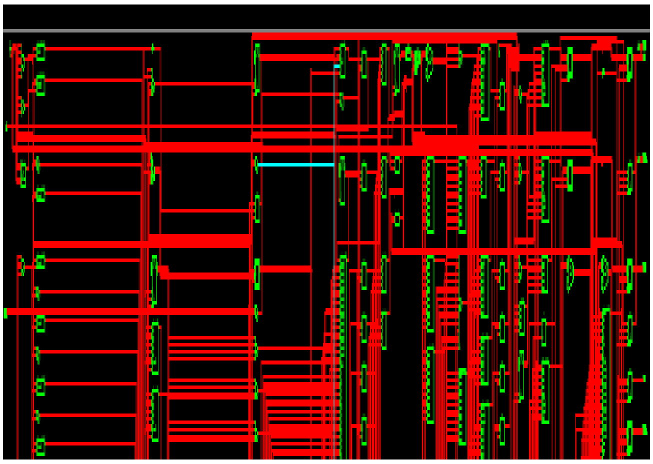


Fig. 13. RTL schematic of proposed 16-QAM transceiver

Table-II: Performance comparison of various 16-QAM Designs

Parameters	**Proposed 16-QAM transceiver**	**Tarig Hyder Makki *et al.* 2015.**	**Satyanarayana *et al.* 2011**
FPGA	Spartan 3	Spartan 3	Spartan 2E
Device	XC3S200 -5 pq 208	XC3S 50 -4 pq 208	XC2S200 -5 pq 208
No. of Slices	672	812	2922
No. of Slices flip flops	384	1238	2252
No. of 4 input LUTs	1102	1154	4674
Gate count	66,232	83,839	151,213
Maximum Frequency	132.31 MHz	85.31 MHz	102.41 MHz

The Vedic multiplier based 16-QAM design reduces 17.2% slices and 4.5% 4-input LUTs compared to the 16-QAM design (Tarig Hyder Makki *et al.* 2015). The same 16-QAM design reduces 77% slices and 76.4% 4-input LUTs compared to the existing 16-QAM design (Satyanarayana *et al.* 2011). The 16-QAM design occupies 66K gates and operates with maximum frequency of 132.31 MHz in Spartan 3 FPGA device. As compared to existing 16-QAM designs, Vedic multiplier based 16-QAM occupies less slices and LUTs in the FPGA device. Hence the proposed 16-QAM provides an area efficient architecture in FPGA

VI. CONCLUSION

In this paper, compressor adder based Vedic multiplier is introduced into 16-QAM transceiver design to obtain area efficient FPGA architecture. The 16-QAM design is implemented using a Spartan-3 XC3S200-5 pq208 FPGA board which occupies 66K gates and operates with clock frequency of 132.31 MHz. As compared to existing 16-QAM design, the Vedic multiplier based 16-QAM design achieves significant area reduction in FPGA. The proposed 16-QAM design attained 17.2% reduction in number of slices and 4.5% reduction in 4-input LUTs. 16-QAM is selected digital modulation technique which reduces bit errors during digital data transmission. Hence, the proposed 16-QAM design can be used in OFDM system for high speed wireless applications.

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AUTHORS PROFILE

Dr. S. Dhanasekar received his Bachelor of Engineering degree in Electrical and Electronics Engineering from K.S.Rangasamy College of Technology, Erode, Tamilnadu, India in 2004 and received his M.S Degree in VLSI CAD from Manipal Centre for Information Sciences, MAHE, Manipal, Karnataka, India in 2006. He worked as R & D Engineer (VLSI and DSP Division) in Scientech Technologies Pvt. Ltd, Indore, Madhya Pradesh, India. He has completed his Ph.D. degree in Information and Communication Engineering from Anna University, Chennai, India in 2019. He is currently working as Associate Professor in Electronics and Communication Engineering, Sri Eshwar College of Engineering, Coimbatore, Tamilnadu. His teaching & research interests includes low power VLSI design, signal processing and communication systems.

Mrs. P. Malin Bruntha working as an Assistant Professor in the Department of Electronics and Communication Engineering, Karunya Institute of Technology and Sciences, Coimbatore. She completed her B.E Electronics and Communication Engineering from Anna University. She completed her post graduate studies (M.E. Applied Electronics) at Anna University Regional Center, Tirunelveli. Her research area includes image processing, computer vision and VLSI. She has published four research papers to her credit in peer reviewed Scopus indexed journals. Her passion is to motivate and invigorate the young minds in the ever-green field of Electronics and Communication engineering

Dr. C. Arunkumar Madhuvappan working as an Assistant professor in the department of ECE, Vinayaka Mission’s Kirupananda Variyar Engineering College, Salem, Tamil Nadu. He received the B.E. degree in Electronics and Communication Systems from Anna University, Chennai in the year 2005. He obtained his M.E. Degree in Communication Systems in the year 2007 from Anna University, Chennai. He completed his Ph.D. degree in the year 2019. He is a Life Member of the Indian Society for Technical Education (ISTE). He is having 10 International Journal Publications and more than 6 National and International conferences.

Dr. K. Martin Sagayam received his Ph.D in the research field of Signal, Image processing and machine learning approaches in 2018. Master degree in Communication Systems from Anna University in the year 2012 and B.E degree in Electronics and Communication Engineering from Anna University in the year 2009. Currently, he is working as an Assistant Professor in the Department of Electronics and Communication Engineering at Karunya Institute Technology and Sciences (Deemed University). He has authored/ co-authored in several referred International Journals, and conferences. He has authored 3 book chapters with reputed international publishers. He is an active member in various professional bodies. His area of interest includes pattern recognition, artificial intelligence, big data security, privacy preserving and signal processing.