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Characterization of SiO_2/SiC Interface of Phosphorous-Doped MOS Capacitors by Conductance Measurements

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Abstract*: *Interface states of MOS structures capacitors incorporated with low levels of phosphorous have been investigated by conductance and C-ψ_s method. The frequency response of interface states was observed by the conductance method up to 10 MHz. The correlation between the frequency response of interface states and interface state density determined by C-ψ_s method was studied. It was found that fast states in phosphorous incorporated samples reduced significantly at high frequency (>5 MHz) while sample annealed with nitrogen remained high up to 10 MHz. The interface state density, D_{it} of phosphorous incorporated sample near conduction band is lower compared to nitridated sample. These results indicate phosphorous passivation effectively reduces D_{it} at the SiO_2/SiC interfaces and can be correlated to high channel mobility.

Index Terms*: *MOS capacitor, Phosphorus, Interface state density, Fast trap, 4H-SiC MOSFET.

I. INTRODUCTION

Silicon carbide, (SiC) is one of the alternative materials for high power, high voltage, high temperature and high-frequency devices due to its superior properties such as high breakdown voltage, low intrinsic carrier concentration and high electron mobility. In recent times, the research in SiC material has extensively progressed and SiC devices are now commercially available. However, SiC devices are still far less mature than their counterparts (silicon devices) in term of reliability and performances. For example, SiC MOSFETs have been suffering from low channel mobility, which mainly caused by poor SiO_2/SiC interface properties. Nitridation is the most common technique to reduce the interface state density, D_{it} by passivating defects that exist at the interface [1][3][4]. Even though many reported that remarkable reduction of interface state density, D_{it} can be achieved by nitrogen passivation, yet the field-effect mobility, μ_{FE} has been restricted to around 50 $cm^2 \cdot Vs^{-1}$ on (0001) off-axis substrates.

H. Yoshioka et al. reported that the conventional high low and conductance method using frequency range of 0.1 to 1MHz are not able to detect fast states that exist at the interface and result in underestimation of D_{it} at a specific energy level near to the conduction band. A new method, (so-called C-ψ_s) was proposed to accurately determine the interface state density, D_{it} in SiC MOS capacitors [11]. C-ψ_s method is much better than other methods because it can detect all type of interface states than respond in any frequencies by evaluating the difference between quasi-static and theoretical capacitance.

Conductance method has been one of the most popular method to understand the electrical activity at the interface of MOS structure capacitors. Different from other techniques, this technique can determine the capture cross-section in addition to interface state density. Conductance method measures the loss in a MOS capacitor as a function of measurement frequency at a diverse energy level in the depletion region. Each interface states have a single trapping time constant (capture cross-section) will produce a loss peak at a characteristic frequency. Different type of traps has a different capture cross-section and surface potential fluctuations resulting in a broadening of loss peak. The capture cross-section seems most likely influenced by defects from acceptor and donor states in the annealing process, but their chemical nature is unknown.

In order to elucidate the limitation of the field effect mobility of nitrogen passivated samples which is approximately 50 cm^2Vs^{-1}, the samples annealed in nitrous oxide (NO) at various temperatures were investigated by the conductance and C-ψ_s and method [12]. The results show that a huge portion of reduction in interface state was cancelled by the generation of very fast state that can only be detected by high-frequency measurement at 100 MHz or higher.

Beside nitridation, $POCl_3$ annealing or phosphorous passivation process also leads to lower interface state density and higher field effect mobility [3][6].

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A significant phosphorus-induced field effect mobility improvement of ~125 cm^2Vs^{-1} was achieved by [2][3]. Therefore, it is important to reveal the factor that lowers the D_{it} and increases the mobility at the phosphorous incorporated SiO_2/SiC interfaces. In this paper, the fast states of interface states incorporated by phosphorous at SiO_2/SiC interfaces were investigated using the conductance method and revealed that the fast states at high frequency can be successfully reduced by the incorporation of phosphorous atoms at the interfaces.

II. EXPERIMENT AND EVALUATION METHODS

Two samples of 4H-SiC wafers (Silicon face, 4° off-axis, N_D= 1.4 × $10^{17}cm^{-3}$) with a different process of gate dielectric are compared. The gate dielectric for Sample 1 was fabricated by a thermal oxide oxidation process that has been through the post oxide annealing process, as a reference sample. The gate dielectric for Sample 2 was annealed in a planner source of PHOS after thermal oxidation. Both wafer processes are intended to be well-matched with a commercial process. Process details are summarized in Table 1.

Table 1. Summary of the fabrication process of MOS capacitor for both samples 1 and 2

Sample	Gate dielectric	Effective oxide thickness (nm)	Capacitor Size (um^2)
1	Thermal oxidation + anneal + nitride cap	33	~1.1×10^5
2	Thermal oxidation + anneal (phosphorous source) + nitride cap	36	~1.1×10^5

The measurements were performed using a Keithley 4200 parameter analyzer and a Cascade Summit probing station. The quasi-static measurements were performed using the ramp rate method and the current measured using 4200-PA PreAmps with a delay time of 0.1s. In all measurements, the voltage was swept from the depletion region to the accumulation region at a rate of 0.1 V/s.

The extraction of D_{it} from the capacitance data requires accurate knowledge of the surface potential,ψ_s. Following the technique described in, the surface potential is extracted from capacitance characteristics in the depletion region using

$$\psi_s(V_G) = \int \left(1 - \frac{C_S}{C_{ox}}\right) d\,V_G + A \qquad (1)$$

where C_{ox} is the capacitance under accumulation and A is an integration constant that lowers by ensuring that the extrapolated $1/(C_D+C_{IT})^2$ versus ψ_s data in the depletion region meets the origin. The interface state density is then determined using equation 2, which is based on the difference between quasi-static and theoretical capacitance.

$$D_{it} = \frac{(C_D+C_{IT})_{QS}-(C_D)_{theory}}{Ae^2} \qquad (2)$$

The theoretical semiconductor capacitance (C_D, theory) can be calculated by using the surface potential obtain from the Eq (1)[5][7].

$$C_{D,theory}(\psi_s) = \frac{AqN_D\left|exp\left(\frac{q\psi_s}{kT}\right)-1\right|}{\sqrt{\frac{2kTN_D}{\varepsilon_{SiC}}\left\{exp\left(\frac{q\psi_s}{kT}\right)-\left(\frac{q\psi_s}{kT}\right)-1\right\}}} \qquad (3)$$

The interface-state conductance (G_{PIT}) is extracted from the measured impedance. In the conductance method, the interface state density is directly linked to G_{PIT} by

$$\frac{G_{PIT}}{\omega} = e^2 SD_{IT} \int_{-\infty}^{\infty} \frac{\ln(1+(\omega\tau\exp(\eta))^2)}{2\omega\tau\exp(\eta)} \times \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{\eta^2}{2\sigma^2}\right) d\eta \qquad (4)$$

where ω is the angular frequency. The interface state density D_{it}, the time constant of the interface states τ, and the standard deviation, σ are determined by fitting experimental results with this equation. The capture cross-section (σ_C) is given by

$$\sigma_C = \frac{1}{\tau V_{th} N_C} exp\left(\frac{E_C-E_T}{kT}\right) \qquad (5)$$

where V_{th} (1.8×10^7 cm/s) is the thermal velocity of electrons, and NC ($1.8 \times 10^{19}cm^{-3}$) is the effective density of states in the conduction band.

III. RESULT AND DISCUSSION

The data in Fig. 1 show the parallel mode conductance (G_p) measured at room temperature at a different frequency for Sample 1 (top) and Sample 2 (bottom). Sample 2 has higher G_p peak compare to Sample 1. The existence of interface state can be observed at 1-2 V as the peak conductance.

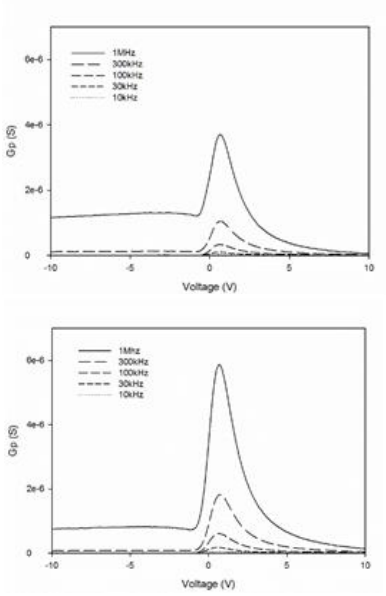

Fig. 1. Conductance-voltage (G-V) characteristics of a SiC MOS capacitor (n-type) measured at various frequencies for sample 1 (top) and sample 2 (bottom).

The data in Fig. 2 show the interface-state conductance (G_{PIT}) at a different energy level for sample 1 and sample 2. Two distinct peaks were observed for sample 1 at high frequency (>5 MHz) and remained plateau until measurable frequency. The interface-state conductance, G_{PIT} for both sample 1 and 2 are almost zero below 5 MHz indicate the generation of fast interface states are dominant in these two samples. For sample 2, the same type of fast interface states peaks was observed at 6 MHz. In contrast to sample 1, the G_{PIT} peaks for sample 2 significantly decreased when the frequency approaches 10 MHz. The G_{PIT} of both samples at the same energy level near conductance band egde (E_C-E_F= 0.2 and 0.3 eV) are shown for comparison as in Fig. 3.

Apparently, there is no peak of slow interface states were observed for both samples and the G_{PIT} value for sample 2 is almost zero below 5 MHz. For each sample, main conductance peaks are observed at frequency >5 MHz, which originate from relatively fast interface states. The peaks for fast interface states are in good agreement with previous reports on SiC MOS capacitors [12][13].

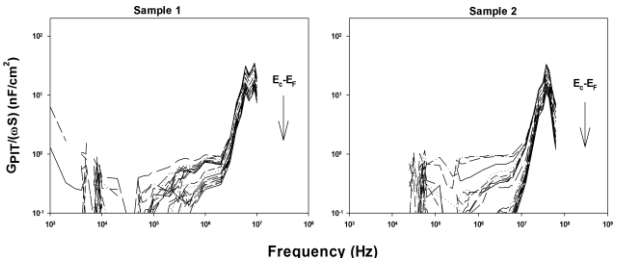

Fig. 2. Interface-state conductance (G_{PIT}) standardized by angular frequency (ω) and area (S) at a various energy level for Samples 1 and Sample 2.

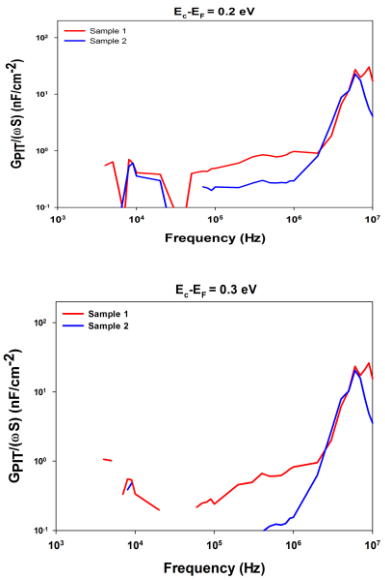

Fig. 3. Interface-state conductance (G_{PIT}) standardized by angular frequency (ω) and area (S) at E_C-E_F= 0.2 and 0.3 eV for Samples 1 and Sample 2.

To expose the full conductance behavior produced by the fast interface states, sufficiently high-frequency measurements need to be performed. Alternatively, the conductance measurement can be executed at low temperature because the interface trap time constant will become slow and measurable at low temperature environments [13].

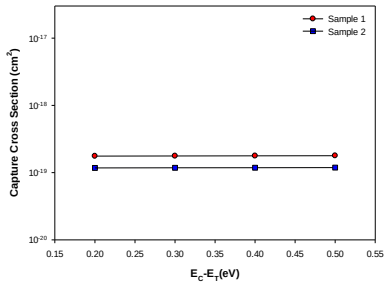

Fig. 4. Capture cross-sections of peaks obtained by the conductance method for Sample 1 and Sample 2.

The data in Fig. 4 represents the capture cross-sections (σ_C) of interface states for sample 1 and 2 that were extracted from the interface state conductance. The magnitude of capture cross-section can anticipate the charge state of interface states. For example, donor-type states change from positive to neutral in the charge state by capturing electrons and have a large capture cross-section. In contrast, the ccceptor-type states change from neutral to negative by capturing electrons and have a smaller capture cross-section. As can be seen in Fig. 4, interface states of sample 1 and 2 exhibit small cross-section in the range of 10^{-19} to 10^{-18}, which is comparable to previous reports [12][14] and most likely are acceptor type states. Sample 2 has slightly smaller capture cross-section, but the difference was very small. Yoshioka et. al, reported that interface state of samples that have gone through annealing process (nitridation) lower than about 1200°C will have much smaller capture cross-section (10-17) compared to samples that were annealed at 1350°C (capture cross-section is about 10-12) [12]. This was confirmed by investigating N atom concentration by secondary ion mass spectroscopy (SIMS) at the SiO_2/SiC, where samples that were annealed at 1150°C only have half of N concentration of samples that were annealed at 1350°C due to small diffusion coefficient of nitrogen into SiC.

The response of fast interface states requires a complex measurement. Due to that reason, the conventional method sucha as high-low and conductance method (in frequency range of 0.1 to 1 MHz) are not able to detect fast interface states. Although 100 MHz equipment can only detect part of peak that comes from fast interface state although at relatively deep energy levels. Thus, it is hard to extract the interface state density accurately using the conventional method. Nevertheless, H. Yoshioka et al. have developed a method that can detect all type of interface state from the difference between quasi-static and theoretical capacitance without utilizing high-frequency measurements.

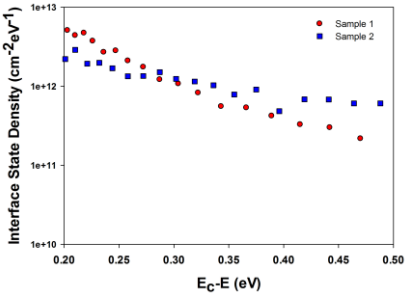

Fig. 5 The distribution of D_{it} verses energy near the conduction band, extracted using the C-ψ_s technique for both samples at room temperature.

The data in Fig. 5 show the distribution of D_{it} extracted using the C-ψ_s technique at room temperature from the data of quasi-static C-V measurements for both samples [11]. The voltage was measured from positive (the depletion region) to negative (the accumulation region) with a rate of 0.1V/s. The data show the variation of D_{it} with energy and the values of D_{it} at E_C-0.2eV (near conduction band) are approximately equal at 2×10^{13} cm^{2}eV^{-1} for both samples.

In comparison to previous data on the phosphorous doped oxides, this value is high because the C-ψ_s technique can precisely determine the density of interface state including the fast states. Near conduction band where E_C-E= 0.2 to 0.28, the D_{it} of sample 2 (phosphorous incorporated) is lower compared to sample 1 but at E_C-E > 0.3, the D_{it} of sample 1 crossover sample 2 and reduces significantly. This is likely because of the D_{it} reduction in phosphorous incorporated oxide is not significant for Si-face 4H SiC substrate and the concentration of phosphorous incorporated into the oxide is inadequate to form PSG in these samples [9]. Nevertheless, the results are in agreement with the previously published reports [9][10].

IV. CONCLUSION

The SiO_2/SiC interfaces incorporated with low concentration of phosphorous were investigated by C-ψ_s and conductance method that is suitable for the detection of all type interface states. The inclusion of low level phosphorous has a vague impact to the capture cross-section but we have shown that the fast states interfaces that are generated by nitridation at high frequency (>5 MHz) can be significantly reduced by incorporating phosphorous at the SiO_2/SiC interfaces. This is maybe the reason for high channel mobility in phosphorous passivated MOSFETs.

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