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Implementation of Low Power Carry Skip Adder using Reversible Logic

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Abstract: ***Addition is a vital arithmetic operation. It is the base of commonly used arithmetic operations such as division, subtraction, and multiplication. Adder is a digital circuit that accomplishes addition of numbers. The one bit full adder is the basic block of an arithmetic unit. There are several adder designs implemented so far to reduce the power. However, each design suffers from exact drawback. Reversible logic is the growing technology in the current era. The numbers of input and output lines in reversible logic are equal. In reversible logic the inputs are to be recovered from the outputs. Reversible logic gates are defined by the user. In this paper Carry Skip Adder (CSKA) is implemented in two different designs i.e. design-I and design-II. Design-I is implemented using Peres gates with irreversible (XOR, AND, OR) logic gates. Design-II is implemented using PERES, TOFFOLI, and FREDKIN reversible logic gates. Design-I and design-II designs are synthesized and simulated by Mentor Graphics tool. Design-II is more efficient in terms of transistor count and power consumption compared to Design-I.***

Keywords— Reversible Logic Gates, Carry Skip Adder, Power Consumption.

I. INTRODUCTION

Adders are one of the important blocks of the digital applications. These are the basic building modules of the arithmetic circuits. Number of transistors is the main concern in digital designs as it affects the area and power. Irreversible and reversible logics gates are used for the design of digital circuits.

The half and full adder are the basic adders. Generally these circuits are implemented using CMOS logic, it has an important characteristic i.e., high noise immunity but there is a significant increase in the power consumption due to the increasing speed and complexity of the circuits. Irreversible logic function describes a single valued function on n discrete inputs, example b = f (a1, a2… an).

The disadvantages of irreversible logic are input cannot implement from the output however in reversible logic input can be getting from the output. Additional circuitry is required in conventional logic gates, to acquire the input from the output. Reversible logic is becoming prominent technology for low power applications. Reversible logic gate can produce exclusive input vector from each output vector, and vice versa.

It has one to one communication between the output and input vectors. The traditional NOT gate is the only reversible gate

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II. LITERATURE SURVEY

Isha Sahu, and Poorvi K. Joshi et.al, implemented reversible 4*4 CSKA using Peres, Toffoli and Fredkin gates. Basically the design used Peres gate. The transistor implementation of Peres gate uses 10 transistors and this full adder block consists of 20 transistors [1].

Isha Sahu and Poorvi Joshi implemented four bit CSKA block using reversible logic gates Peres gates, Toffoli gates and Fredkin gate with smallest possible number of transistors. The design consists of 12 gates, 12 garbage outputs and 81 transistors [2].

Bharathi Panneerselvam, Harshitha Venkatesan et.al, implemented high speed and low complexity CSKA using reversible gates. The speed improvement is attained by using concatenation. For skip logic, AOI and OAI compound gates used instead of multiplexer logic. The structure recognised with both variable and fixed stage size styles, of the adder. The carry skip adder implemented using reversible logic with Toffoli gate, which shrinks the garbage output and increases the speed compared with conventional structure [3].

Gowthami P, and R.V.S.Satyanarayana implemented RCA using reversible logic gates. Basically the design used HNG and Peres gate. Eight Peres gates are used for the design of four bit RCA and also four bit RCA designed with four HNG gates. Four bit ripple carry adder with HNG gate design achieved less gate count, garbage output and quantum cost [4]. Praveena Murugesan implemented Carry Skip BCD Adder and CSKA using reversible logic.

The CSKA implemented using the modified TSG (MTSG) for parallel addition. The Carry Skip BCD Adder implemented using the MTSG for 4 bit parallel addition and the carry skip logic module consists of one FREDKIN and 3 PERES gate's [5].

In this paper, proposed work aims at implementing the Carry Skip Adder in two ways using different combinations of reversible logic gates. In design-I, Carry Skip Adder is designing using PERES gates and some conventional gates. In design-II, CSKA is designing using PERES, TOFFOLI and FREDKIN gates.

III. PROPOSED WORK

A Design-I: Implementation of CSKA by Full Adders with PERES Reversible Logic Gates and Some Conventional Gates

The block diagram of CSKA using full adders with PERES gates and some irreversible gates is shown in figure 1. It consists of four full adders, four EX-OR gates, one four input AND gate, one two input AND gate, and one two input OR gate. The four full adders are designed using PERES gates.

PERES Gate

The block diagram of PERES gate is shown in figure 2. The 3*3 PERES reversible logic gate inputs (A, B, C) mapping to outputs (P=A, Q=A $\oplus$B, R= (A.B) $\oplus$ C). The schematic diagram of Peres gate is shown in figure 3. Each PERES gate requires 10 transistors.

Full Adder using PERES Gates

The block diagram of full adder using two PERES gates is shown in figure 4. Full adder using PERES gates requires 20 transistors. The 3 inputs of 1st Peres gate used for inputs A & B and 3rd input is connected to ground.

The 1st output of PERES gate is a garbage output and the 2nd and 3rd outputs are connected to the 1st and 3rd inputs of 2nd PERES gate, 2nd input of 2nd PERES gate connected to C_{in}. The 1st output of 2nd PERES gate is a garbage output. The sum and carry are taken from 2nd and 3rd outputs of the 2nd PERES gate.

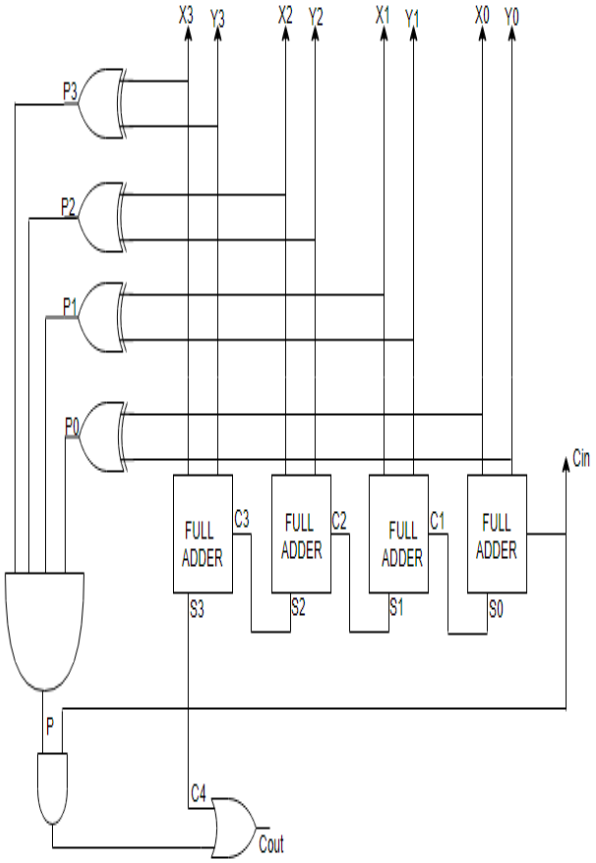

Figure 1: Block Diagram of CSKA by Full Adders with PERES Gates and Some Conventional Gates

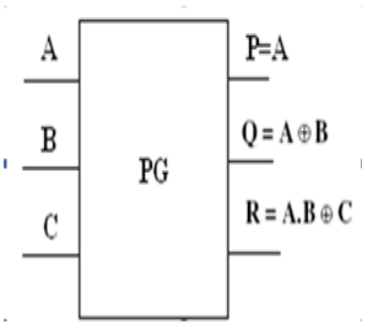

Figure 2: PERES Gate

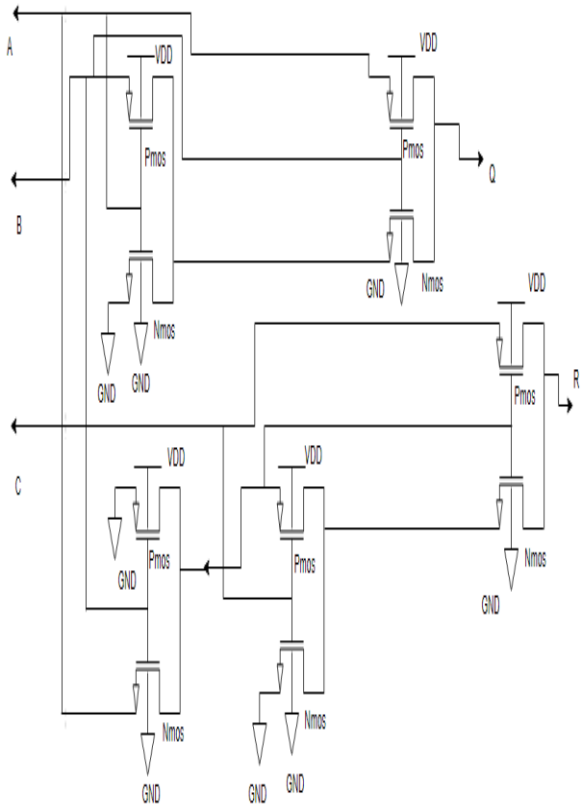

Figure 3: PERES Gate

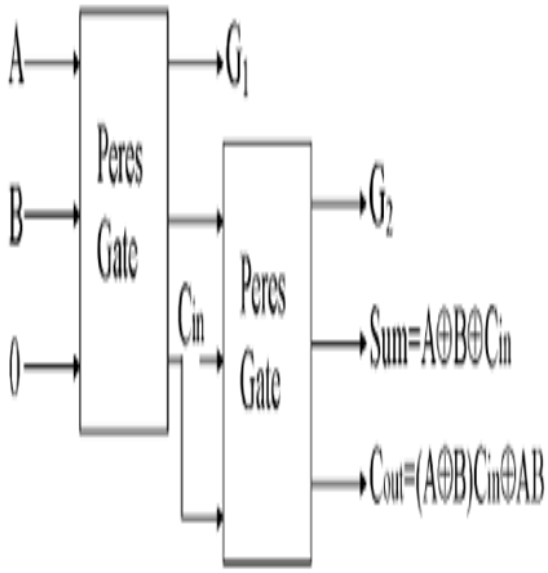

Figure 4: Full Adder using Two PERES Gates

Two Input XOR, Two Input AND, Four Input AND, and Two Input OR Gates

The schematic diagram of 2-input XOR, two input AND, 4-input AND, and two input OR gates are shown in figures 5 to 8 respectively. Each 2-input XOR, two input AND, four input AND, and two input OR gates requires 12, 6, 10, and 6 transistors respectively.

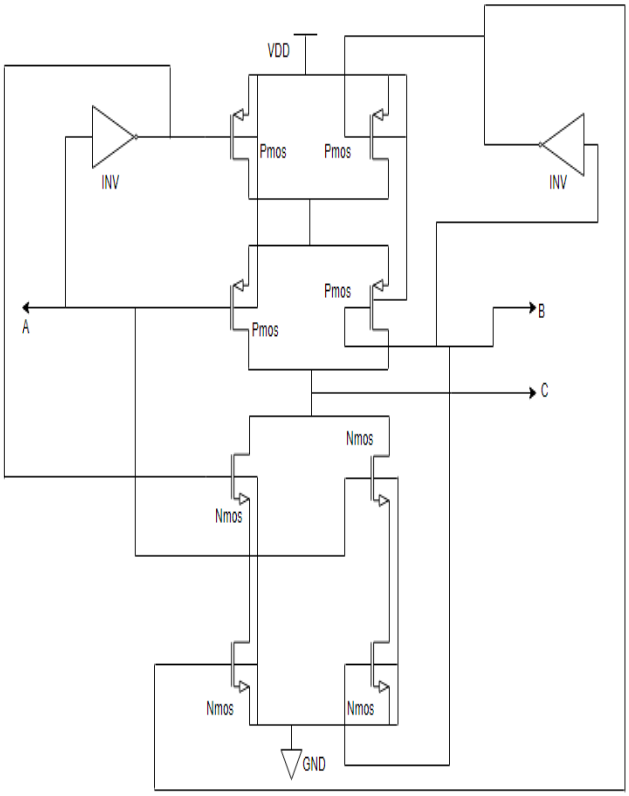

Figure 5: 2-Input XOR Gate

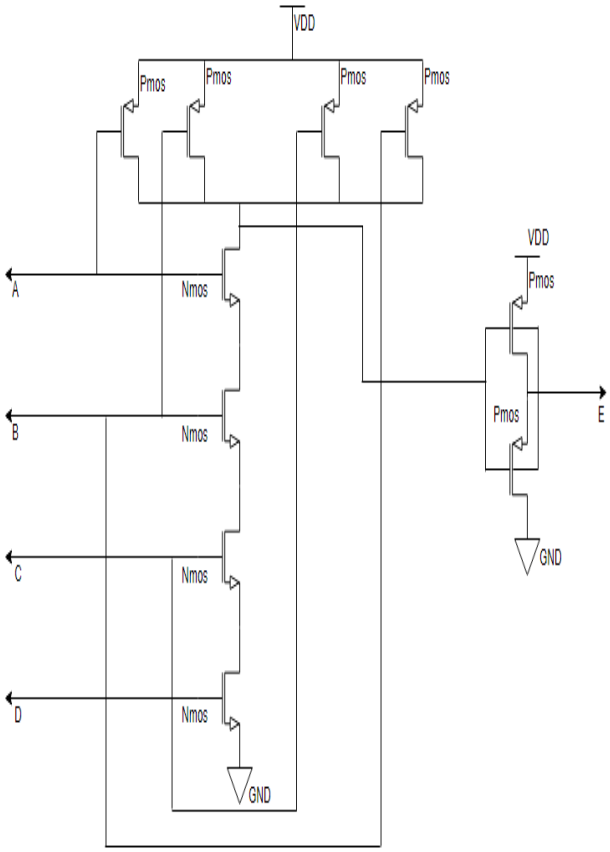

Figure 7: 4-Input AND Gate

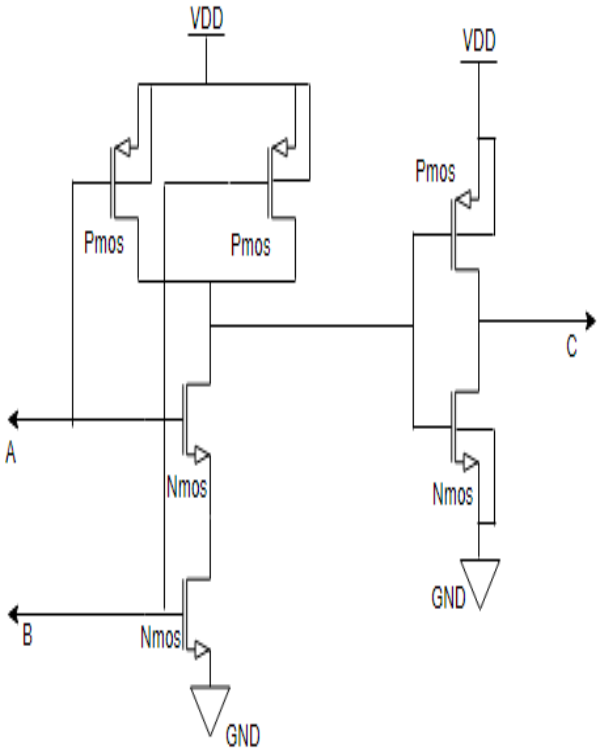

Figure 6: 2-Input AND Gate

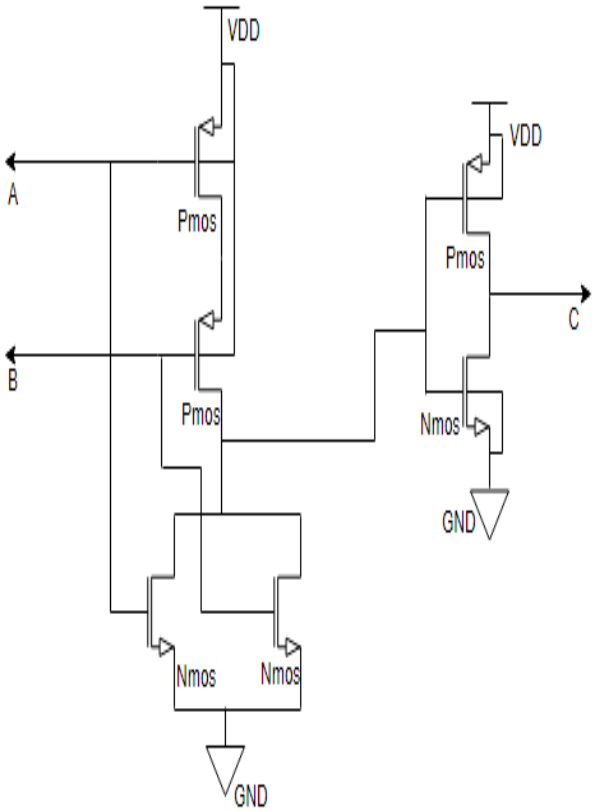

Figure 8: Two Input OR Gate

B. Design-II: Implementation of CSKA using PERES, TOFFOLI and FREDKIN Reversible Logic Gates

The block diagram of CSKA using PERES, TOFFOLI and FREDKIN gates is shown in figure 9. It consists of eight PERES, three TOFFOLI, and one FREDKIN reversible logic gates. The eight PERES gates form the four full adders required to generate the sum and propagate signals. For AND operation 3 TOFFOLI gates are needed. Which are used to generate propagate P signal. FREDKIN gate is used to generate C_{out}.

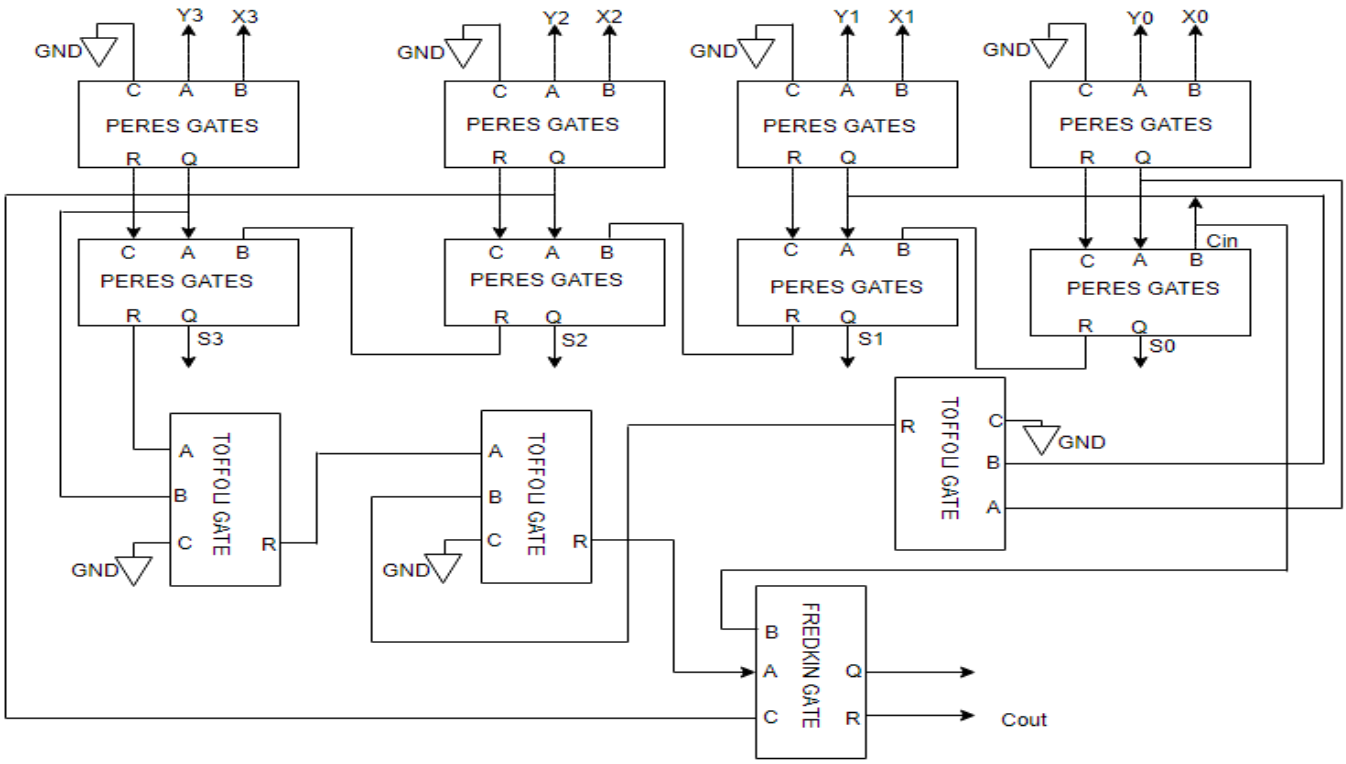

Figure 9: CSKA using PERES, TOFFOLI, and FREDKIN Reversible Logic Gates

TOFFOLI Gate

The block diagram of TOFFOLI gate is shown in figure 10. The 3*3 Toffoli gate inputs (A, B, C) mapping to outputs (P=A, Q=B, R = (A.B) $\oplus$ C). The schematic diagram of Toffoli gate is shown in figure 11. Each Toffoli gate requires 3 transistors.

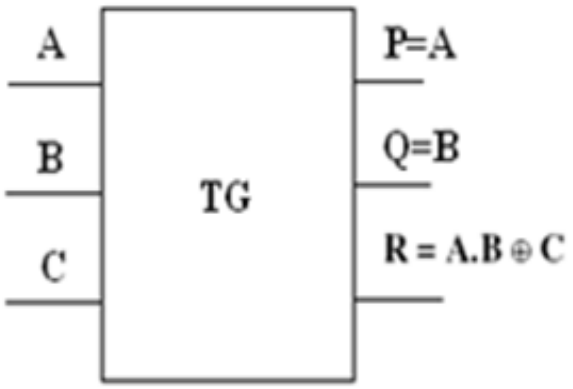

Figure 10: Toffoli Gate

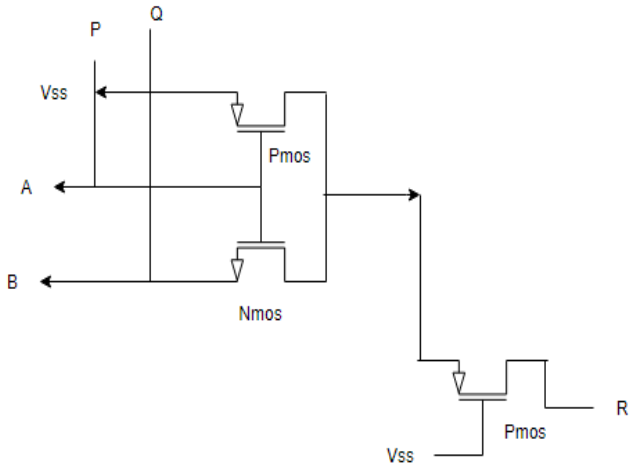

Figure 11: Toffoli Gate

FREDKIN Gate

The block diagram of FREDKIN reversible logic gate is shown in figure 12. The 3*3 FREDKIN gate inputs (A, B, C) mapping to outputs (P=A, Q=A'B+AC, R=AB+A'C). The schematic diagram of FREDKIN gate is shown in figure 13. Each FREDKIN gate requires 6 transistors.

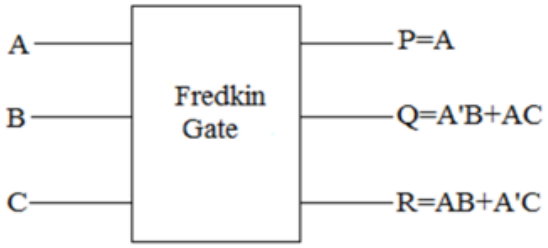

Figure 12: FREDKIN Gate

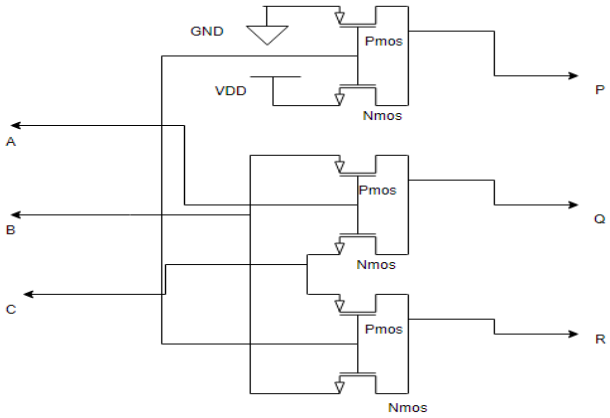

Figure 13: FREDKIN Gate

IV. RESULTS

The schematic diagrams of 2-input XOR, two input AND, four input AND, and two input OR irreversible gates are shown in figures 14 to 17 respectively. The schematic diagram and symbol of PERES, TOFFOLI, FREDKIN reversible logic gates, full adder using PERES gates, Carry Skip Adder using full adders with PERES gates & some irreversible gates, and CSKA using PERES, TOFFOLI& FREDKIN reversible logic gates are shown in figures 18 to 27 respectively using Mentor Graphics.

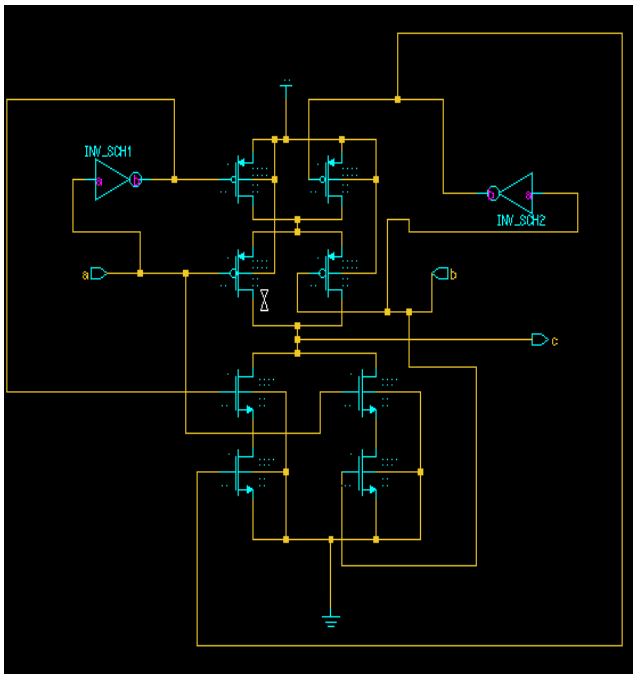

Figure 14: XOR Gate

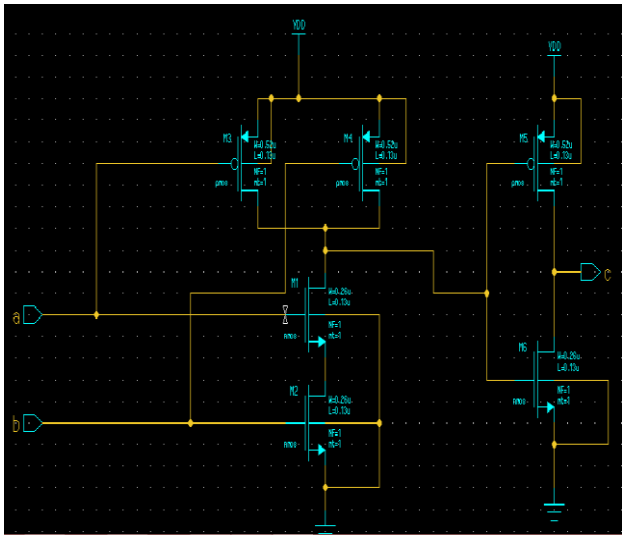

Figure 15: Two Input AND Gate

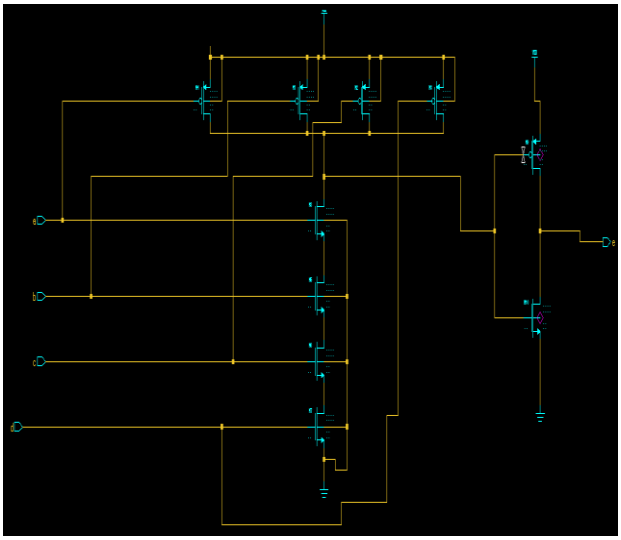

Figure 16: 4-Input AND Gate

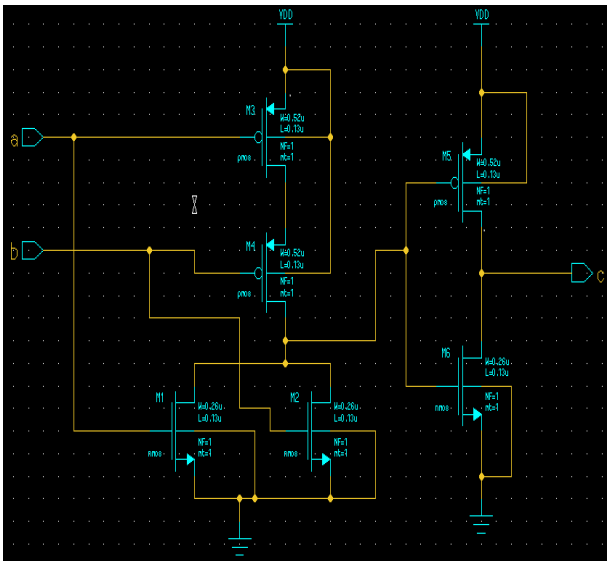

Figure 17: OR Gate

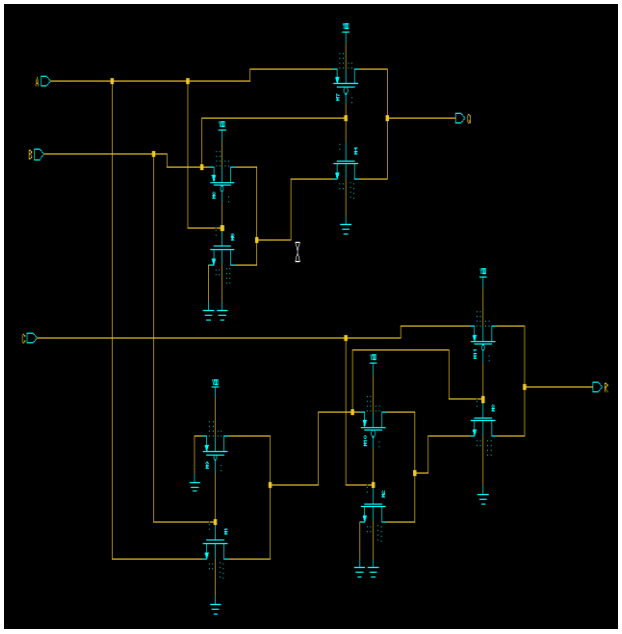

Figure 18: PERES Gate

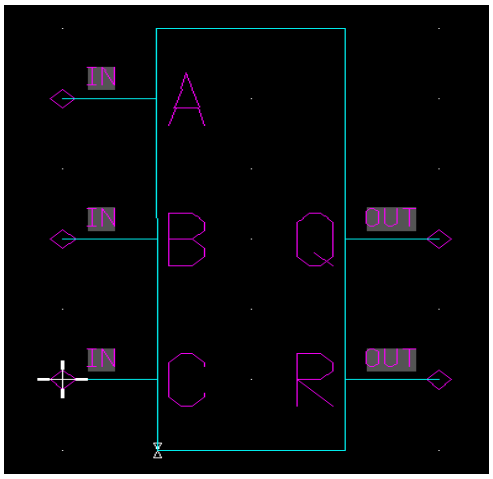

Figure 19: Symbol of PERES Gate

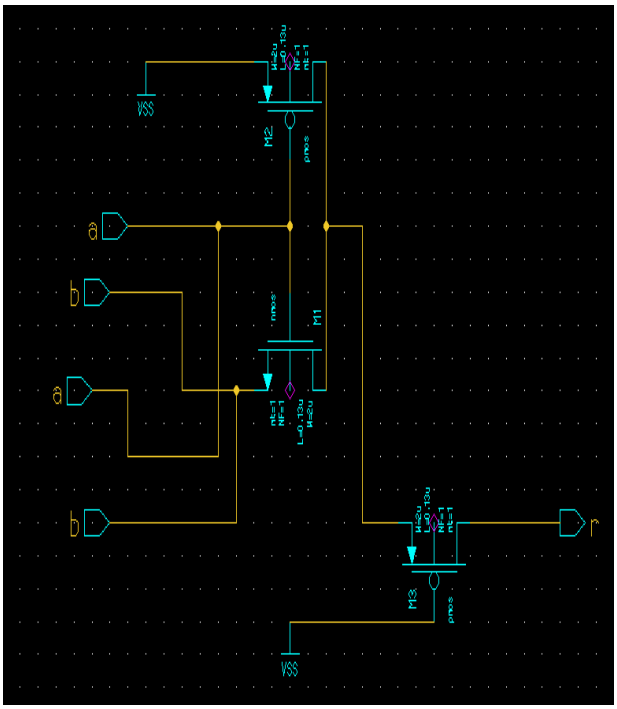

Figure 20: TOFFOLI Gate

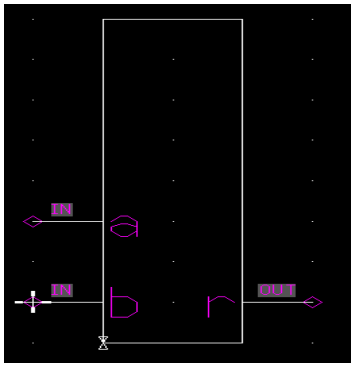

Figure 21: Symbol of TOFFOLI Gate

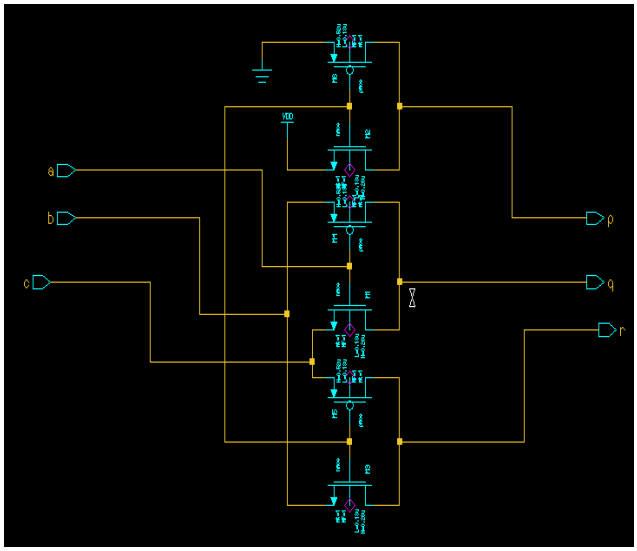

Figure 22: FREDKIN Gate

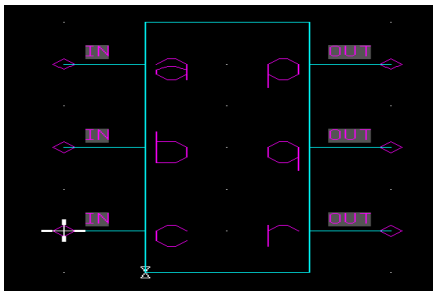

Figure 23: FREDKIN Gate

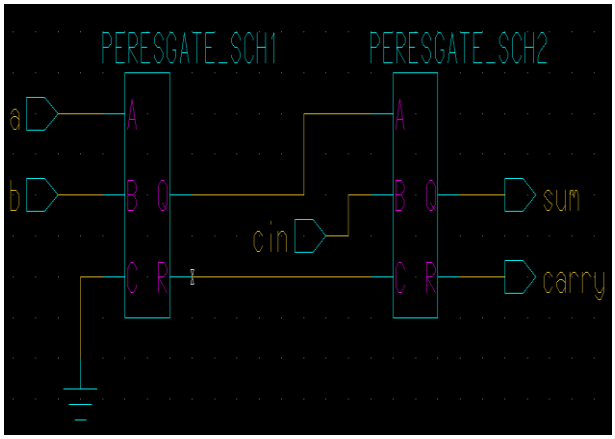

Figure 24: Full Adder using PERES Gates

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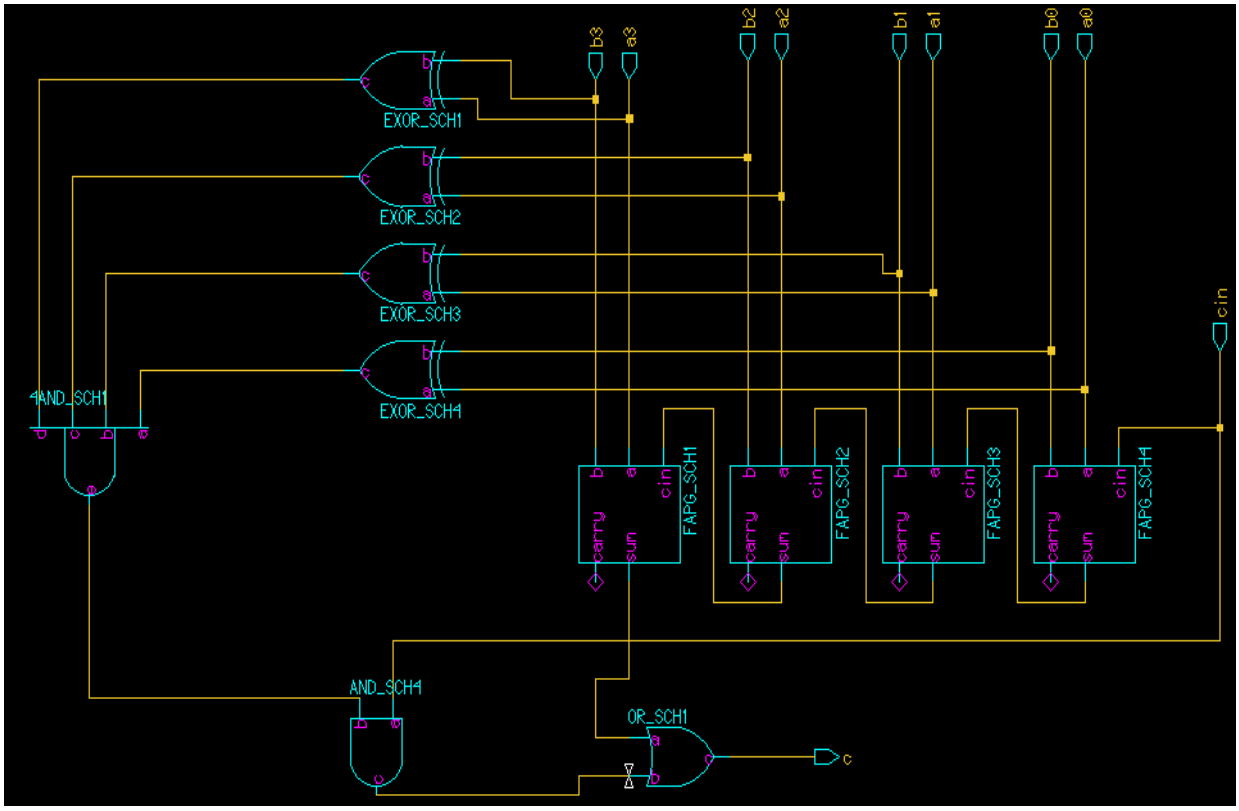

Figure 25: CSKA using Full Adders

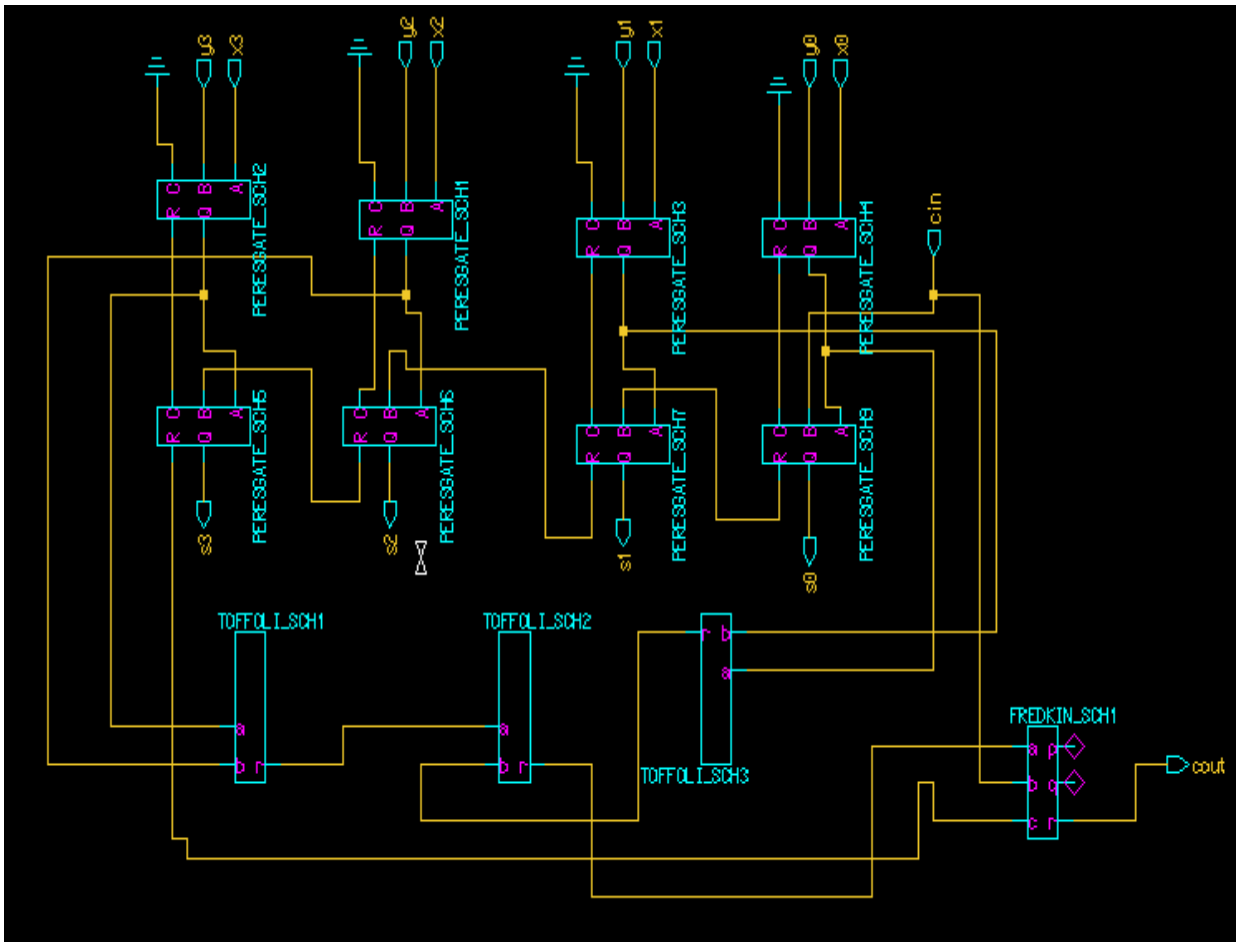

Figure 26: CSKA using PERES, TOFFOLI and FREDKIN Gates

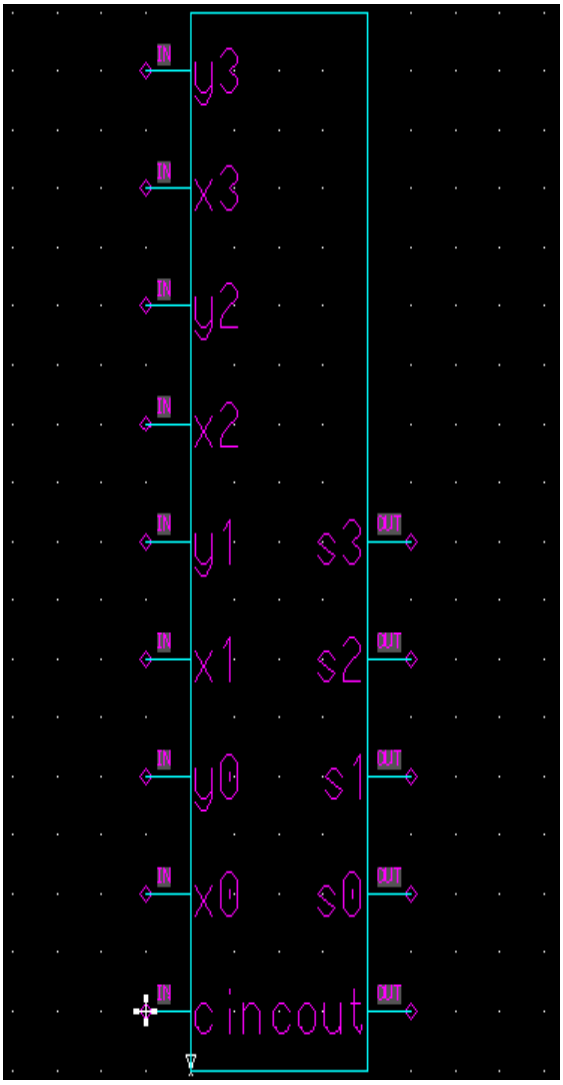

Figure 27: Symbol of CSKA using FREDKIN, PERES, and TOFFOLI Gates

The transistors count and power consumption of design-I and design-II of CSKA is shown in tables 1.

Table 1: Transistors Count and Power Consumption of Design-I and Design-II of Carry Skip Adder

Carry Skip Adder	Transistors Count	Power Consumption (P Watts)
Design-I	150	19.99
Design-II	95	11.06

V. CONCLUSION

In this work two 4-bit CSKA designs, design-I and design-II are implemented using full adders with PERES reversible logic & some conventional gates and PERES, TOFFOLI and FREDKIN reversible logic gates respectively, using Mentor Graphics tool. Among these two CSKA designs, design-II is the best because power consumption and transistors count reduced by 44.67 % and 36.67% respectively.

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Addanki Purna Ramesh has more than 21 years of teaching and research experience. He obtained his Master's degree from JNTU, Hyderabad and Ph.D. from JNTUK, Kakinada. He is presently working as professor of Electronics and Communication Engineering at Vishnu Institute of Technology, Bhimavaram. He is a member of ACEEE, Fellow of Institution of Electronics and Communication Engineers (IETE), Fellow of Institute of Engineers (India). His areas of interest are VLSI, DIP, and Embedded Systems. He has 29 publications in international journals and 2 in international conferences.