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Analytical Modeling of Adiabatic Logic with the Effects and Analysis of Performance Parameter Variations

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Abstract*: *Adiabatic or energy recovery circuits are based on recycling the energy stored in nodal capacitances. For a given amount of energy stored in nodal capacitance, the energy drawn from the source depends on the rate of drawing the charge from the source. Power drawn from the source will be lower if the rate of charging is lower. The efficiency of charging of adiabatic circuits depends on how slowly the capacitance is being charged. We have presented one analytical model of adiabatic logic circuit and find out the expressions for power dissipations in charging and discharging phases. From the expression conclusions on design parameters are made. We have also examined the power dissipation of the adiabatic circuits with the variation of some device parameters like width of the transistors, load capacitance, power clock frequency and input data frequency.

Keywords* : *Adiabatic, CMOS, PMOS, NMOS, charge, power clock

I. INTRODUCTION

With increased scaling in CMOS technology, today's designs are capable of performing very high speed computations as the complexity and number of devices on a given IC is no longer an issue. Much of the research efforts in the recent decades have been dedicated to improving the speed of digital systems. Thus, high speed computation has become an expected norm for average users. Along with this, there is a growing desire to have access to computation at any location without being limited to a given space with a wired network. This requirement for portability of the computational device places restrictions on the size, weight and power.

Conventional CMOS logic circuit design approaches rely on charging the output capacitive nodes to the power supply V_{dd} or discharging it to ground. This design approach has been widely used. For Low power applications, although there are many techniques both at circuit level and system level, a very fundamental source of energy dissipation is the discharge of the capacitor to ground. Every time capacitor is discharged to ground, an amount of energy = $1/2CV^2$stored in the capacitor is lost.

This loss of energy can be prevented if instead of discharging the capacitor to ground, the charge or energy stored can be recycled. Another way of reducing the power consumption is to design the circuit in such a way that the charging of the capacitive node takes place very slowly. Here in this scope, we have prepared an analytical model for adiabatic charging and discharging. The expressions for charging and discharging in an adiabatic circuit have been established. From the established expressions, we have suggested suitable low power adiabatic system design requirements. One glitch free adiabatic inverter is also presented here to examine the variations of power dissipation in adiabatic circuits with the device parameter variations. Depending on the simulation results, some conclusions are made on the design issues of adiabatic inviters.

II. CHARGING OF ADIABATIC CIRCUITS

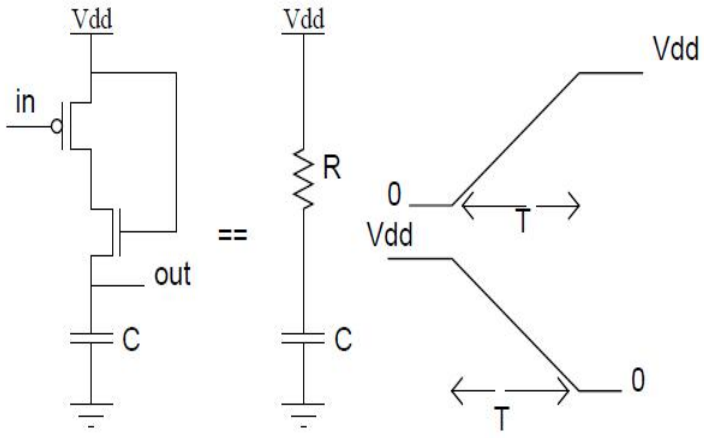

Figure 1. Model of adiabatic logic circuit

The charging and discharging pattern of the adiabatic inverter and the variation of the waveform with different parameters is further investigated by considering the charging and discharging branches as composed of resistors when the corresponding branch is active. Assuming that the combination of PMOS and NMOS in series acts as a resistor of value R when both the transistors are ON, it can be seen that both the charging and discharging branch present the same resistance path. Although the transistors are not completely ON for the whole charging or discharging process, we assume this to simply our analysis.

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During charging, when the input is low(logic0), the MOSFET M1 is ON and as V_{ck} increases from 0 to V_{dd}, the capacitor is charged through the transistor M3. The clock voltage reaches its peak value V_{dd} in a time T. the equation for clock waveform can be written as

$$V_{ck}(t) – V_{dd}.t/T \text{ ----------(1)}$$

The clock reaches a value V_{th} the threshold voltage of the MOSFET M3 at time T_{th}. The voltage V_c across the load capacitor C after T_{th} is given by

$$\frac{V_{dd}t}{T} = RC.\frac{dVc}{dt} + Vc \text{ ---------- (2)}$$

$$\frac{dVc}{dt} + \frac{1}{RC}.Vc = \frac{1}{RC}\left(\frac{Vddt}{T}\right) \text{ ---------- (3)}$$

The solution becomes

$$\mathrm{Vc(t)}e^{\frac{t}{Rc}} = \frac{1}{RC}\frac{Vdd}{T}\int te^{\frac{t}{RC}}\,dt + V_0 \text{ ---------- (4)}$$

$$Vc(\mathrm{t}) = \mathrm{e}^{\frac{-t}{Rc}}\left(\frac{1}{RC}\frac{Vdd}{T}RC.e^{\frac{t}{RC}}(t-RC) + V_0\right. \text{ ---- (5)}$$

Equation (5) can be written as

$$Vc(t) = \frac{Vdd}{T}(t-RC) + V0e^{\frac{-t}{RC}} \text{ ---------- (6)}$$

Now, current can be calculated as

$$i_c(t) = C\frac{Vdd}{T} - \frac{V0}{\mathrm{R}}e^{\frac{-t}{RC}} \text{ ----------(7)}$$

$$Echarging = \int Vclk(t)\left(\frac{Vclk(t)-Vc}{R}\right)dt \text{-------- (8)}$$

$$\frac{1}{R}\int V\,2\mathrm{clk(t)} - \frac{1}{\mathrm{R}}\int \mathrm{Vclk(t)Vcdt}$$

First term will be $\frac{1}{R}\int\left(\frac{Vdd}{T}\right)t2 = \frac{V2dd}{RT}\frac{t3}{3}$ ---------- (9)

Second term will be

$$\frac{1}{R}\int\left(\frac{Vddt}{T}\right)\left(\frac{Vdd}{T}(t-RC) + V0\,te^{\frac{-t}{RC}}\right)\mathrm{dt} \text{------ (10)}$$

$$= \frac{1}{R}\left(\frac{Vdd}{T}\right)2\frac{t3}{3} - \frac{C\frac{V2dd}{T_2}t2}{2} - \frac{VddV0}{T}Ce^{\frac{-t}{RC}}(t+RC)$$

So the complete expression for $E_{CHARGING}$ is

$$= \frac{1}{R}\left(\frac{Vdd}{T}\right)2\frac{2t3}{3} - C\frac{V2ddt}{T2}\frac{t2}{2} - \frac{VddV0}{T}Ce^{\frac{-t}{RC}}(t+RC)$$

------- (11)

III. DISCHARGING OF ADIABATIC CIRCUITS

The equation of clock voltage during discharge is

$$Vclk(t) = \frac{-Vdd}{T}t + \mathrm{Vdd} \text{----------(12)}$$

$$Vclk(t) = Vdd\left(1-\frac{t}{T}\right) \text{----------(13)}$$

When the input is logical '1', the transistor M is ON and when the clock voltage $Vclk(t)$ is falling, the load capacitor discharges through M4 and M2. The differential equation in this case is

$$\frac{dVc}{\mathrm{dt}} + \frac{1}{RC}Vc = \frac{1}{RC}Vdd\left(1-\frac{t}{T}\right) \text{---------(14)}$$

The voltage across the capacitor is

$$Vc(t)e^{\frac{t}{RC}} = \int\frac{1}{\mathrm{RC}}\mathrm{Vdd}\left(1-\frac{\mathrm{t}}{\mathrm{T}}\right)e^{\frac{t}{RC}} + \mathrm{V1}$$

$$= \frac{Vdd}{RC}\int\left(1-\frac{\mathrm{t}}{\mathrm{T}}\right)e^{\frac{t}{RC}} + \mathrm{V1} \text{ ----------(15)}$$

$$Vc(t) = Vdd - \frac{Vdd}{T}(t-RC) + V1e^{\frac{-t}{RC}} \text{-------(16)}$$

$$ic(t) = C\left(-\frac{Vdd}{T} - \frac{V1}{RC}e^{\frac{t}{RC}}\right) \text{----------(17)}$$

Energy consumed in discharge cycle is

$$E_{DISCHARGE} = \int Vclk(t)\left(\frac{Vclk(t)-Vc}{R}\right)dt$$

$$= \frac{1}{R}\int(V2clk(t) - Vclk(t)Vc)dt \text{ ----------(18)}$$

$$\frac{1}{R}\int V2dd\left(1-\frac{t}{T}\right)2\,dt - \frac{1}{R}\int Vclk(t)Vcdt \text{-(17)}$$

first part is

$$= \frac{1}{R}\int V2dd\left(1-\frac{t}{T}\right)2\,dt = -V2\frac{ddT}{3R}\left(1-\frac{t}{R}\right)3$$

---------- (19)

The second part is

$$\frac{1}{R}\int Vclk(t).Vc(t)dt$$

$$= \frac{1}{R}\int\frac{Vcct}{T})Vdd - \frac{Vdd}{T}(t-RC) + V1^{\frac{-t}{RC}})dt$$

$E_{DISCHARGE}$

$$= \frac{V2dd}{R}\left(\frac{t2}{2T} - \frac{T}{3}\left(1-\frac{t}{T}\right)3 - \frac{1}{T2}\left(\frac{t3}{3} - RC\frac{t2}{2}\right) - \frac{1}{R}\frac{Vdd}{T}V1RCe^{\frac{-t}{RC}}(t+RC)$$

----------(20)

IV. GLITCH FREE ADIABATIC CIRCUITS

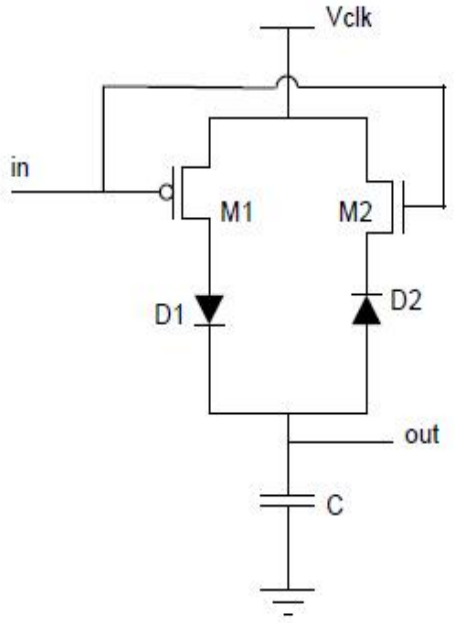

Figure 2. Diode based glitch free CAL inverter

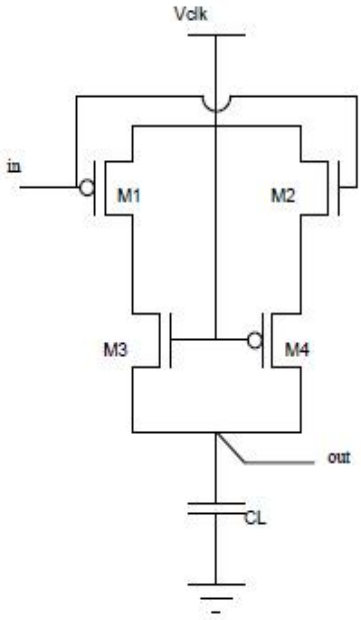

Figure 3. Diode free glitch free CAL inverter

Glitch free inverter circuits are shown in fig. The first one is diode based and the second one is modified and diode less. Transistor M1 and M3 form the charging path and M2 and M4 form the discharging path. For any applied logic either charging or discharging path will be valid. The power supply used here is trapezoidal waveform which varies from 0 and $V_{dd.}$ In case of GFCAL inverter the transistor M1 will on and diode D1 will conduct when clock transits from 0 to Vdd. Thisresults the capacitor to change and an output of high logic is obtained. When M2 transistor is on and M1 is off and diode D2 allows discharging only. That time the clock transits from V_{dd} to 0.

In case of diode free GFCAL the transistors M2 and M4 switch alternatively. These transistors allow either charging or discharging for a given period of time. These switching transistors are controlled by the power clock signal. This power clock signal controls the charging and discharging process. Let us assume output capacitor is initially unchanged and input is in low logic level. For diode free GFCAL, the load capacitor is in uncharged state and input is low. In this case the transistor M1 turns on and when clock goes from 0 to high at some voltage when the power clock voltage exceeds the threshold voltage of M3, this will turns on and the capacitor will begin to charge. Next when transistor M2 will be on but M4 will be off, the clock transits from 0 to Vdd. When clock goes from V_{dd} to 0,M3 turns off and prevents discharging of capacitor. In case of diode free GFCAL, output is high or charged to some initial voltage level and the input voltage is 0,the circuit remains in the same state as before. For input level=low, the transistor M3is on and transistor M3 allows charging operation when power clock goes from 0 to V_{dd}. So the output is in high state. Next ,when M3is on and M3,M4 will allow the discharge of the capacitor when power clock goes from high to low.M1 will be off and no further charging will take place.

V. TRANSISTOR WIDTH VARIATIONS

Increasing the width of transistors allows the circuit to charge or discharge the capacitive nodes faster. This is due to the fact that, a larger width allows more current to pass through the transistors and thus lesser time is required to charge the capacitors to a required voltage level. Although the charging and discharging processes are accelerated, there are other effects of increasing the device width. One effect is that large device dimensions mean that large capacitance of gate-source and drain-source junctions. As seen from the table1 obtained from simulation results. An increase in device width increases the power dissipation of the circuit due o increased current flow through the charging and discharging branches.

Table 1: Variation in power dissipation with transistor width

Width (µm)	Power dissipation (µw)
0.2	1.21
10	2.11
15	2.76
20	2.92

VI. LOAD CAPACITANCE VARIATION

Load capacitance takes time to charge or discharge based on its capacitance values. Large capacitance creates slow charging and discharging. Small capacitance gives very fast discharging times.

Table 2: Variation in power dissipation with load capacitance

Load capacitance (pf)	Power dissipation (µw)
5	2.11
10	2.45
15	4.17
20	6.15

VII. CLOCK FREQUENCY VARIATION

Clock frequency means power clock frequency. Power clock basically responsible for efficient charging of load capacitance. Power dissipation across the transistor depends on how fast the charging or discharging signal is varying. An increase in power clock frequency tends to increase the power dissipation.

Table 3: Variation in power dissipation with clock frequency

Clock Frequency(ns)	Power dissipation (µw)
50	300
100	324
150	335
200	356.7

VIII. INPUT DATA FREQUENCY VARIATION

Input data frequency determines how often the logic switches between high and low levels. This is how it influences power consumption of gate. It can be proved that lower input frequencies give a low power input. The minimum time period of the input signal can be equal to the time period of the power clock. The output voltage levels do not change with input data frequency. The output voltage levels are decided by the power clock voltage levels and threshold voltage of the switching transistors.

Table 4: Variation in power dissipation with clock frequency

data Frequency(ns)	Power dissipation (nw)
1	200
2	212
3	312
4	325
5	412

IX. CONCLUSION

From the analytical model it is clear that the performance parameters are responsible for adiabatic charging and discharging.

For adiabatic charging V_{dd} supply, RC time constant and value of the capacitor are responsible. Charging power is directly proportional to RC time constant, value of capacitor and V_{dd} supply. Therefore proper values of these parameters will reduce the charging power dissipation.

Discharging power dissipation is proportional to RC time constant and square of the power supply $V_{dd.}$

Therefore by taking proper values of power supply Vdd and capacitor will minimize the discharging power dissipation.

From the device parameter analysis such as transistor width, powr clock frequency, input data frequency, it is clear that ,to reduce power dissipation in glitch free inverters the designers have to make a tradeoff between performance and device parameter variations. Increasing transistor width, capacitance value, input data frequency will increase power dissipation. So proper device parameters will have to choose for optimum results.

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