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# Low Cost Hardware Architecture of Fast Lifting Wavelet Transform for Image Compression

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***Abstract:In this work, the researchers have given a low-cost, multiplier-less design with latest DWT (2D lifting technology) for high-speed dual-Z scans. A single dimension parallele row, column processors and five transposing registers are the suggested architecture. Furthermore, a 4N timeline buffer is used to process 2D DWT images with NxN resolution. Flipping architecture is intended to decrease the critical path, replacing multipliers with shifting and adding logic. To reduce transposition and latency buffers, dual Z scanning technology is introduced. The proposed architecture is better for similar performance requirements than the existing hardware architectures. Verilog is defined as the suggested Design Register Transfer Logic (RTL) and is synthesized with Xilinx ISE 14.5. When synthesized with a better hardware efficiency for Xilinx Spartan 6 series field programmable gate array, the suggested architecture works at a frequency of 140.47 MHz.***

***Keywords: Image compression; lifting, pipeline, DWT, filter bank, Dual scan.***

## I. INTRODUCTION

Since the implementation of the JPEG2000 image encoding standard [1], much has been thought of creating effective circuit architectures for a two-dimensional and discrete wavelet transformation (DWT). Traditionally, DWT was performed with filter benches [2], [3]. However, the elevation scheme [4] promises to reduce the amount of DWT calculation operations as a convolutional approach to almost half [5]. The elevation scheme also offers onsite processing which allows low-memory devices to use DWT. The architectural design in [6] is feasible only for wavelet filters that have not been generated by more than two measurements based on a continuous matrix algorithm. In [7], how the use of inefficient hardware and complicated power circuits lead to the RPA DWT 2-D are discussed. Two other 2-D carrier architectures DWT [9], [10] reduce the amount of built-in memory by dividing the image into blocks, but additional calculations are required. A new DWT 2-D design offers biorthogonal reinforcement of the 9/7 wavelet. The architecture seems to have 100 percent hardware usage, a periodic flow of information and few command difficulties. Additional measurements and concentrations are easily adjustable. The elevation scheme is used to extend images symmetrically without further calculations or clock cycles. Our architecture has small requirements for integrated memory without blocking the image. The basic architecture has been described in [11], which shows how our design is applied in a programmable port matrix.

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## II. RELATED WORK

Grangetto et al. [12] and Martina et al. [13] suggested an integer wavelet transform (IWT) algorithm to be optimized and implemented. It proposed the selection of optimum factorizations of the polyphase wavelet filter matrix will be used in lifting system. The effect of the finite word length on the wavelet coefficients was discussed, so that a small number of bits of the given image coefficients are kept for mantissa to reduce the degradation of performance. The IWT-based VLSI architecture can achieve higher frame rates with moderate gate complexity.

Dillen et al. [14] suggested a line-based architecture for the JPEG2000 5/3 and 9/7 Wavelet transform. The lifting wavelet is used to realize a fast transform wavelet. Two lines are processed, allowing Requirement for minimum memory and fast calculation. The proposed architecture allows the computation of images continuously to be processed for several decomposition levels can be achieved through time / space cascading. The pipeline and operational optimization speed while the combination of the two transforms into a single structure helps to save the area.

Liao et al. [15] proposed efficient recursive wavelet transforms for 1-D and 2-D lifting. That's the Traditional DWT architectures calculate the current jth level and (J-1)th level after completion. However, the number of samples to be processed at each level at the previous level in the multiresolution DWT is always half the size. Therefore, multiple processing levels can be decomposed simultaneously. The recursive and dual 1-D and 2-D DWT scanning architectures based on lifting scheme is suggested. The 1-D recursive architectures exploit interdependencies between the wavelet coefficients by alternating use of the same data path for clock cycles. It uses common function blocks to process two separate data streams. Dual scanning architectures 2-D simultaneously transform column and row and process the required amount and the buffer size is reduced. The calculation in higher decomposition levels is initiated as soon as the sufficient intermediate data is low the subband frequency is available for computation.

Huang et al. [16] proposed a tilting framework to decrease critical path and minimize DWT carrying storage demands. Latency in lifting based architectures is to the time gaps from the entry node to the calculation node in each computation section, which can be accomplished by reducing the multipliers from the entry node to the route node. This can be accomplished by turning the inverse coefficient of each calculation node. DWT lifting system's critical path is decreased and the decrease speed rises as the amount of serially linked machine devices rises.

Chen [17] proposed the 1-D Multilevel lifting based wavelet transformation implementation of VLSI. The lifting scheme was developed as a flexible tool for building bi-orthogonal wavelets. The architecture folds all resolution calculations into the same low-pass and high-pass units to obtain greater hardware usage owing to its modular, regular and flexible structure. The architecture has a similar topology to a scan chain; it can be changed by adding additional hardware resources to a testable scan chain.

Jung et al. [18] presented an efficient line based VLSI 2-D lifting DWT architecture. The architecture calculates lifting feature based on state space representation and utilizes RPA. To enhance hardware use, the filter responsible for first-level column activities perform second-level and subsequent row and column operations. This improves hardware use of architecture. Periodic symmetric expansion is used to analyze boundary image coefficients.

Barua et al. [19] suggested a scalable architecture for multiple lifting steps. The architecture is steady flow of data and control less complexity, attaining 100% hardware use. The symmetrical expansion is the minimum amount of clock cycles. The architecture is more efficient and uses less inbuilt memory than convolutionary filter banks.

Xiong et al. [20] utilizes the integrated decimation method to optimize the 1-D Lifting DWT architecture intended to obtain input and produce output with the alternately accessible low-and high-frequency parts of initial data. Based on the 1-D DWT architecture, an effective line-based high-speed 2-D DWT architecture is suggested using parallel and pipeline methods, consisting primarily of two horizontal filter modules and a vertical filter module, running in parallel and 100% software use pipeline mode. This is accomplished by exploiting the parallel between the four coefficients of the 2-D DWT lifting scheme. The multipliers are replaced by shift-added operations for a lossless transform of 5/3, as the lifting coefficients are integer power of two.

Angelopoulou et al. [21] suggested implementing and comparing FPGA's 5/3 2-D discrete wavelet transformation schedules. Several calculation schedules based on separate input traversal patterns were suggested for multilevel 2-D DWT execution. For real-time implementations, row column, line and block architectures can be introduced.

Cheng & Parhi [22] suggested a high-speed systemic DWT VLSI application based on hardware-efficient parallel FIR filter constructions. For an image with a controlled increase in hardware costs, it is easy to achieve high-speed 2-D DWT with calculation time as low as N^2/12. This structure can save a large amount of multipliers or storage components, and can also be used to introduce traditionally suitable 2-D DWT designs for lifting or flipping. Parallel FIR buildings are introduced using cyclic convolution property. The non-separable 2-D DWT architectures are suggested by converting the filtering and down sampling column sizes into two FIR filters each with half of the initial FIR filters. The 2-D DWT architectures are shown for 8*8 image coefficients and four filter lengths.

Meher et al. [23] suggested a 2-D DWT, hardware efficient Modular Systolic Like (MSL) design. The general calculation is divided into two distinct steps, where column processing is performed in phase 1 while row processing is performed in phase 2. A fresh information access system and a fresh folding method are used concurrently to calculate both phases for the transposition free application of convolutional 2-D DWT. The proposed method can provide almost the similar throughput rate and requires the less number of adder and multipliers as the best of the existing structures.

Saeed Koko and Agustiawan [24] presented VLSI lifting based 2-D DWT parallel pipeline architectures. For real time applications of 2-D DWT with demanding speed and throughput requirements, two parallel and four parallel VLSI lossless pipeline lifting architectures algorithms 5/3 and loss 9/7 are proposed. The overlapped scan method used to scan the image coefficients in parallel is used to derive pipeline architecture. When calculating the lifting coefficients, the column processor works in parallel with the row processor this is done to reduce the internal memory between the processor row and column.

Lai et al. [25] delivered high performance and efficient memory Pipeline architecture with 2D lifting parallel scanning method DWT for applications JPEG 2000. It consists of two 1-D DWT cores and 2x2 register array for transposition. The 1-D DWT core consumes two data inputs and produces two coefficients for each cycle. The critical path is just unit delay multiplier. The coefficients in the same column are scanned in the row direction and transported to the column processor using a parallel scanning method. The internal buffer size and the requirement for on-chip memory are reduced. The architecture can process 30 frames with 100 MHz HDTV1080p (full HD) images per second.

Shi et al [26] proposed an efficient folded architecture by applying parallel and pipeline techniques to the serial operations of the data flow of the lifting scheme with the parallel operations. The optimized architecture has short critical latency and efficient folding techniques are used to create an efficient architecture. The use of hardware is improved by folding technique and shift-add operations are replaced by multipliers.

An efficient 3-D DWT architecture for the image and video compression algorithm was suggested by Anirban Das et al. [27]. This architecture forms the first 3-D DWT lifting architecture without restrictions on group of images. The novel computing technique based on an analysis of the signal flow minimizes storage requirements. The architecture minimizes the memory, low power consumption and low latency and high performance. The proposed architecture offers a speed of 321MHz for the compression of images in real time with larger frame sizes.

Mohanty et al. [28] proposed 3-D DWT high performance, multilevel and parallel pipeline architecture.

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The 3-D DWT calculation for each decomposition level is divided into three separate stages and all three stages are carried out in parallel by a processing unit consisting of a variety of processing modules.

Salehi and Amirfattahi [29] suggested a 2-D DWT block based framework with unique section scanning techniques. The primary challenge in 2-D DWT design is the quantity of internal memory required to generate wavelet coefficients. The parallelism is needed depending on the size of the input frame. Multipliers are removed and substituted with minimal hardware demands. Ghantous and Bayoumi [30], proposed the VLSI 2-D DWT parallel and pipeline architecture. A zone efficient, parallel and pipeline architecture with a modified image scan coupled $i^{th}$ multiplier-free multiplications is Mohanty & Meher [31] suggested a modular, high-performance, low-latency VLSI memory-efficient architecture for multi-level 2-D DWT. For multi-level 2-D DWT lifting, a modular and pipeline the architecture is discussed without a line buffer and frame buffer. Appropriate partitioning and calculation of each decomposition stage reduces the general product. A cascaded pipeline structure is used to process distinct concentrations to maximize hardware use effectiveness.

Zhang et al. [32] suggested high-speed and reduced-area 2-D DWT architecture. The intermediate outcomes are recombined and stored to decrease the number of pipeline stages to reduce the current method's latency. Two parallel scanning architectures input / output are using three registers as a transposition buffer between filters in row columns, resulting in greater performance.

Mohanty & Meher [33] suggested a memory-efficient architecture for a convolution-based general structure for 3-level 2-D Daubechies and bi-orthogonal DWT calculations. The architecture does not need a structural buffer. The limits of this architecture are that it requires more arithmetic components than lifting structures, which provide significant savings in area and power with smaller memory sizes and time. The DWT level is calculated simultaneously in this architecture to prevent a frame buffer. At each DWT level, parallel data access is used to reduce the complexity of memory.

Masahiro & Hitoshi [34] has presented a non-separable 2-D DWT with an increased number of lifting steps and is compatible with the JPEG 2000 lossless and loss standard Separable 2-D DWT. The non-separable lifting has reduced, reducing the latency suitable for high speed image processing.

## III. LIFTING WAVELET TRANSFORM

The lifting method has been used to reduce the amount of change coefficients and develop wavelets from the second generation. Daubechies and Sweldons [4] proved that another wavelet shift structure can be constructed from any orthogonal and biorthogonal channel using a polyphase frame factorization. So this scheme, known as the lifting scheme, begins with an exceptional arrangement of channels, say (h, g), and the channels are part of even and odd. The polyphase grid, provided by

$$P(z)=\begin{bmatrix} h_{even}(z) & h_{odd}(z) \\ g_{even}(z) & g_{odd}(z) \end{bmatrix} \quad (1)$$

The polyphase matrix is factorized using a consecutive division strategy and can be expressed as Laurent's polynomial.

$$P(z)=\begin{bmatrix} 1 & P1 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ U1 & 1 \end{bmatrix}\begin{bmatrix} 1 & P2 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ U2 & 1 \end{bmatrix}\begin{bmatrix} K & 0 \\ 0 & 1/K \end{bmatrix} \quad (2)$$

Where, K is a constant and the Laurent polynomial

$$P1=\alpha(1+z^{-1})$$

$$U1=\beta(1+z)$$

$$P2=\gamma(1+z^{-1})$$

and $U2=\delta(1+z)$ are the prime and dual lifting stage respectively, here we chosen the filter bank as 9/7. This type of filter pair has the advantage of less area and high performance, it has smaller critical paths than the other filter pair. Consider this filter pair required four lifting steps and also it requires simple multiplications say,

$\alpha=-1.586134342$

$\beta=-0.052980118$

$\gamma=0.8829110762$

$\delta=0.4435068522$ and scaling coefficients are $K=1.149604398$ and this also implements using shift and add logic.

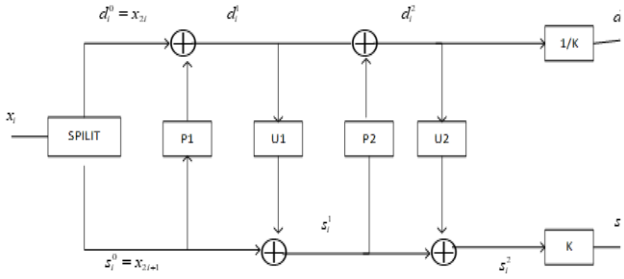


Fig. 1. 9/7 Filter Lifting Scheme.

The lifting scheme realize using four basic steps shown in figure1, they are Splitting, Prediction (P), Updating (U) and Scaling (K), Where $s_i^0$ and $d_i^0$ are the even and odd components of input sequence for 9/7 filter pair with N=2, $S_1$=-1.586134342, $U_1$=-0.052980118, $P_2$=0.8829110762, $U_2$=0.4435068522, and K=1.149604398 so lifting scheme or 9/7 filter bank comprises of two prediction step and two update step that are calculated by the following equations.

$s_i^0=x_{2i}$, $d_i^0=x_{2i+1}$ and

$$d_i^1=d_i^0+\alpha(s_i^0+s_{i+1}^0) \quad (3)$$

$$s_i^1=s_i^0+\beta(d_{i-1}^1+d_i^1) \quad (4)$$

$$d_i^2=d_i^1+\gamma(s_i^1+s_{i+1}^1) \quad (5)$$

$$s_i^2=s_i^1+\delta(d_{i-1}^2+d_i^2) \quad (6)$$

$$d_i=\frac{d_i^2}{k} \quad (7)$$

$$s_i = s_i^2 \times k \quad (8)$$

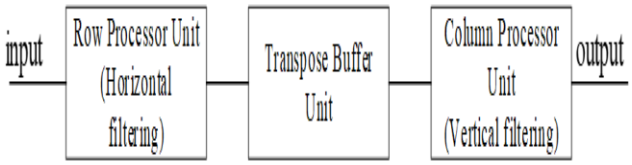


**Fig. 2. Hardware Architecture Block Diagram.**

From the above equation, to calculate the predictor and update the lifting framework, at least three image samples must be available together.

If image data is entered in a raster scan manner, this will correspond to the DWT row processing order. However, the image data must always be reordered in a column-wise sequence to perform the 2D DWT column implementation. As shown in Figure 2, the suggested DWT architecture comprises mainly of three units.

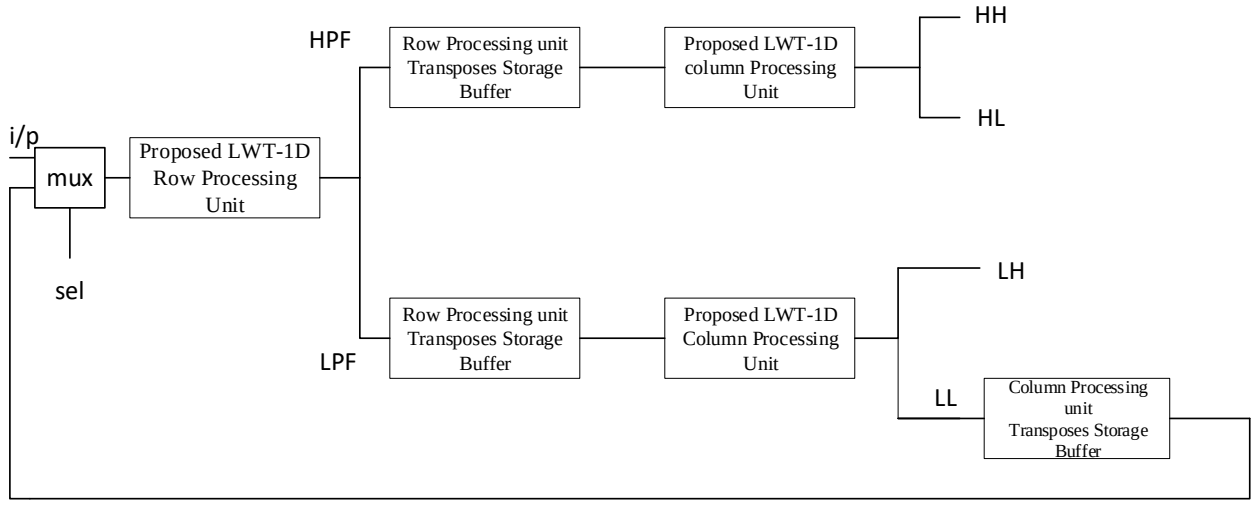


**Fig. 1. Proposed two level Decomposition DWT**

The suggested algorithm utilizes medium data distribution on various independent data flow graph (DFG) paths. Parallel measures are introduced to decrease the critical path length to Tm with a very basic control path. The suggested dual-scan architecture requires only N*N/2 computers to handle NxN image, and only five registers are switched.

## IV. PROPOSED FLIPPING ARCHITECTURE

The suggested lifting system 2D-DWT 9/7 in Fig 3 Each DWT generates four subband i.e., LL, LH, HL and HH linked to the temporary processor for transforming output of these temporary transformers consisting of detailed coefficients and approximate coefficients. The suggested architecture has 1D row (RPU) and column (CPU) processor unit for executing 1D DWT in both rows and columns, as well as a transposing unit (TU). Use a time memory to store coefficients processed in the intermediate 1D row. A fresh, optimized dual-line scanning technique is provided to decrease latency and create the transposition buffer size regardless of image size. An efficient less power TU has only five registers in line-based architectures, not the traditional 1.5N memory requirement. Rather than using distinct RPU and CPU scaling equipment for scaling factor K and 1/K. This decreases space, power and latency. Pipeline shift-and-add logic develops proposed DWT 2D architecture multipliers. This method reduces the critical path and latency with trade off in area. Multiplication is introduced with constant lifting coefficients 9/7. Where $d_{i+2}^0$ and $s_{i+2}^0$ are current cycle and $d_i^2$ and $s_i^2$ are current cycle outputs obtained from $d_{i+1}^0, s_{i+1}^0$, $d_i^1$ $s_i^1$ and $d_{i-1}^2$ intermediate data from inbuilt memory devices. The standard lifting system processes these intermediate information serially, which results in a longer critical route.

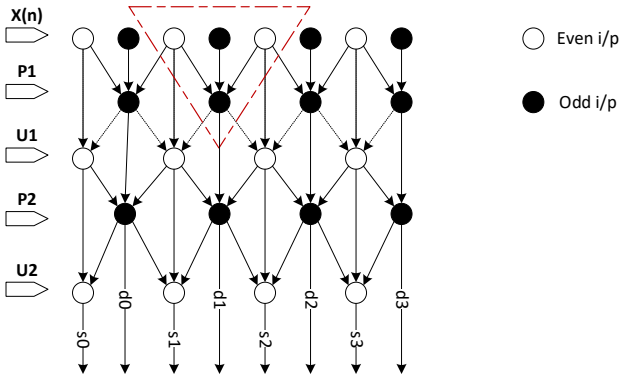


**Fig. 2(a). 9/7 Conventional Signal Flow Graph lifting steps**

Thus the data flow graph is modified to process the intermediate information in advance to shorten the critical path in the suggested algorithm as follows.

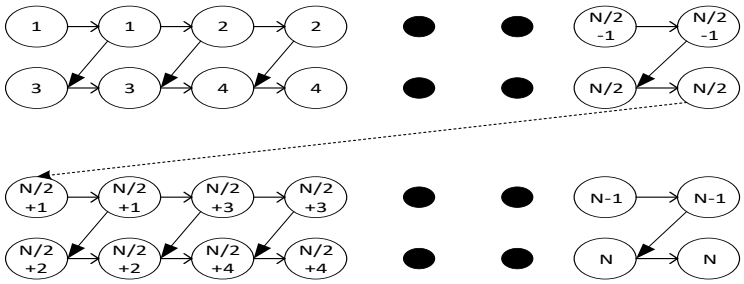


Fig. 3. Dual Z scanning scheme.

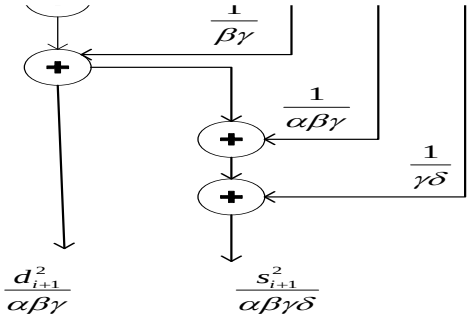


**Fig. 4. (b) Modified 9/7 Signal Flow Graph Lifting Steps.**

$$\frac{d_i^1}{\alpha} = \frac{d_i^0}{\alpha} + (s_i^0 + s_{i+1}^0) \quad (9)$$

$$\frac{s_i^1}{\alpha\beta} = \frac{s_i^0}{\alpha\beta} + (\frac{d_{i-1}^1 + d_i^1}{\alpha}) \quad (10)$$

$$\frac{d_i^2}{\alpha\beta\gamma} = \frac{d_i^1}{\alpha\beta\gamma} + (\frac{s_i^1 + s_{i+1}^1}{\alpha\beta}) \quad (11)$$

$$\frac{s_i^2}{\alpha\beta\gamma\delta} = \frac{s_i^1}{\alpha\beta\gamma\delta} + (\frac{d_{i-1}^2 + d_i^2}{\alpha\beta\gamma}) \quad (12)$$

Since these intermediate data is on distinct routes, it can be calculated parallel to the current procedure and then used in the subsequent operation. For instance, in (9) operation, $\frac{d_i^1}{\alpha}$ is calculated simultaneously with the addition operation between $s_i^0$ and $s_{i+1}^0$ during the estimation cycle of $\frac{d_i^1}{\alpha}$. Similarly, it is determined manner (10). During the second lifting phase in (11) and (12), the targets $d_i^1$ and $s_i^1$ are scaled by $\frac{1}{\beta\gamma}$ and $\frac{1}{\gamma\delta}$, respectively, instead of $\frac{1}{\alpha\beta\gamma}$ and $\frac{1}{\alpha\beta\gamma\delta}$, because the second lifting phase uses the outputs $\frac{d_i^1}{\alpha}$ and $\frac{s_i^1}{\alpha\beta}$ generated from the first lifting unit. The final output is scaled by

$$d_i = \frac{d_i^2 \alpha\beta\gamma}{k} \quad (13)$$

$$s_i = s_i^2 \times \alpha\beta\gamma\delta k \quad (14)$$

The basic idea is to remove multiplications in the critical path by reversing the multiplier coefficients of remaining paths. Figure 4(b) describes how multiplications can be lowered by scaling at each point and further splits the extra three input nodes into two adders of 2 inputs. 5Ta is the critical path.

### A. Dual Z Scan Flipping Hardware Architecture

The Dual-Z Scan Flipping (DSFA) hardware architecture is obtained from the revised signal diagram, as shown in Fig.5. Odd and even outputs are obtained as shown in the Figure4 in Z-scan, where the figures show the order of pixels read on the positive edge of the clock. Column processing may begin once a 1-D DWT image is generated. The entire image can be segmented into 2 pixels to process in alternating rows. Z-scanning allows the simultaneous processing of rows and columns to generate small set latency and transfer buffer size, independent of N.

The Fig. 6(a) and 7(a) shows the data signal flow graph of the processing element unit and internal architectures of processing element of Row processing and Column processing element. The proposed method has been implemented with parallel processing unit, the operation of 1D DWT as follows, the input image pixel is split in to even and odd samples which is known as lazy wavelet, then the odd samples receive the predicted module during first clock cycle, then the even input sample and previous even input sample are added, then the previous odd sample is multiplied with the first filter coefficients during the second and third clock cycles, during this time shift and add arithmetic operation were performed. During fourth clock cycle the shift and add result is added with the odd sample input which gives the result of predict output. During fifth clock cycle the present predict value and the previous predict value along with the past even input sample gives the updated value. The signal flow graph shows that only adders are required to compute the each of clock cycle, so that the critical path can be limited with the delay.

The Row Processing Element (RPE) line has two input lines and a multiplier line is shown in Fig.6 (a).

The RPE also has two adders, one shift add logic. The present and previous even pixels are fed to the adder line and they are added for row processing operation and a pre-calculated constant coefficients multiply an odd pixel fed to the multiplier line, depending on the specific RPE. The suggested algorithm utilizes the inversion values of the coefficients, which are sufficiently large to cause an overflow during multiplication operation. For 2's complement arithmetic operations, it is possible to reduce the critical path by multiplying the flipping coefficient [35] values by $2^k$, where k is an integer.

Consequently, constants $2^4$ , $2^5$ , and $2^3$ are scaled in equations (11), (12) and (13). Therefore, the result of adding 3D register information is divided by the SAL's right shift operation. Tabulated in Table I are the necessary right shift and the new scaled-coefficients. Equation (9) is not broken down by a scalable factor as the value α is greater than 1, but (10) is split into 16 resulting in a 4-bit change through the shift register. Similarly, (11) is divided by 32, with the predecessor RPE providing the correct one-bit shift as a correct four-bit shift, and (12) is divided by 8, resulting in a 2-bit shift, as the predecessor RPE already produces a 1-bit shift. Finally, the scaling system retrieves the output by multiplying (13) by 32 and (14) by 128. Table II demonstrates the processing element1 line processing process information flow, showing a 5-clock latency to execute the output. Thus, the previous pipeline's second entry. digit bits for the integer and last 5 digit bits for the fraction part [7]. To execute a 2D DWT operation, a Transposition Unit (TU) is placed in between the 1D row processor and 1D column processor. The 1D row registers have only five registers highpass (H) inputs and lowpass (L) outputs, with one 4to2 multiplexer as shown in Fig.8. As shown in Table II, rearrange the high-processor to supply the 1D column processor. The CPE is similar to RPE, compared to RPE, the CPE has a line buffer, as shown in Fig. 7(b). Output line 2 is delayed by 3 clocks to synchronize the two unit delays in two digit bits for the integer and last 5 digit bits for the fraction part [7]. To execute a 2D DWT operation, a Transposition Unit (TU) is placed in between the 1D row processor and 1D column processor. The 1D row registers have only five registers highpass (H) inputs and lowpass (L) outputs, with one 4to2 multiplexer as shown in Fig.8. As shown in Table II, rearrange the high-processor to supply the 1D column processor. The CPE is similar to RPE, compared to RPE, the CPE has a line buffer, as shown in Fig. 7(b).

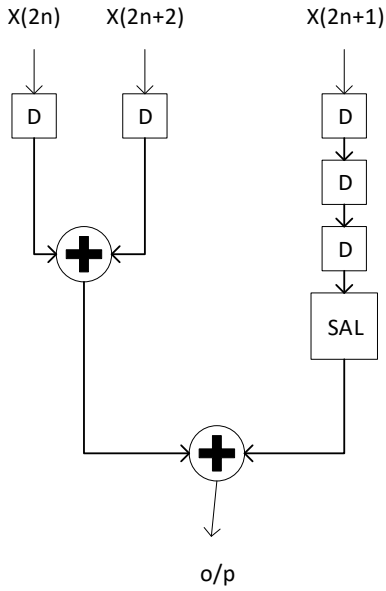


**Fig. 4 (a) Row Processing Element**

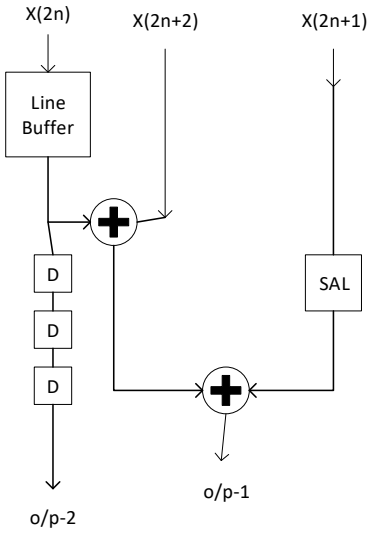


**Fig. 6(b) Column Processing Element**

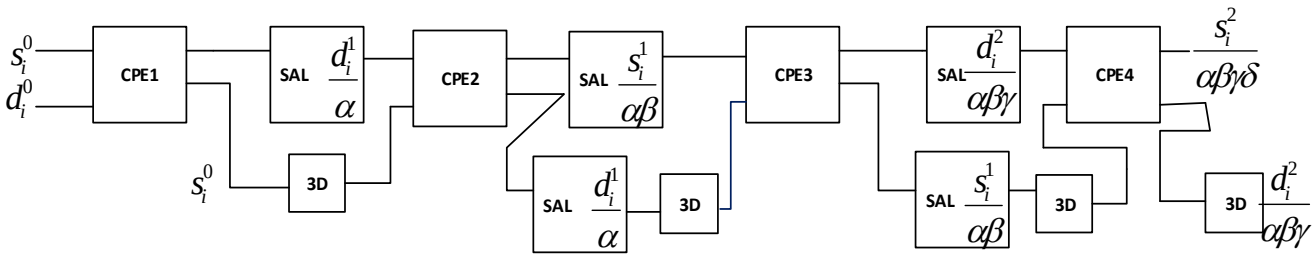


**Fig. 7(a) Column Processor Unit**

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Output line 2 is delayed by 3 clocks to synchronize the two unit delays in two adder element and one shifter delay element in output1. Then both output lines connect to further processing element. Figure 7(b) shows the column processors complete architecture. A multilevel 2D DWT also be computed with the dual scans chip architecture by using off-chip is delayed by five clocks, as shown in the Figure. 6(b). Therefore, the critical path delay has only one product delay. The hardware has 16-bit fixed-point at $\frac{N^2}{4}$ memory

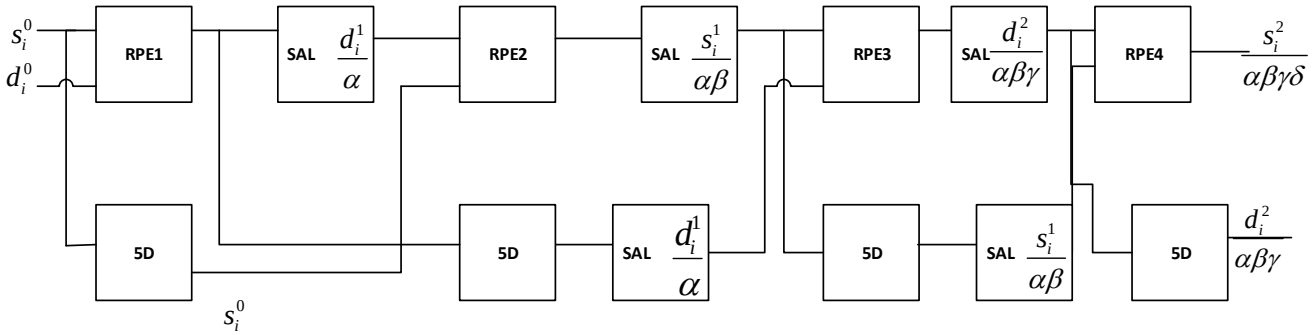


**Fig. 7(b). Row Processor Unit.**

for storing present-level LL band coefficients for next greater level DWT calculations. In order to calculate a j-level DWT $\frac{2}{2^{j-1}}\left(2+\frac{N}{2^j}\right)$ clock cycles are needed for neglecting the latency.

## V. PERFORMANCE ANALYSIS AND DICUSSION

Tables III and IV assess the performing comparison with existing 1D and 2-D 9/7 DWT architectures. The suggested 1D processing unit requires eight adders and four SALs with 20 delay registers. Compared to the suggested NxN architecture, there is a critical path delay for $T_m$ , with an output of $\frac{N^2}{2}$ two computing cycles per cycle to process an image control path. In addition, the pre-calculation in [39] is irregular, whereas the suggested scheme is very uniform with only one multiplication. Thus, the 1-D processing element in [39] cannot be folded, whereas the suggested 1D processing element can be folded easily and the resulting information route decreases to two adders and one multiplier without losing the critical path. The optimized lifting architecture proposed in [40] has as good as critical path latency, but clock cycles are needed. The performing comparison with other existing 1-D and 2-D 9/7 DWT architectures is assessed in Tables III and IV. Eight adders and four SAL with 20 delay registries are required for the proposed 1-D processor. There is a critical path delay for with an output of two computing cycles per cycle to process an image control path when compared to the proposed NxN architecture. Furthermore, pre-calculation in [39] is irregular, whereas it is very uniform with only one multiplication in the suggested scheme. The 1D processing element cannot be folded, whereas the 1D processing element proposed by the design can be folded easily and the resulting data route reduces to two adders and one multiplier without changing the critical path. The optimized lifting architecture proposed in [40] has comparable critical path latency, but N*N clock cycles needed.

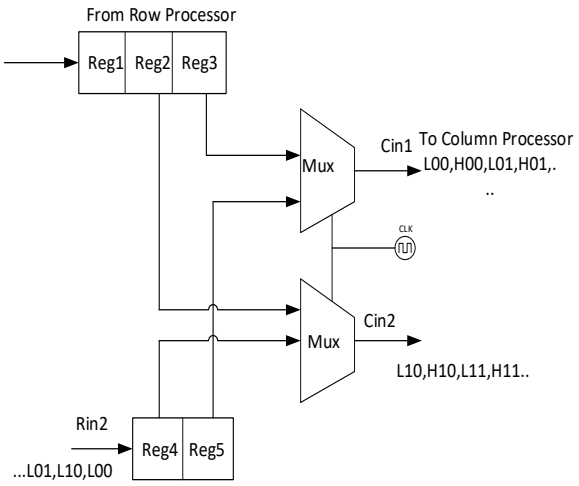


**Fig. 8.Transposition Unit**

Table I. Coefficients for column and Row Filter

| Flipping coefficient | Flipping coefficient value | Binary value (half precision-16 bit) fixed point | Shift Logic(>>-Right Shift,<<-Left Shift) |
|---|---|---|---|
| $\frac{1}{\alpha}$ | -.0630 | 101110 0100001010 | 2<<3+2<<2+2<<1+2>>1+2>>6+2>>8 |
| $\frac{1}{\alpha\beta}$ | 11.91 | 0 0010 0111110100 | 2<<4+2<<1+2>>1+2>>2+2>>3+2>>4+2>>5+ 2>>7 |
| $\frac{1}{\alpha\beta\gamma}$ | 13.47 | 0 0010 1010111100 | 2<<4+2<<1+1+2>>2+2>>4+2>>5+2>>6+2>>7 |
| $\frac{1}{\beta\gamma}$ | -2.718 | 1 0000 0101110000 | 2<<4+2>>1+2>>3+2>>4+2>>5 |
| $\frac{1}{\alpha\beta\gamma\delta}$ | 11.72 | 0 0010 0111011100 | 2<<4+2<<1+>>1+2>>2+2>>3+2>>5+2>>6+ 2>>7 |
| $\frac{1}{\gamma\delta}$ | 2.551 | 0 0000 0100011010 | 2<<4+2>>1+2>>5+2>>6+2>>8 |
| $\alpha\beta\gamma\delta k$ | 0.038 | 0 1010 0011011101 | 2<<3+2<<1+2>>2+2>>3+2>>5+2>>6+2>>7+ 2>>9 |
| $\frac{\alpha\beta\gamma}{k}$ | 0.064 | 0 1011 0000011001 | 2<<3+2<<1+1+2>>6+2>>7+2>>9 |

Table-II: Data Flow of Transpose Unit of 9/7 filter

| Clock | Rin1 | Rin2 | Reg1 | Reg2 | Reg3 | Reg4 | Reg5 | Cin1 | Cin2 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | $H_{00}$ | $L_{00}$ | - | - | - | - | - | - | - |
| 1 | $H_{10}$ | $L_{10}$ | $H_{00}$ | - | - | $L_{00}$ | - | - | - |
| 2 | $H_{01}$ | $L_{01}$ | $H_{10}$ | $H_{00}$ | - | $L_{10}$ | $L_{00}$ | $L_{10}$ | $L_{00}$ |
| 3 | $H_{11}$ | $L_{11}$ | $H_{01}$ | $H_{10}$ | $H_{00}$ | $L_{01}$ | $L_{10}$ | $H_{10}$ | $H_{00}$ |
| 4 | $H_{02}$ | $L_{02}$ | $H_{11}$ | $H_{01}$ | $H_{10}$ | $L_{11}$ | $L_{01}$ | $L_{11}$ | $L_{01}$ |

Table III. Hardware Requirements of 2D DWT

| | Row Filter | Column Filter | Scaling | Total |
|---|---|---|---|---|
| Adder | 38 | 4 | 60 | 85 |
| Subtractor | 4 | 4 | 0 | 8 |
| Register | 60 | 17 | 6 | 112 |

The suggested one-dimensional DWT architecture has a much better critical route delay [41] and a better efficiency than the job in [40]. The suggested 2-D architecture uses 76 adders, 8 subtractors and 4 for final scaling shown in Fig 9. Each processing component uses two extra parts, leading in a total of sixteen parts for 2D DWT processing. The DSFA can be folded into six SAL and eight extra modules without affecting critical path. This flipping offers less critical path time than RAM-based architectures [45] and dual-scan [15]. The pipeline-back architecture defined in [47]'s critical route delay is the same as the DSFA, but buffer size is $11N$.

The architectural technique outlined in [36] seeks to reduce calculation cycles by improving parallelism.. Hsia et al.[35] recently proposed a two-dimensional memory efficient DWT lifting architecture with 4N time buffer and 2Tm+4Ta critical path delay. The proposed DSFA utilizes the same time storage

size but has reduced cycle, latency, and critical routes than indicated in [35]. Hsia et al. propose a multiply-and-accumulate $1.5(N+3)$ cycle's latency with $N+3$ compared to DSFA. The suggested 2-D DWT DSFA is introduced on a target Xilinx Spartan 6 xc6slx45t-3-fgg484 field-programmable gate array (FPGA) and 1D level output Shown in Fig 10. The FGPA execution information shows the critical path delay of 5.6 ns proposed architecture and uses a total of 1769 four-input lookup tables.

Table IV. Performance Comparison of 1-D DWT Hardware Architecture.

| Architecture | Adders | Multipliers | Registers | Critical Path | Throughput |
|---|---|---|---|---|---|
| Direct | 8 | 4 | 6 | $4T_m + 8T_a$ | 2 |
| Flipping | 8 | 4 | 4 | $T_m + 5T_a$ | 2 |
| Zhang et al. [42] | 8 | 4 | 18 | $T_m$ | 2 |
| Lai et al. [43] | 8 | 4 | 22 | $T_m$ | 2 |
| Wu et al. [40] | 4 | 2 | 20 | $T_m$ | 1 |
| Darji et al. [44] | 8 | 4 | 20 | $T_m$ | 2 |
| Proposed DSFA | 38 | 0 | 112 | $5T_a$ | 2 |

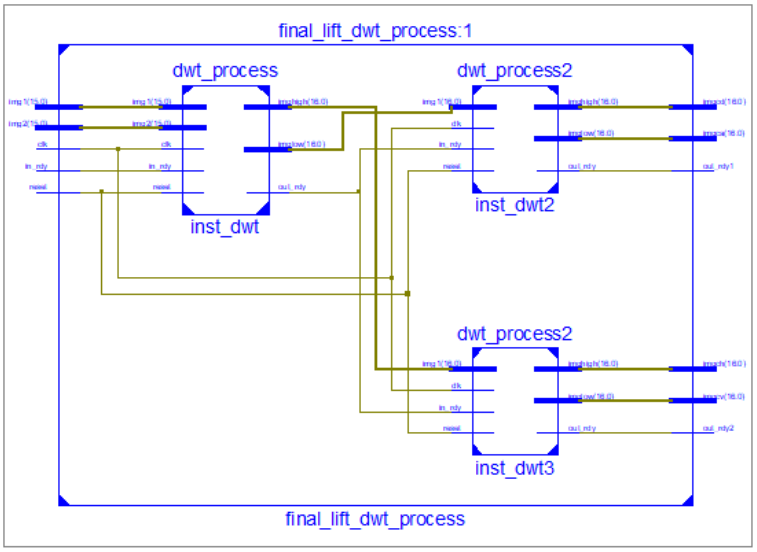


**Fig. 9. DWT one level Decomposition Hardware structure**

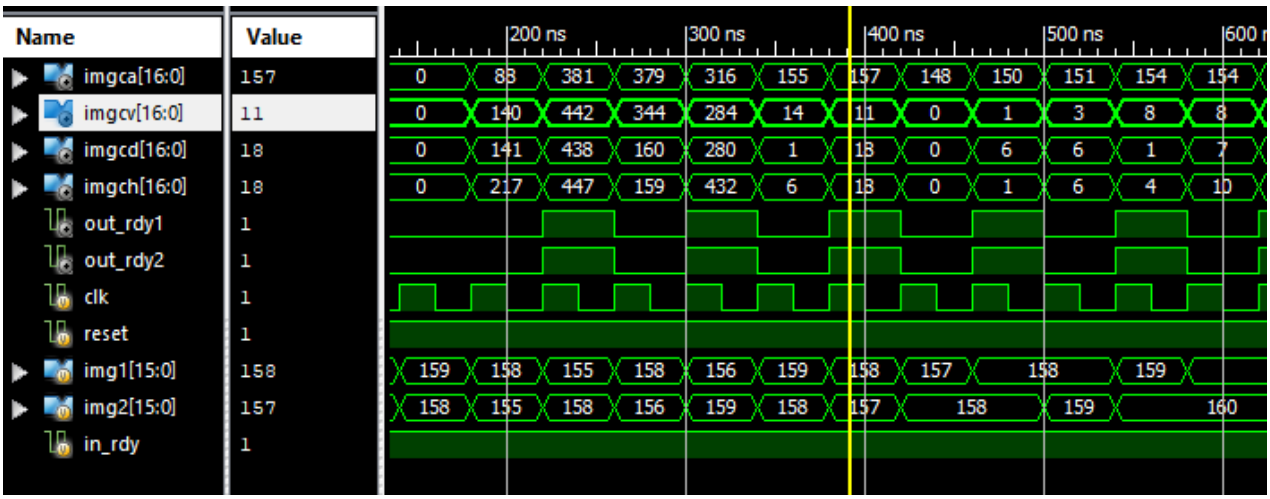


**Fig. 10. Final decomposed output image data.**

## VI. CONCLUSION

For a 9/7 lifting filter, novel flipping-based one-dimensional and two-dimensional DWT architectures were suggested. Compared to the best of the current hardware complexity, critical path removal, memory size and architecture performance, the suggested DSFA proposed a multiplier-less 2D DWT off-chip Architecture. The architecture especially suits high-speed image processing. Implement a three-input DWT architecture. Adders and hardware shifters for replacing multipliers are less time consuming. The proposed architecture thus achieves a critical delay of almost one full delay and is more efficient than current parallel architectures. DSFA was found as a symmetrical high-speed architecture with reduced hardware complexity. It also needs less memory

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