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Optimization of Switching Loss of a DC-DC Boost Converter

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Abstract*: The dc-dc boost converters are widely used in various power conversion applications because of their increase in demand both in domestic, commercial and industrial applications. The voltage boosting techniques include mostly combination of components such as inductors, capacitors, switches etc with their various configurations. The combination of these boosting components oriented in different configurations appears largely in literature, but refer the techniques of hard-switching of the semi-conductor devices. In order to meet the growing demand and to look into the aspect of better efficiency of these converters, the soft-switching of devices plays a prominent role, which lacks in literature. Though very few papers appear in literature as far as soft-switching is concerned, but the addition of more than one or two switches make the things uneasy and the researchers lack interest in it. Even though the conventional boost converters appear in various forms of topologies in literature, but it needs further critical investigation so far to minimise switching loss. The proposed topology, which is similar to the conventional topology with slight modification, gives lucid insight in fulfilling with partial soft-switching capability of circuits. The single switch is turned-off under zero-voltage switching (ZVS) and turned-on under partial hard-switched by proper designing of snubber components. The prominent components of the topology are designed at its optimum level to improve performance.

Keywords* : Boost converter, Polypropylene switched capacitor, ferrite core switched inductor, Fast recovery diodes, Soft-switching.

I. INTRODUCTION

The step-up dc-dc converters/ boost converters transform dc power from lower voltage to higher voltage level by storing energy temporarily and then releasing at higher voltage at its output level. This storage of energy can occur in inductor in form of magnetic field or in capacitor in form of electric field through switching elements. The step-up dc-dc converter, which is hard-switched, non-isolated and having high efficiency, is demonstrated. The inclusion of coupled inductor is investigated [2-4], whereas in [5], it is presented a tapped inductor for boost converter. Siwakoti et.al [6] presented z-source based boost converter. The steady-state analysis of dc-dc converters are presented [7].

Prahala et.al.[8] has focussed on very high voltage multiplier technique using two separate boost stages at input. In this case, the topology comprises a series of diodes and capacitors in stages and provides additional losses as burden upon equipment. However, all above converters suffers from hard-switching. The soft-switching techniques overweigh in many aspects over hard-switching. Researchers [6,8 -15] have stressed upon soft-switching using load resonant technique, parallel-resonant zero-voltage transition technique, zero-current transition technique and quasi-resonant technique. The quasi-resonant principle [15] is much better over all other resonant principles, as the switching devices are not only relieved from the switching stress, but also from overvoltage. The conventional boost topology is shown in Fig.1.

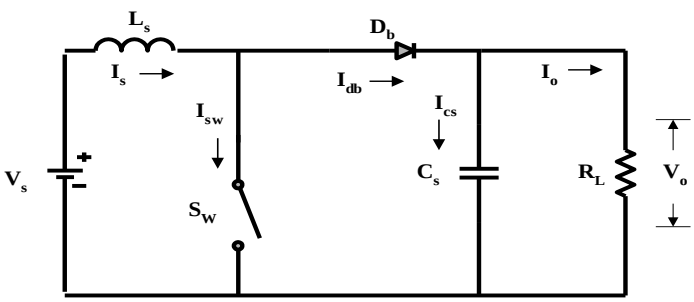

Fig.1. Conventional Boost Converter

This topology in reality possesses the switching loss during turn-on and turn-off due to series resistance–capacitor across the switching device. Because of hard-switched, the switching frequency is limited to few kHz. As the level of output power goes up, it restricts in increasing switching frequency and suffers from many limitations like large heat sink, EMI problem, increase in weight, communication line interference etc In present literature, the conventional boost converter is modified to suit the soft-switching technology to improve the performance.

II. PROPOSED TOPOLOGY AND OPERATIONAL ANALYSIS.

In this paper, the proposed topology is a modified of the conventional one as shown in Fig.2.

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This is intended to include soft-switching technique to minimise switching loss. Further, the prominent component values, which are responsible in aiding switching loss, have been optimised after proper design. The various modes of operation for the proposed modified boost converter are shown in Fig.3.

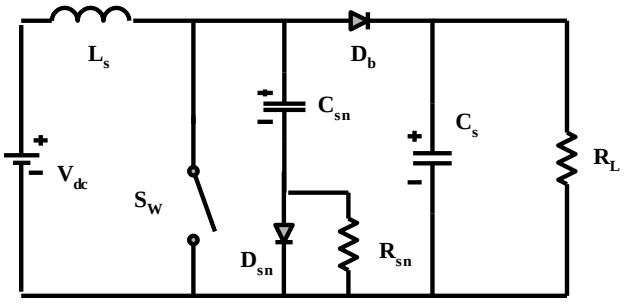

Fig.2. The proposed modified topology

When the proposed circuit is provided dc supply without turning-on the switch, the capacitors across load(i.e., also known as boost capacitor, C_s) and device (i.e., snubber capacitor C_{sn}) are charged to peak of input. The magnitude of this output depends upon duty ratio of the switch. As the duty-ratio increases, the average output voltage level increases and vice-versa. The output voltage is usually more than input and governed by mathematical equation which is discussed afterwards in analysis. As the source inductor (i.e., boost inductor, L_s) pumps the energy to output during the period of switching-off the device, the average output voltage across load(i.e., same as that of capacitor) is more than fixed input dc.

The mode-I operation is initiated with closing the switch and shown in Fig. 3(a). The source voltage is shorted through inductor and snubber capacitor releases energy to the resistor through switch. The boost capacitor provides the power to load. This mode continues till the voltage across snubber capacitor falls to zero and Mode-II is commenced shown in Fig.3(b). Here the source inductor current goes on increasing as the switch is still on and simultaneously the boost capacitor still provides power to load. Mode-III is initiated with opening up the switch. Now the dc voltage source along with energy stored in source inductor is acted upon snubber capacitor which is earlier at zero-voltage level. This mode continues till the snubber capacitor is charged to peak of input dc supply. During the snubber capacitor is charged from zero to input dc level, the device is turned-off under zero-voltage switching due to snubber capacitor appearing across the device. This charging time of snubber capacitor is sufficient to facilitate soft-switching off the device. The snubber capacitor is charged through the diode and device is switched off at cut-in voltage appearing across it. In Mode-IV, the voltage level across the capacitor rises above input level as the polarity of voltage across the source inductor reverses due to fall in source current. The input voltage dc combined with reversed polarity voltage across the source inductor is acted upon boost capacitor. By this action the average voltage across boost capacitor (Cs) is maintained at higher level than input dc. But the source current is maintained continuous, and the cycle repeats with closure of switch (Mode-I) after Mode-IV.

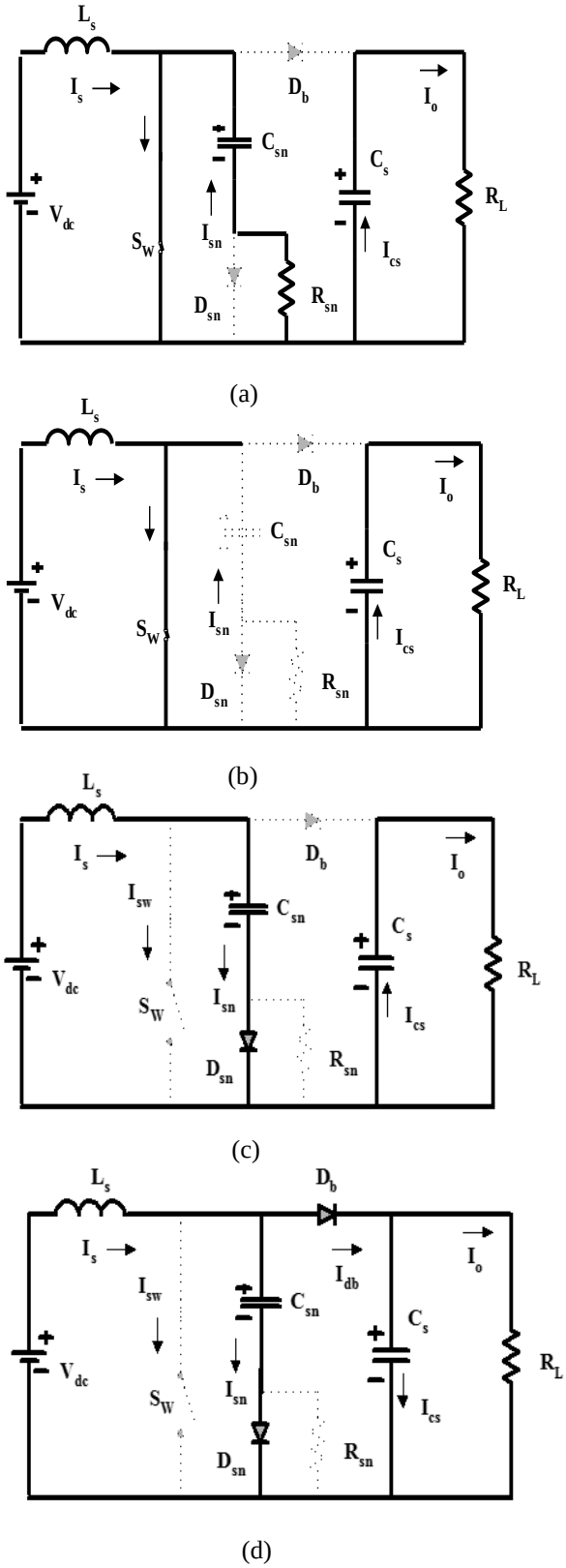

Fig.3 Various modes of operation of proposed topology

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III. STEADY-STATE ANALYSIS AND OPTIMAL DESIGN OF COMPONENTS.

The total switching period (T) of the proposed topology is divided into two intervals (i.e., on time (t_1) and off-time(t_2); $T= 1/f_s = t_1+t_2$). where as 'f_s' is the switching frequency. The steady-state analysis of conventional boost converter is presented.

A. During Turn-on process of switch

The source inductor current rises from I_1 to I_2 in time t_1.

$$V_s = L_s\left(\frac{di}{dt}\right) \quad for\ 0 < t \le t_1 \ \ and\ I_1 < i \le I_2 \qquad (1)$$

$$=> \int_{I_1}^{I_2} di = \int_0^{t_1} \frac{V_s}{L_s}\, dt$$

$$=> \quad I_2 - I_1 = \frac{V_s}{L_s} t_1 \qquad (2)$$

B. During Turn-off process of switch

The source inductor current changes from I_2 to I_1 in time t_2 (off-period of switch). 'V_o' is the average output voltage across load. 'Vs' is the input dc supply.

$$V_s - V_o = L_s\left(\frac{di}{dt}\right) \quad for \quad t_1 < t \le T\ ;$$

$$I_2 < i \le I_1 \ and\ t_1 + t_2 = T \qquad (3)$$

$$L_s\left(\frac{di}{dt}\right) = V_s - V_o \quad => \int_{I_2}^{I_1} di = \int_{t_1}^{T} \frac{V_s - V_o}{L_s} dt$$

$$=> \quad I_1 - I_2 = \frac{V_s - V_o}{L_s}(T - t_1) \quad =>$$

$$I_2 - I_1 = \frac{V_o - V_s}{L_s} t_2 \qquad (4)$$

Equating (2) &(4),

$$=> \quad \frac{V_s}{L_s} t_1 = \left(\frac{V_o - V_s}{L_s}\right) t_2 \qquad (5)$$

$$=> \quad V_o = \frac{V_s}{1-k} \ \ and\ \ k = \frac{t_1}{T} \qquad (6)$$

Eq.(6) depicts the relation between input voltage (V_s) and output voltage (V_o).

$$1 - k = 1 - \frac{t_1}{T} = \frac{V_s}{V_o} \quad => t_1 = \frac{V_o - V_s}{V_o f_s} \qquad (7)$$

From (2) and (4) => $t_1 = \frac{L_s}{V_s}(I_2 - I_1)$ and $t_2 = \frac{L_s}{V_o - V_s}(I_2 - I_1)$ (8)

$$=> T = \frac{1}{f_s} = t_1 + t_2 = \frac{L_s V_o}{V_s(V_o - V_s)}(I_2 - I_1) = \frac{L_s}{V_s k}(I_2 - I_1) \qquad (9)$$

Where 'T' is the switching period and 'f_s' is switching frequency. As current $I_2 > I_1$, the equation (9) is simplified to

$$\Delta I = (I_2 - I_1) = \frac{V_s k}{f_s L_s} \qquad (10)$$

$$=> \quad f_s = \frac{V_s k}{L_s\ \Delta I} \qquad (11)$$

If the circuit is assumed lossless, input power = output power

$$=> \quad V_s I_s = V_o I_o \qquad (12)$$

Substituting the relation between V_s and V_o of (6) in eq.(12), we get

$$I_s = \frac{I_o}{(1-k)} \qquad (13)$$

C. Design of Boost Inductor

In order to know the condition for verge of the continuous mode from discontinuous mode of input current, the source/ boost inductor ripple current is $\Delta I = 2\, I_s$ where I_s is the average source/input current.

Combining (10) and (13) in following assumption.

$$=> \Delta I = 2\, I_s \ => \quad \frac{kV_s}{f_s L_s} = 2\frac{I_o}{1-k} \qquad (14)$$

$$= \frac{2V_o}{(1-k)R_L} = \frac{2V_s}{(1-k)^2 R_L} \qquad (15)$$

$$=> L_s = \frac{k(1-k)^2 R_L}{2\, f_s} = L_{cs}(\text{critical}) \qquad (16)$$

where L_{cs} (critical) = Critical value of L_s below which the source current changes from continuous current to discontinuous mode (DCM). R_L=load resistance. In eq.(15), $\Delta I = 2I_s$ is the maximum ripple under verge of continuous current mode. If load resistance and switching frequency are assumed to be constant, the value of L_{cs} (critical) is a function of $k(1-k)^2$.

If ripple is to made as small as possible (i.e., say factor 'a' as %age of maximum ripple peak value), then $\Delta I = a(2I_s)$ and eq.(16) becomes

$$=> L_s = \frac{k(1-k)^2 R_L}{2\, a\ f_s} \qquad (17)$$

D. Design of Boost/Load Capacitor

During the turn-off of the switch, the boost capacitor provides load current from $t=t_1$ to end of the switching period. The average current of boost capacitor during time (t_1) is $I_{cs} = I_o$ and assuming constant load current, the peak to peak ripple voltage of capacitor is

$$\Delta V_{cs} = \frac{1}{C_s}\int_0^{t_1} i_{cs}\ dt = \frac{I_o t_1}{C_s} \qquad (18)$$

Substituting value of t_1 from (7) in (18)

$$\Delta V_{cs} = \frac{I_o}{C_s}\frac{(V_o - V_s)}{V_a\, f_s} = \frac{I_o}{C_s}\frac{k}{f_s} \qquad (19)$$

Similarly for capacitor the voltage condition from continuous mode to discontinuous mode, the maximum ripple capacitor voltage

$$\Delta V_{cs} = 2V_{cs} = 2V_o \qquad (20)$$

, where V_{cs} is the average capacitor voltage, which is output voltage (Vo).

On equating (19) and (20) , we get

$$=> 2V_{cs} = \frac{I_o}{C_s}\frac{k}{f_s} \quad => \quad 2I_0 R_L = \frac{I_o}{C_s}\frac{k}{f_s} \qquad (22)$$

where Io is the average load/ output current and eq.(22) is simplified to

$$=> \quad C_s(critical) = C_s = \frac{k}{2R_L f_s} \qquad (23)$$

Where C_s (critical) is the critical value of C_s below which the capacitor voltage goes from the continuous mode to verge of discontinuous mode. If the ripple content is needed to reduce both on input and output side, the value of actual values of L_s and C_s must be greater than those corresponding critical values L_s(critical) and C_s(critical). In case of %age ripple factor 'a' is to be included , then

$\Delta V_{cs} = a(2V_{cs})$ and eq. (23) is changed to

$$C_s = \frac{k}{2a\, R_L f_s} \qquad (24)$$

If ripple factor on load votage is needed as minimum as possible, then the capacitor $C_s >> C_s$(min) Eq.(24) is the expression under consideration of ripple factor. In boost converter, the significant ripple factor may be allowed but with continuous conduction in source current, but in case of load voltage , the ripple factor is very small.

E. Design of Snubber Capacitor

The snubber capacitor helps in relieving stress upon device during switching off . During every switching period, the snubber capacitor is charged and discharged by feeding energy to resistor / source. In proposed topology, the snubber capacitor is charged during turn-off and discharged during turn-on. But discharging capacitor has two options. One way to is to dissipate the stored energy through external resistance (R_s) or other way is to reutilise by some other means. Here first one is considered diverting stored energy to external resistor.

The current through snubber resistance and power loss during turn-on of the device are as follows and this current would continue for a time constant ($\tau = R_{sn} C_{sn}$) during time-period (T).

$$i_{sn} = \frac{V_s}{R_{sn}} e^{-\frac{t}{R_{sn} C_{sn}}} \text{ and}$$

$$=> P = \frac{1}{T}\int_0^T p\, dt = \frac{1}{T}\int_0^\tau (i_{sn}^2 \; R_{sn})\, dt \qquad (25)$$

$$P = \frac{1}{2}\frac{C_{sn} V_s^2}{T}\left(1 - e^{-\frac{2\tau}{R_s n C_{sn}}}\right)$$

$$=> P = \frac{1}{2}\frac{C_{sn} V_s^2}{T} \approx \frac{1}{2} C_{sn} V_s^2 f_{sw} \qquad (26)$$

From this equation, it is obvious that losses in snubber circuit during turn-on is dependent upon the value of snubber capacitance (C_{sn}), supply voltage(V_s), switching frequency(f_s), but independent of snubber resistance(R_{sn}). So if the supply voltage and the switching frequency are made constant, the loss is totally dependent upon value of capacitance. So the value of the snubber capacitance is designed at optimum (minimum) value in order to minimise snubber loss and simultaneously facilitating switching device to undergo soft-switching off. The present topology allows the snubber capacitor to facilitate the soft-switching of device during turn-off. So in order to optimise the value of capacitor so as to minimise switching loss during on-time of device, it is mandatory to know the device off-time.

For a practical device like Power MOSFET (ex IRF 540N), the device turn-on time is 100 ns and turn-off time is 145ns as per the specification of the manufacturer. So to facilitate easy turn-off, the circuit turn-off (i.e., charging time of snubber capacitor) must be larger than the device turn-off time (i.e., specified by manufacturer) respectively.

When device is turned off, the source current is bypassed through snubber capacitor and diode. This snubber capacitor gets charged during this period. The charging time must be greater than the device turn-off time (t_q) to facilitate smooth turn-off. The equation for charging a capacitor is

$$\frac{I_p t_{off}}{C_{sn}} = V_s \qquad (27)$$

$$C_{sn} = \frac{I_p \; t_{off}}{V_s} \quad (t_{off} \approx 2 * t_q) \qquad (28)$$

where I_p : Peak current through the device (i.e., current at the end of turn-on of the device).

t_{off} : Charging time/ circuit turn-off time ;

t_q : Device turn-off time by manufacturer

The value of snubber capacitor can be found out from eq.(28)

During turn-on, the device voltage is same as supply voltage. If above MOSFET device is considered with following data (t_{off} =250nsec= 0.25 µs, I_{peak}= 20A(source), V_s=50V , f_s =25kHz), the value of C_{sn} is 0.1 µF from eq.(28) and switch loss (i.e., from eq. (26)) is 3 watt.

With above optimisation of snubber capacitance, the small energy stored in it to be dissipated snubber resistance will have no impact upon efficiency. In proposed circuit, the discharging current of snubber capacitor is to be minimised through device during turn-on by adding external resistance in series. So the peak discharging current is to be decided to be small

$$i_{sn}\ (peak) = \frac{V_s}{R_{sn}} \ll I_o \qquad (29)$$

$$\tau = R_{sn} C_{sn} < 0.1\ T \qquad (30)$$

i_{sn}(peak) =V_s/R_{sn} << Is and snubber time constant ($\tau = R_{sn} C_{sn}$) < 2 µs

The snubber resistance is to be decided by compromising between above two equation(i.e., 29 &30).

With above prevailing data, (V_s = 50V, C_{sn}= 0.02 µF, R_{sn} = 50 ohm, I_o= 20Amp, fs = 25 kHz, T=1/f_s = 40 µs) and assumption of current i_{sn}(peak) =1A and τ= 1 µs , the snubber resistance is found out (i.e., R_s = 50 ohm). The snubber loss is independent of resistance as per eq(26). If load resistance is to be assumed to be 20 ohm, the critical value of source inductance is found to be 50µH at k=0.5 from eq.(16), which specifies the situation of verge of continuous. If value of this inductor is made less than above value, the source current will be discontinuous provided the duty-ratio is unchanged. Since the ripple voltage on load side is needed to be very small (say a=0.005 or 0.5%), the boost/load capacitor is found to be 100 µF from eq.(24).

IV. SIMULATION RESULTS

In order to realise the feeling of a practical set up, the parameters of components used in this simulation are considered from data sheet of reputed manufacturer. The inductor used is ferrite core type and high frequency one. This ohmic loss of such component is minimised. Similarly the snubber capacitor across the device is polypropylene and high frequency type, but with low dielectric loss and represented with resistive component in model. The value of this component has also been considered from data sheet of manufacturer, The two diodes used across the device(D_s) and in series with load(D_b) are fast recovery type mostly preferred for high frequency operation. These diodes are having less ohmic resistance, less turn-on and turn off time The converter is having only one switch with high frequency feature and so it can be a Power Mosfet / IGBT, whose gate drive needs negligible power as the gate of this device is voltage controlled and needs to be charge injected into it. In this case a power Mosfet is considered. With fixed value of frequency = 25 kHz, switching period (Ts = 40µs), Duty-ratio= 0.5, Load resistance = 20 ohm, the other designed value are obtained. The source inductance (Ls) is 35 µH having resistance 0.01 ohm as loss equivalent. The boost capacitor/ capacitor across the load is electrolytic type having quite larger value in comparison to snubber capacitance and a dc type. Such a capacitor is considered to be having low dielectric loss and high retentive capacity of charge with respect to time. The actual inductor is considered to be less than designed value for discontinuous current at input. On comparing designed values in previous section and available components in industry, the following components (Table-I) have been considered for simulation without sacrificing performance. The topology is simulated with Simulink. The results of simulation for the topology under steady-state conditions are shown in Fig 4~7.

In Fig.4, the current and voltage across switch (i.e, I_{sw},V_{sw}), the boost diode(I_{db},V_{db}) are shown, Since the circuit is operated under the discontinuous current mode at input(i.e., before verge of continuous conduction), the current through inductor starts every time from zero. The discharging current of snubber capacitor is kept minimum by snubber resistance. There may be situation in which very small inductance may be present due to connecting wire and lead. For such a situation, the discharging current of snubber capacitor would start from zero. The MOSFET model in Simulink has a parameter of inductance in property which cannot be made zero. Presence of this very small inductance would lead to discharge snubber current to zero. In this case the current is limited to small value by adding a external resistance and along with the very small value of inductance would force the circuit to start discharging from zero.

Table-I : Specifications of components

Item	Rating	Part No of manufacturer
MOSFET (Sw)	600V,50A, Rds=0.06Ω	STW56N60DM2
Diode (D_{sn}, D_b)	250V, 40A,V_D=0.97V	MBR40250T
Boost inductor(L_s), ferrite core type	33µH, DCR=6.38mΩ Ferrite core high frequency type	732-13643-ND
Snubber capacitor (D_{sn})	0.1µF, 310V ac/ 630V dc ; Film Metallized Polypropylene type	R463I310050M1K
Load/Boost capacitor(C_s)	5 × 20µF, 450V,ESR= 2.2mΩ electrolytic type	C4ATGBW5200A3 MJ

So the device is switched on at very small value of discharging current of snubber and it leads to close to ZCS(zero-current switching). The switching device is turned off at very small voltage level across it (i.e., cut-in voltage of diode). So it is the ZVS operation. The current of boost inductor source (Is), output voltage across load (Vo), the snubber diode current(I_{dsn}) and voltage(V_{dsn}) are shown in Fig.5. It is obvious that current in inductor at source is discontinuous (i.e., close to continuous) and ensures ZCS of the device during turn-on. The duration of current rising is turn-on and the current falls after attaining peak value. The instant of falling current is the initiation of turn-off process. The turn-off duration continues till initiation of rising of current of next cycle. The current in snubber diode due to charging of snubber capacitor and voltage across the snubber diode are shown in this Fig.5.

Fig.6 shows the current and voltage of snubber capacitor (C_{sn}) and boost capacitor(C_s). The boost capacitor shows that the magnitude of its voltage is twice to input voltage at duty-ratio at 0.5 and its charging current is same as boost diode. The boost capacitor provides power to load when boost diode (D_b) is out of conduction. The discharging current through snubber capacitor is quite small as compared to its charging current. Though the simulation is carried out at duty-ratio k=0.5(i.e., on verge of discontinuous input current condition), but the requirement of inductor and load capacitor for discontinuous input current and voltage at different duty-ratios is shown in Fig.7. It is observed that maximum value of inductor is required at k=1/3 on verge discontinuous input current condition. As the duty-ratio is increased beyond k=1/3, the requirement of inductor is decreased.

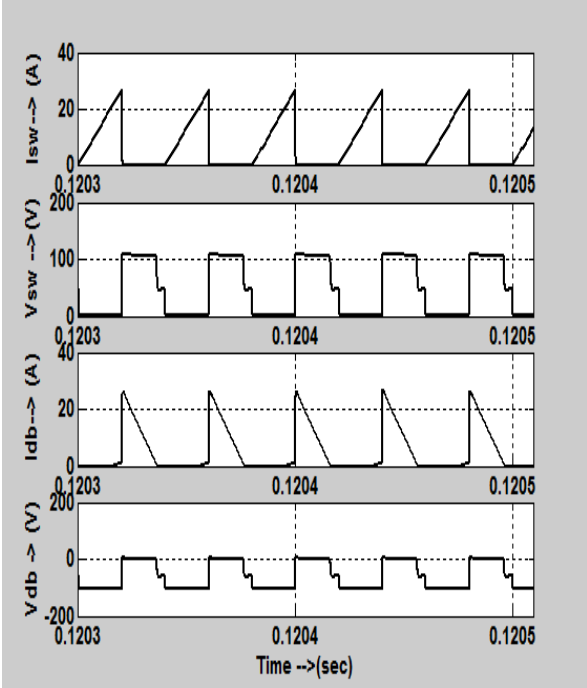

Fig.4. Current and voltage across boost switch and boost diode

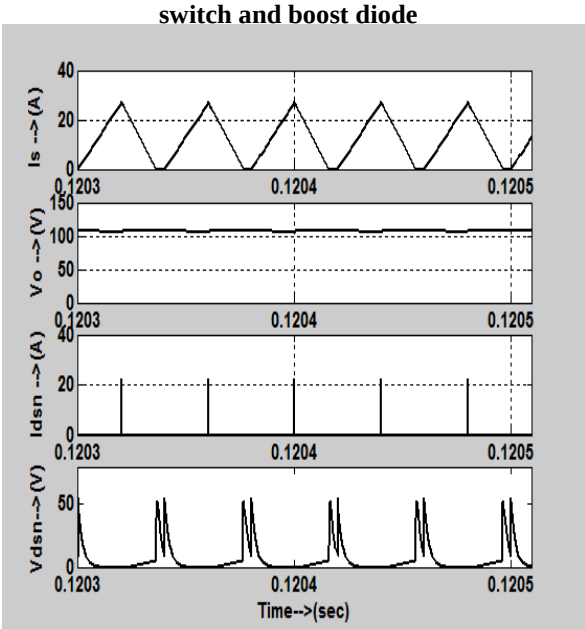

Fig.5. Waveform of current through source inductor(I_s) , load voltage(V_o), Snubber diode current(I_{dsn}) and voltage (V_{dsn})

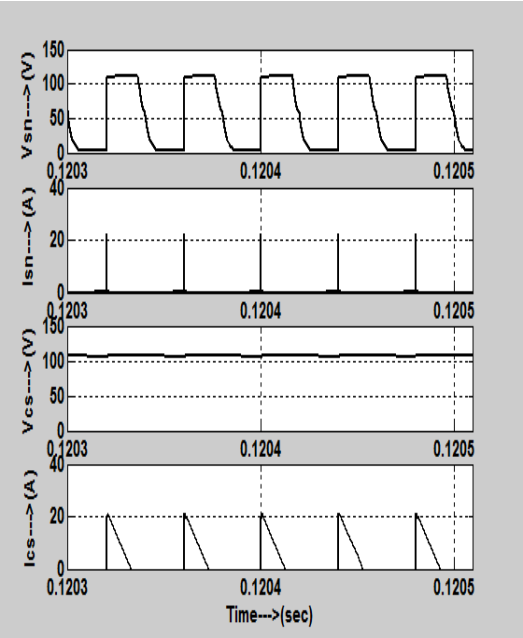

Fig.6. Current and voltage across boost switch and boost diode

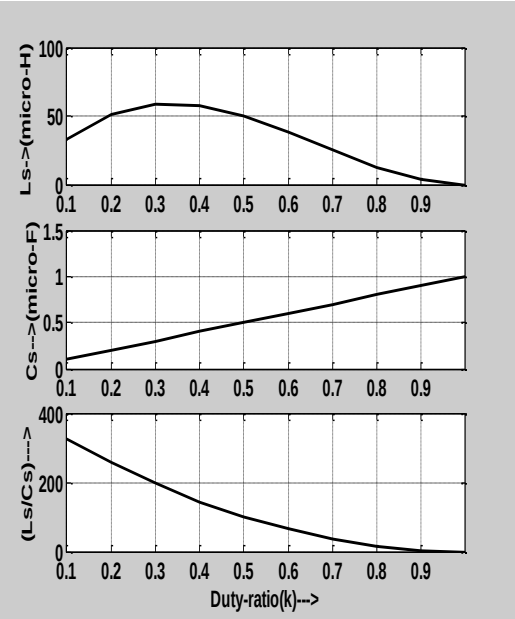

Fig.7. Values of source inductor and load capacitor at different duty-ratio(k) of switch

The efficiency of this converter at different duty-ratios is given in following Table-II.

This table indicates that the efficiency is significantly higher at low duty-ratio and decreases with increase in duty-ratio.

Table-II

Duty_ratio(k)	Efficiency(η) %	Load voltage
0.1	96.82	55
0.2	95.79	65
0.3	94.75	77
0.4	93.9	92
0.5	93.22	106
0.6	92.56	120 (Verge of continuous conduction)

V. CONCLUSION

The proposed topology is simulated by the help of MATLAB/ Simulink. At a fixed value of frequency, duty-ratio(k) and load, the source inductor, snubber capacitor and boost capacitor are designed based upon situation that the source current is on verge of discontinuous from continuous mode of operation. Main intention of making this is to operate switch on under zero-current switching. Simultaneously the discharging current of snubber capacitor becomes initially very small due to small value terminal and contact lead inductance, because their effect at high frequency cannot be neglected. With prevailing parameter, the power loss by snubber capacitor during switching on is approximately 3 watt which is dissipated through snubber resistor. During turn-off, the device is operated at zero-voltage (i.e., at forward-biased voltage/cut-in voltage of snubber diode that appears across the device). So it is treated ZVS off. The efficiency of the topology is higher at low-duty-ratio and reduces with increase in duty-ratio. This decrease in efficiency at higher duty ratio (i.e., above k>0.6) , because the requirement of snubber capacitor is increasing due to excessive increase in input peak current and increase in conduction losses as output voltage is more causing excess load current. The limitation of the circuit is that circuit is operated at significant ripple input current. The output ripple voltage on load side is the lowest. As the duty-ratio approaches to 0.6 with prevailing designed parameters, the source current tends to continuous conduction from discontinuous operation. Between 0<k<0.6, the source current remain discontinuous without changing parameters of the circuit. Beyond this value, the current remains continuous and dc value increases and input ripple decreases. In order to avoid such problem and to keep the loss within control, the ratio of voltage to current at source is required to maintain more than 1 and simultaneously the values of inductors and capacitors need to be updated. From the table, it is concluded that the efficiency is significantly higher (i.e., 96.82% lower duty-ratio k=0.1), but gradually decreases as the duty-ratio increases and remain above 90% (i.e., for k<0.6). This topology is simple as it does not need extra switch, but the optimisation of components after through designing process leads to enhancement of efficiency.

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