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Implementation of Energy Efficient gates using Adiabatic Logic for Low Power Applications

A.Anitha

Abstract: ***In today's electronic sector, low energy has appeared as a major feature. Power effectiveness is one of the most significant characteristics of contemporary, high-speed and mobile digital devices. Different methods are available to decrease energy dissipation at distinct stages of the planning method and have been applied. As the transistors count per device region continues to rise, while the switching energy does not rise at the same pace, power dissipation increases, and heat removal becomes more hard and costly. The power consumption of electronic appliances can be decreased by using various logic types. For such low-power electronic applications, adiabatic logic mode is very appealing.***

Using adiabatic logic, distinct power-efficient gates are intended in this document and contrasted for energy dissipation, propagation delay and no of the transistors used. In addition, the circuit developer can use these gates in the combinational and sequential circuits to develop low-power systems. The simulations of these gates are carried out in 90 nm technology using cadence virtuoso instrument.

Keywords: Adiabatic Logic, CMOS Logic, Efficient charge recovery logic (ECRL), Positive Feedback Logic (PAL), 2N2N2P logic.

I. INTRODUCTION

The power sources in CMOS circuits are dynamic power and standby power. The following equations 1 to 4 define the power within the device

$$P_{total} = P_{dynamic} + P_{short} + P_{leakage} \quad (1)$$

$$P_{dynamic} = \alpha * C * V_{dd}^2 * f \quad (2)$$

$$P_{short} = \alpha(\beta/2)\,(V-2V_{th})^3 * f * T_{rf} \quad (3)$$

$$P_{leakage} = (I_{diode} + I_{subthreshold}) * V_{dd} \quad (4)$$

α = Activity Factor, C = Load Capacitance, V_{dd}=DC Voltage, *f* =Frequency of the clock, β= Gain Factor, T_{rf} = Rise/Fall Time (gate inputs), V_{th} = Threshold Voltage.

Dynamic energy is the device's power consumption when constantly switching from one state to another. It has changing energy owing to loading and discharging, and Short circuit power is due to the current flowing from higher potential to lower potential, when both PMOS and NMOS transistors are ON during their transformation from ON to OFF and OFF to ON. Leakage energy is linked to diode leakage conditions, gate SiO2 leakage processes and sub threshold leakage.

Static energy is produced when the unit is both standby mode and functional mode, the primary problem is usually with leakage energy while the unit is idle.

This energy should be more focused in the device's deep submicron design as it relies exponentially on the device's magnitude. Sub-threshold leakage flow in deep submicron technology and is difficult to handle as it rises as the threshold voltage of the transistor decreases [1][2].

II. PRINCIPLES OF CONVENTIONAL LOGIC AND ADIABATIC LOGIC APPROACH

A. Conventional CMOS Logic

Fig1.Shows the standard CMOS logic which has the steady state power supply. The energy that the power system uses is CV^2_{dd}. When the output of the circuit is high, Load capacitor is charged through the PMOS network and energy of ($^1/_2$ *CV^2_{dd}) is consumed and the other part of the energy is dissipated in the PMOS network. When the output node is low, the energy stored in the capacitor ($^1/_2$*CV^2_{dd}) is discharged to ground through the NMOS network. Transistor sizes could be reduced, or the supply voltage can also be reduced, or the activity factor can be minimized to reduce power consumption.

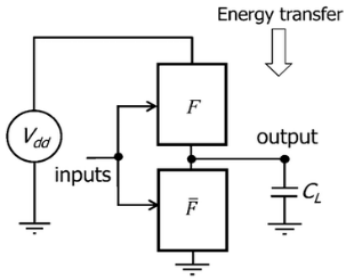

Fig. 1. Conventional CMOS switching

B. Adiabatic Switching

Compared to the standard CMOS design style, adiabatic logic has less energy consumption. The word adiabatic originates from 'thermodynamics', cast-off define a system where the atmosphere does not swap energy. For small energy dissipation, the adiabatic tuning method can be accomplished. Adiabatic_logic provides a system to recycle the "energy" stored in the capacitors, somewhat rather than the conventional manner to discharge the power toward the lower potential & waste it.

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Adiabatic_logic circuit is as shown in fig.2 Let R be the resistance of PMOS network. Here the device RC's time constant is lesser than the time period T of the voltage, i.e. RC<<T. Therefore the "voltage" across the capacitor slowly increases and follow the supply voltage, resulting in a potential difference very close to zero across PMOS transistor. The 'voltage' across the load is also a ramp with the slope of V / T, where V is the swing of the voltage and T is the clock period.

The adiabatic circuit charging current can be calculated using ic= C (dVc / dt) = CV / T. And the energy dissipated in the PMOS can be examined using calculation $E= ic^2RT= (CV/T)^2RT = (RC/T) CV^2$.

The equivalent circuit for discharging is similar to that of the charging except that the supply voltage ramps down. As RC << T, Then E= "(RC / T) CV 2<<<1/2 CV 2 as RC<<<T". It implies that the energy produced in the capacitor is more than wasted during loading or discharging by the resistor. This shows that some energy deposited in the load is effectively transferred to the source of energy [3][4] during discharge.

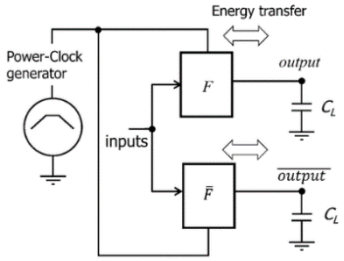

Fig. 2. Adiabatic Switching

III. "Adiabatic Logic" Techniques

There are different adiabatic techniques in the literature [5]

In "Efficient Charge Recovery Logic (ECRL)" Logic, a pair of pull_down NMOS network and pull_up PMOS network forms the logic in ECRL. Both pre-charge and assessment(evaluation) are conducted concurrently in this technique. It removes diodes use and thus has less energy dissipation. It consumes more energy than adiabatic circuits 2N2N2D [6]. It has less output swing, so it is not appropriate for low power applications. It has weak zero logic due to the threshold voltage of P-MOS. Therefore, the ECRL ckt has less noise_margin. Figure 3 shows the ECRL adiabatic logic overall block diagram with dual rail.

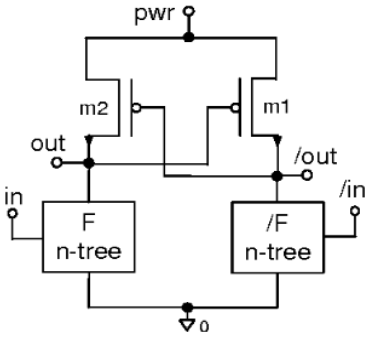

Fig. 3. ECRL Adiabatic Logic

PFAL is one of the methods of adiabatic logic that is robust against parametric changes. It's a dual track system as well. This offers strong noise immunity because there is no degradation of the logic. It is evident from figure 4 that there is a latch of two NMOS and two PMOS transistors that prohibits the input points from being logically degraded. Using this logic, different logic gates can be introduced. PFAL is one of the finest adiabatic logic for reducing CMOS circuit power consumption. The logic frames used to implement the tasks form a simultaneous mix with PMOS, forming a gate of transmission [7].

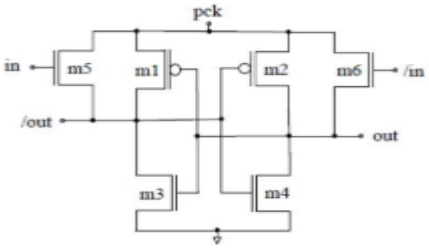

Fig. 4. PFAL Adiabatic Logic

In the attempt to minimize the pairing impact, the 2N2N2P class also refers to the adiabatic logic family extracted from ECRL. Figure 5 shows the 2N-2N2P logic schematics. Its primary benefit over ECRL is the cross-coupling of the NMOS transistor, which contributes to non-floating inputs for most of the retrieval stage, reducing the crosstalk issue and helping to restore the level of logic. In relation to the "cross-coupled" P-MOS transistors prevalent to both classes, the distinction between ECRL logic and 2N2N2P is with the pair of cross coupled NMOS transistors in addition to the cross coupled PMOS transistors common to both the families [8].

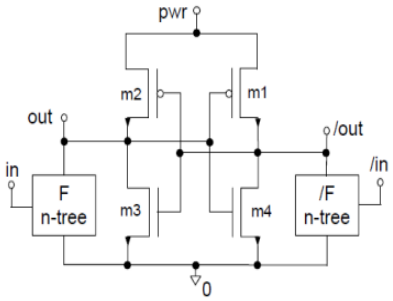

Fig. 5.2N2N2P Adiabatic Logic

IV. IMPLEMENTATION OF LOGIC GATES

All the gates are simulated with the V_{pulse} of 1V, 320ns time, 160ns pulse period, 40ns rise time and 40ns fall time utilizing 90 nm technology cadence instruments. Figures 6 to 29 show NOT, NAND, NOR Gates and their input and output waveforms using standard CMOS logic and adiabatic logic utilizing ECRL, PFAL, 2N2N2P [9].

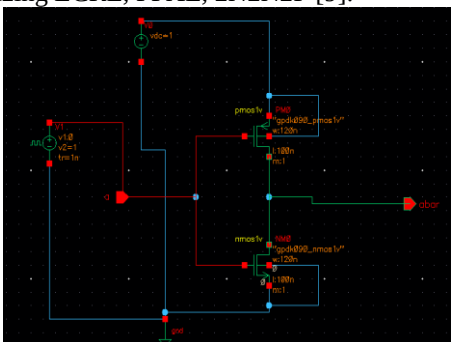

Fig. 6. Schematic diagram of CMOS NOT gate

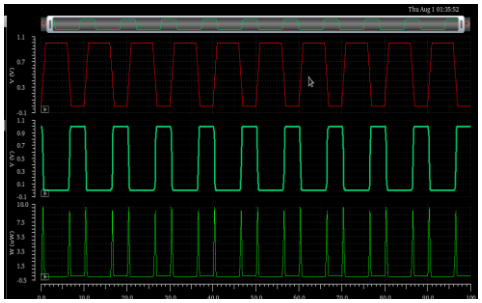

Fig. 7. Simulation results of CMOS NOT gate

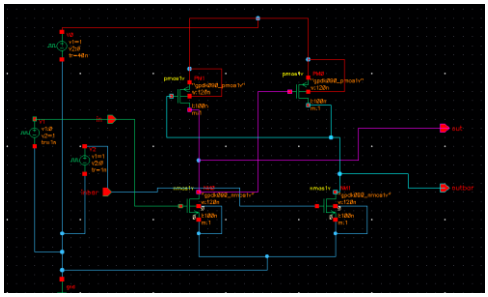

Fig. 8. Schematic diagram of ECRL NOT gate

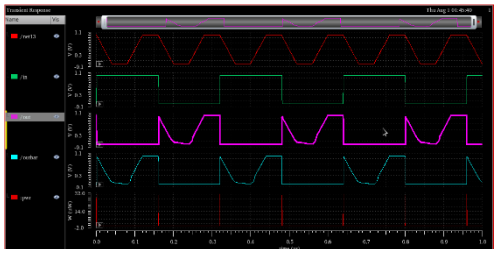

Fig. 9. Simulation diagram of ECRL NOT gate

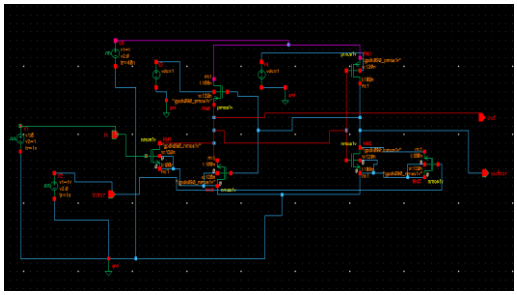

Fig. 10. Schematic diagram of 2N2N2P NOT gate

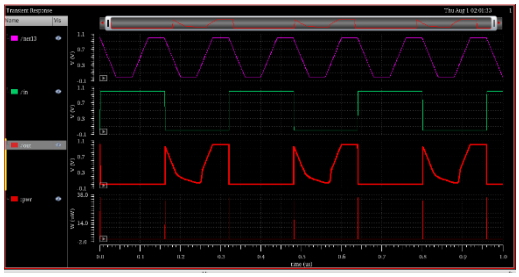

Fig. 11. Simulation results of 2N2N2P NOT gate

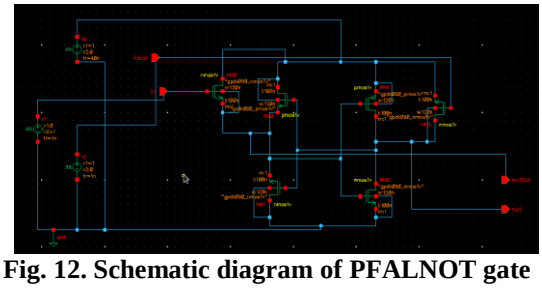

Fig. 12. Schematic diagram of PFALNOT gate

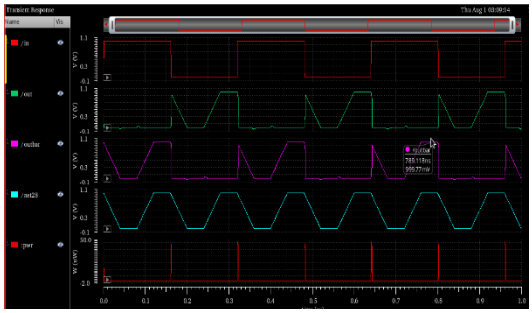

Fig. 13. Simulation diagram of PFAL NOT gate

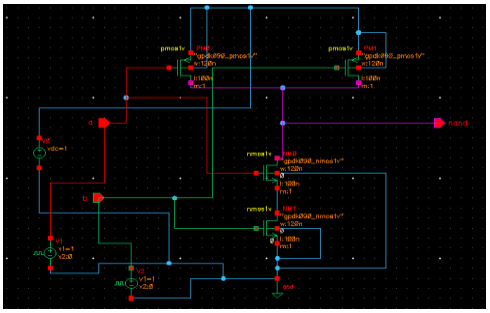

Fig. 14. Schematic diagram of CMOS NAND gate

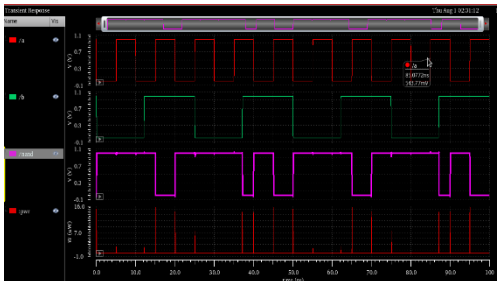

Fig. 15. Simulation diagram of CMOS NAND gate

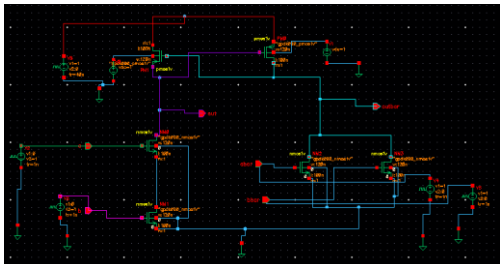

Fig. 16. Schematic diagram of ECRL NAND gate

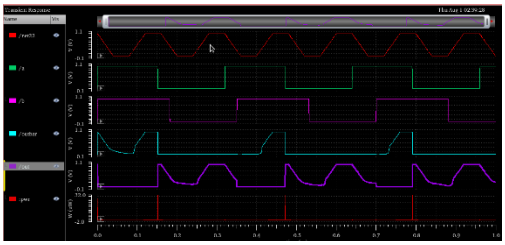

Fig. 17. Simulation diagram of ECRL NAND gate

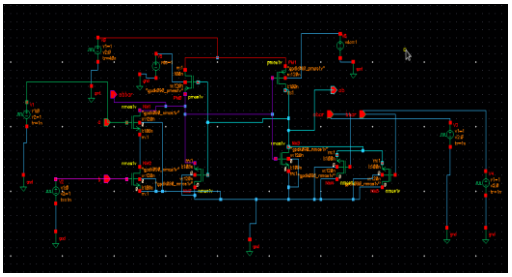

Fig. 18. Schematic diagram of 2N2N2P NAND gate

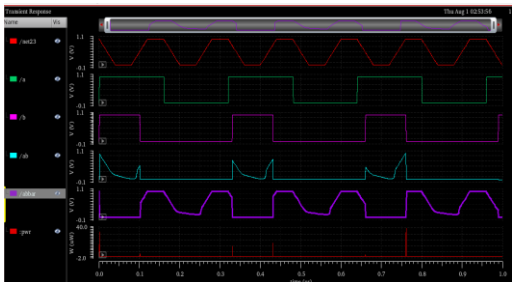

Fig. 19. Simulation diagram of 2N2N2P NAND gate

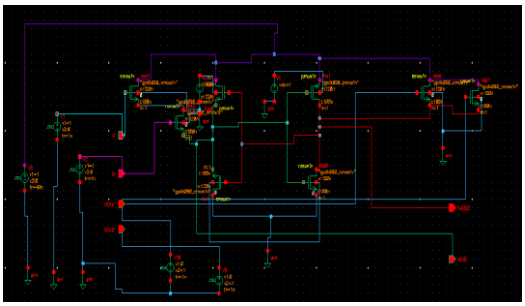

Fig. 20. Schematic diagram of PFAL NAND gate

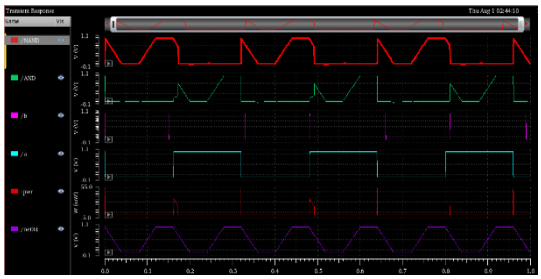

Fig. 21. Simulation diagram of PFAL NAND gate

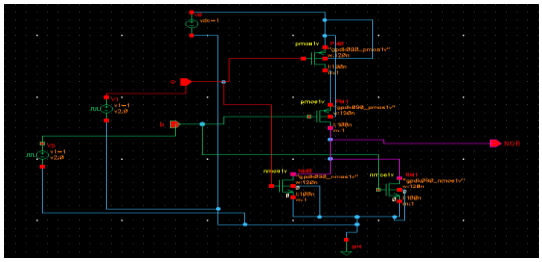

Fig. 22. Schematic diagram of CMOS NOR gate

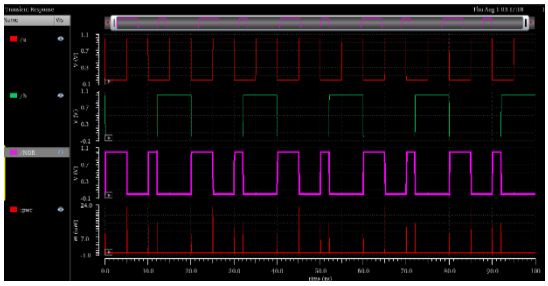

Fig. 23. Simulation diagram of CMOS NOR gate

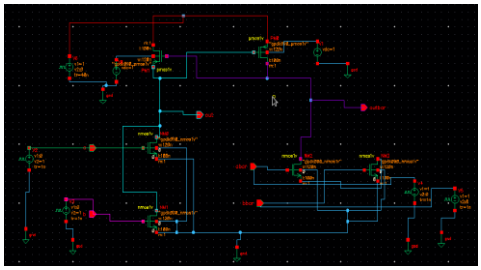

Fig. 24. Schematic diagram of ECRL NOR gate

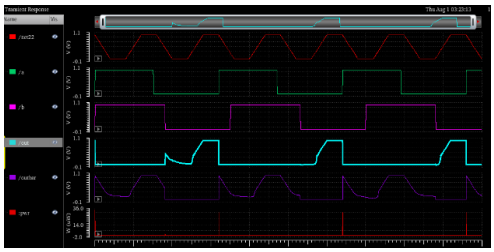

Fig. 25. Simulation diagram of ECRL NOR gate

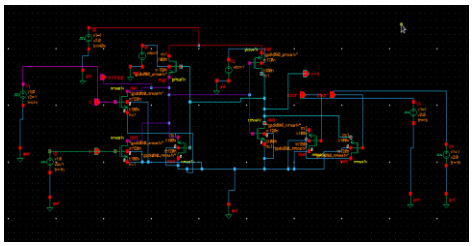

Fig. 26. Schematic diagram of 2N2N2P NOR gate

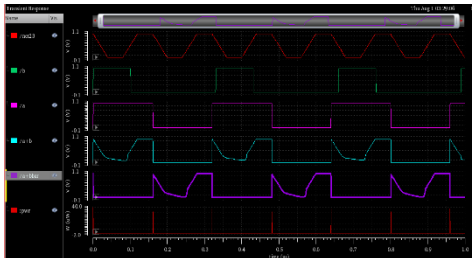

Fig. 27. Simulation results of 2N2N2P NOR gate

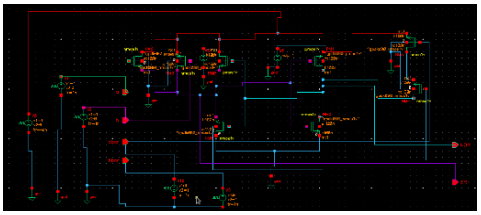

Fig. 28. Schematic diagram of PFAL NOR gate

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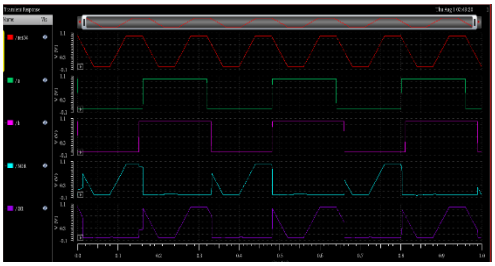

Fig. 29. Simulation diagram of PFAL NOR gate

V. RESULTS

Simulation findings of NOT gate, NAND gate and NOR gate applied using various adiabatic logic styles and CMOS logic are tabulated in the tables 1,2,3 for power, delay and number of transistors utilized. Figures 31 to 33 show the power consumption bar graph depiction.

Table-I: Comparison table of power, delay and no. of transistors used for NOT gate

Logic/ parameter	No of transistors	Power in watts	Delay in sec
CMOS	2	6.08E-07	-85.37E-12
ECRL	4	6.27E-08	91.17E-12
PFAL	6	6.23E-08	162.8E-9
2N2N2P	6	8.00E-08	112.6E-12

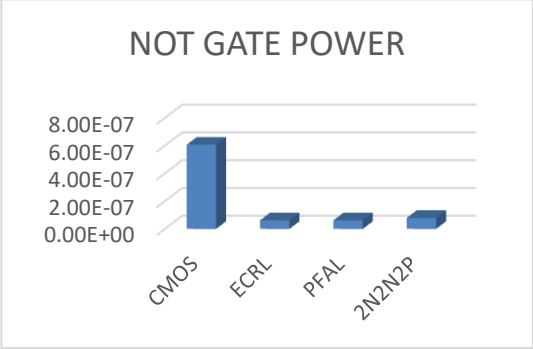

Fig. 30. Bar graph representation of NOT gate power comparison

Table-II: Comparison table of power, delay and no. of transistors used for NAND gate

Logic/ parameter	No of transistors	Power	Delay
CMOS	4	6.62E-08	19.2E-12
ECRL	6	3.98E-08	279.3E-12
PFAL	8	6.50E-08	-469.2E-12
2N2N2P	8	4.38E-08	319.0E-12

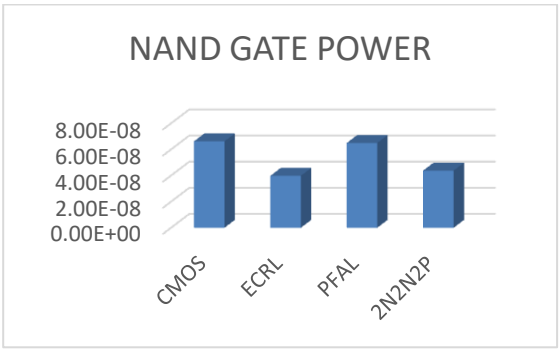

Fig. 31. Bar graph representation of NAND gate power comparison

Table-III: Comparison table of power, delay and no. of transistors used for NOR gate

Logic/ parameter	No of transistors	Power in watts	Delay in sec
CMOS	4	1.06E-07	48.05E-12
ECRL	6	4.04E-08	-44.09E-12
PFAL	8	9.53E-08	11.79E-9
2N2N2P	8	8.20E-08	-31.1E-12

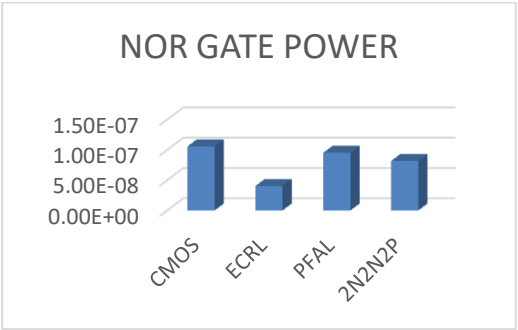

Fig. 32. Bar graph representation of NOR gate power comparison

VI. CONCLUSION

Using adiabatic logic, distinct power-efficient gates are intended in this paper and contrasted for energy dissipation, delay and no of the transistors used. Findings show"s that adiabatic logic will have less dissipation of energy than standard logic of CMOS. Furthermore, in combinational and sequential circuits, the developer could use appropriate gates to develop low energy systems. The simulations of all these gates are carried out in 90 nm technology of cadence virtuoso instruments.

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