International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-3, September 2019

Design and Power Analysis of Vedic Multiplier

S.Kiruthika, P.Sakthi, P.Yuvarani

Abstract*: In this article, displays the capacity of decrease the Power, Area in CMOS VLSI blocks. Power in CMOS circuits is mostly consumed for the duration of the transitions of the gates. Thusly, control estimation of CMOS circuits is changed over into progress action estimation. A few methods are utilized to mimic progress exercises of CMOS circuits. The proposed Vedic multiplier is planned by utilizing various strategies of full adder cells. The structure of full adders for low power is gotten and low power blocks are actualized on the arranged multiplier with the outcomes be broke down used for improved execution. The structures are finished by utilizing TANNER S-EDIT tool and recreated utilizing T-SPICE.

***Keywords* : CMOS, Full Adder, Vedic multiplier, Low power, XOR, XNOR, MUX.**

I. INTRODUCTION

The VLSI means "Very Large Scale Integration". Extremely enormous scale-coordination (VLSI) is characterized as an innovation that permits the development and interconnection of huge numbers (millions) of transistors on a solitary incorporated circuit. Coordinated circuit is an accumulation of at least one entryways created on a solitary silicon chip. The intricacy of VLSI being structured and utilized today makes the manual way to deal with plan unfeasible. Structure robotization is the request of the day with the quick mechanical improvements [5].The VLSI low power structure issue realizes that how will generally be broadly requested into two examinations with improvement.

Analysis issue is troubled concerning the accurate assumption of the power or vitality scattering on a range of period of the plan process. The investigation procedures contrast in their exactness and effectiveness. Examination strategy additionally fills within the same as the beginning for plan streamlining. [3] A requirement for low power VLSI chips emerges from such advancement powers of incorporated circuits. Some different variables that fuel the requirement for low power chips are the expanded market interest for convenient customer hardware controlled by the batteries. Another real interest for low power chip and framework originates from natural concerns. The examination methods contrast in their exactness and productivity.

Manuscript published on 30 September 2019
* Correspondence Author
S.Kiruthika*, Department of Electronics and Instrumentation Engineering, M.Kumarasamy College of Engineering, Karur, India. Email: kiruthikavlsi@gmail.com.
P.Sakthi, Department of Electronics and Instrumentation Engineering, M.Kumarasamy College of Engineering, Karur, India. Email: sakthi.npi@gmail.com.
P.Yuvarani, Department of Electronics and Instrumentation Engineering, M.Kumarasamy College of Engineering, Karur, India Email: yuvaranieie@gmail.com.

II. DESIGN OF FULL ADDERS

A binary full adder is the adder basic to almost all mathematics operation. It is the center module utilized for some, fundamental tasks like multiplication, division and addresses calculation for every memory gets to and it is typically present in the math rationale unit and gliding point units. Henceforth, their speed improvement conveys critical potential for superior applications. Various adder designs can be used depending on the application and low power consumption [3]. In this project, power reductions for signed multipliers are explained and power comparisons of different multipliers are obtained. For power decrease the 10T full adder adjusted with 8T full adder. Be that as it may, the circuits dependent on PTL are surely helpful in structure up greater circuit, used for instance, dissimilar section input adder and multiplier. In this paper, an extraordinary failure power and fast full adder cell utilizing just 8 transistors is exhibited, in particular new 8T full adder. So as to show the proficiency of the new structure, some broad qualities of the new plan, for example, control utilization and deferral, against other various kinds of five full adder cells are performed.

A. XOR Full Adder Design

The Full Adder is an essential unit in every single advanced circuit. A little modify in transistor check, power and postpone will cause a radical change in the presentation of a huge VLSI circuit [6]. The presentation of multipliers relies upon the full adder utilized. The distinctive full adders are utilized to examination. The first is 10T XOR full adder, the planned ten transistor full adder appeared within picture (1) utilizes four transistor XOR appeared within picture (1) gates in their structure. This plan of proposed XOR eight transistor full adders appeared in figure 5.1 depends on three transistor XOR gates, it obtains least silicon territory. The plan of 3T XOR gate is appeared within Figure (2).

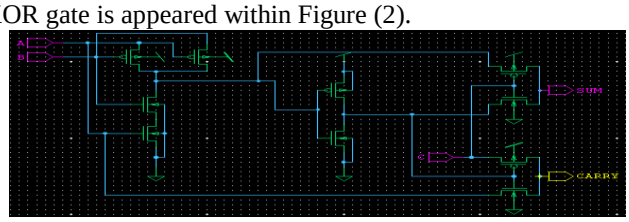

Fig. 1. 10T XOR adder

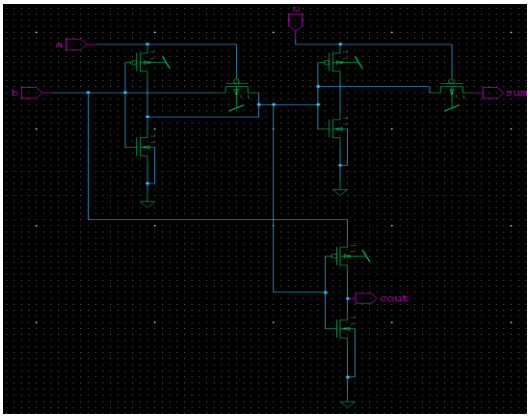

Fig. 2. 8T XOR adder

B. XOR Full Adder Design

The second full adder is the 10T full adder which is having XNOR kind of full adder, this sort of full adder utilizing pass transistor logic (PTL) [9]. This kind of full adder is called static vitality recuperation full adder it having 4T XNOR appeared in figure plan [9]. The disposal of the way in the direction of the position lessens the absolute power utilization through decreasing the small out power utilization.

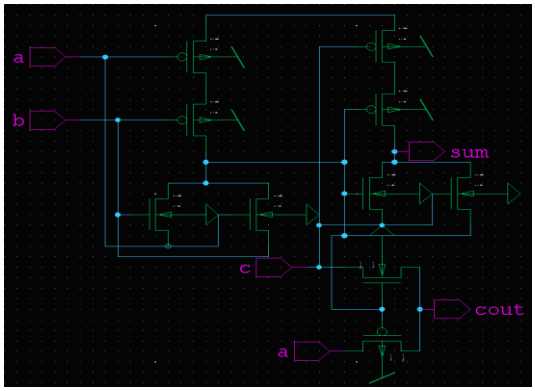

Fig 3. 10T XNOR adder

The static energy recovery full adder appeared in figure comprises of two XNOR with single MUX circuit. The XNOR planned with utilizing four transistors appeared in picture (3). The second proposed plan is XNOR 8T full adder appeared in figure (4) depends on top of 3 transistor XOR gate, it gains smallest amount silicon territory. The plan of 3T XOR gate is appeared within Figure (4).

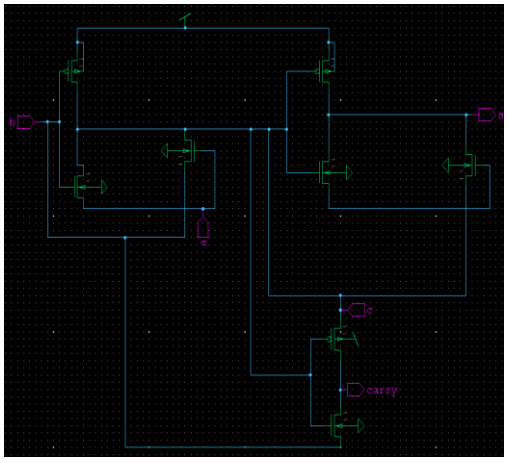

Fig. 4. 8T XOR adder

C. Design of Full Adder using 2:1 MUX

The third kind of full adder is comprises of 2:1 Multiplexer circuit and 2 inverters. The system is to stay away from numerous limit voltage misfortunes in convey chain by legitimate dimension reestablishing. DC and transient examination delineates that the CLRL adder experiences just a single edge voltage misfortune issue with require the base voltage.

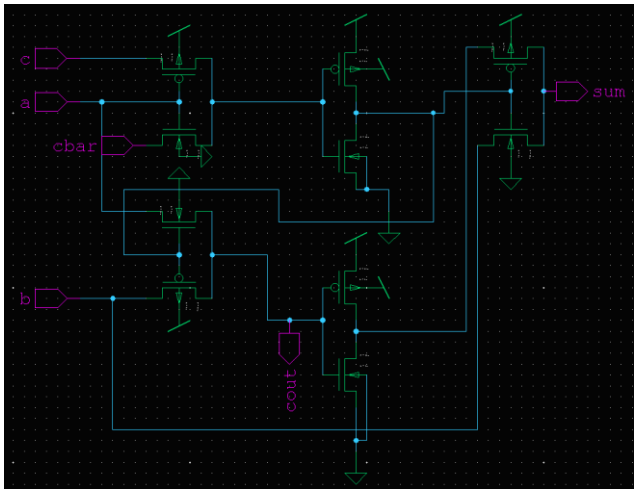

Fig. 5. 10 Transistor adder using 2:1 MUX

The third kind of proposed configuration is Complementary and Level Restoring Carry Logic adder comprises of 2:1 multiplexer circuit and inverter appeared in figure (6). It is having just 8T. The methodology is to maintain a strategic distance from numerous edge voltage misfortunes in convey chain by appropriate dimension reestablishing.

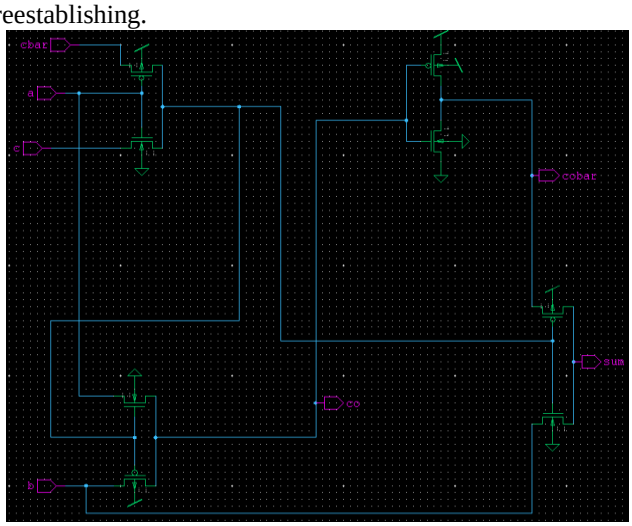

Fig 6. 8T Full adder using 2:1 MUX

D. Shannon Full Adder Design

The control input terminals are associated with the capacity inputs. In the proposed adder 2, from Table I as opposed to giving every one of the contributions from outer information the inner yield from the SUM circuitry acts as input to the carry logic [8]. The full adder is 8T Transistor full adder utilizing pass transistor logic. The arranged structure of Shannon full adder circuit as appeared within picture (8).

The total and convey activity are multiplexing in a signal circuit [11].

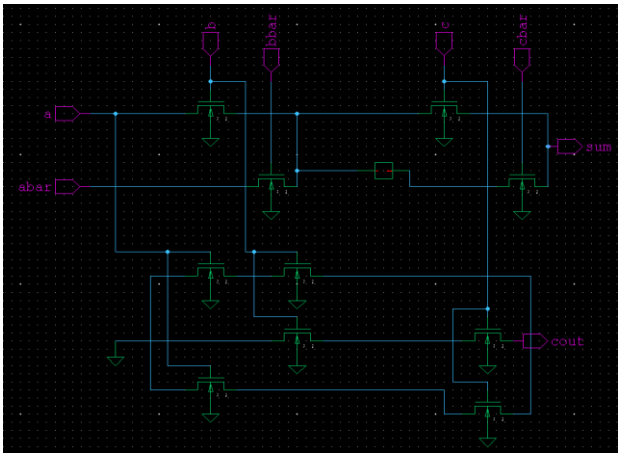

Fig. 7. 12T Shannon full adder

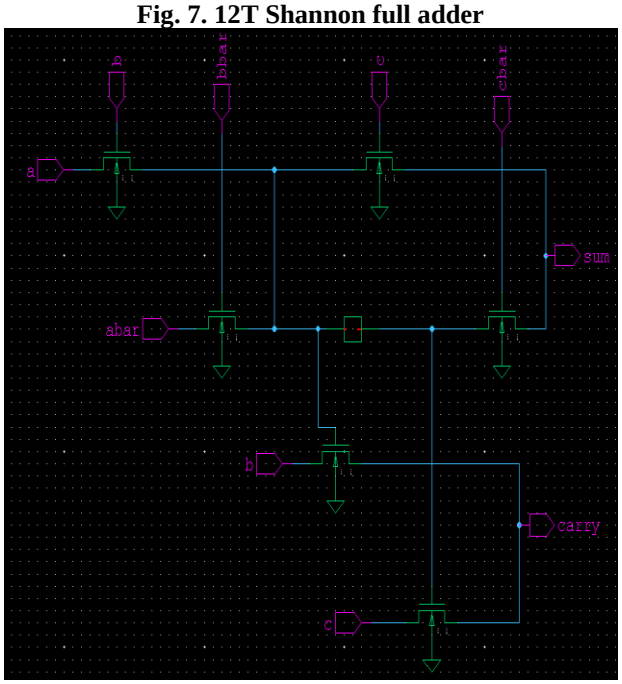

Fig. 8: 8T Shannon full adder

III. FULL ADDER RESULT AND DISCUSSION

The new 8T full adders have best execution contrast with existing sort of full adders. The transistor check and power utilization are diminished look at 10T full adder. The majority of the adders having same sources of input and furthermore gives same out puts. For the full adders Inputs:

A=1001, B=1011, C=0111
Outputs: SUM=0101, CARRY=1011

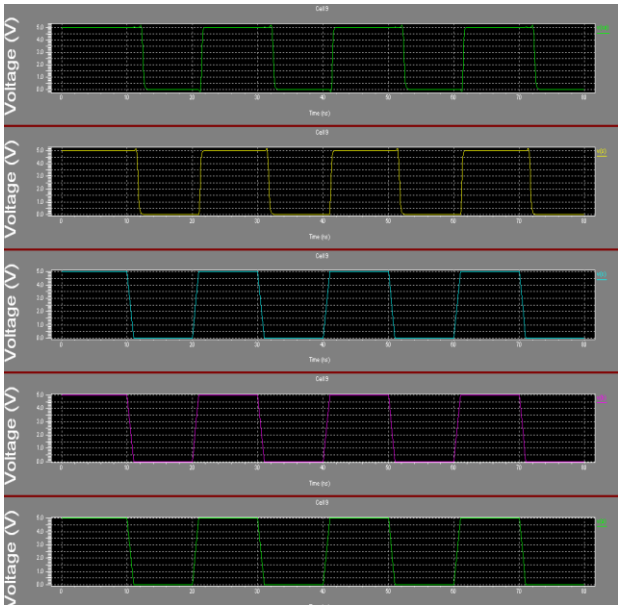

Fig. 9. 12T Full adder output waveform

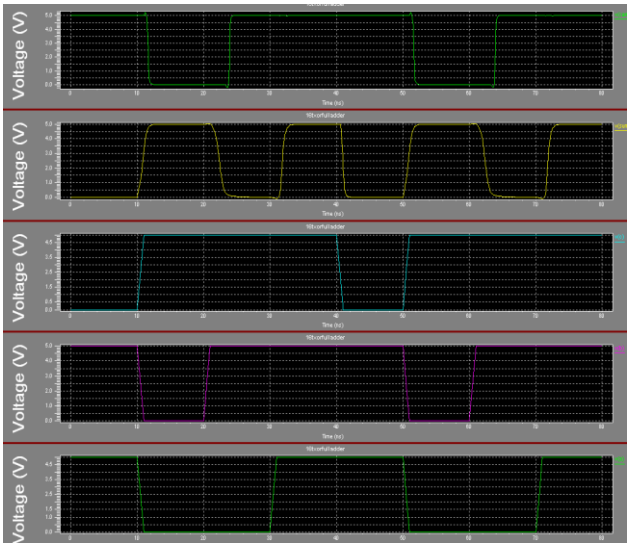

Fig. 10. 10T Full adder output waveform

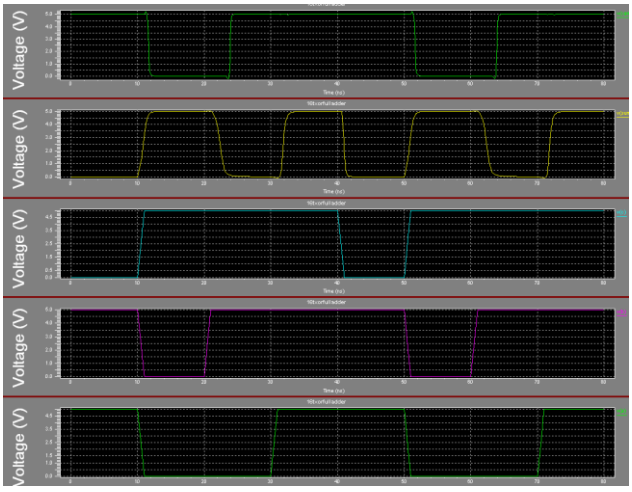

Fig. 11. 8T Full adder output waveform

Table I: Comparisons of Full Adders

Full Adder Type	Power(watts)		Transistor count	
	Existing method	Proposed method	Existing method	Proposed method
XOR	0.146	0.094	10	8
XNOR	0.125	0.082	10	8
CLRCL	0.112	0.071	10	8
SHANNON	0.102	0.058	12	8

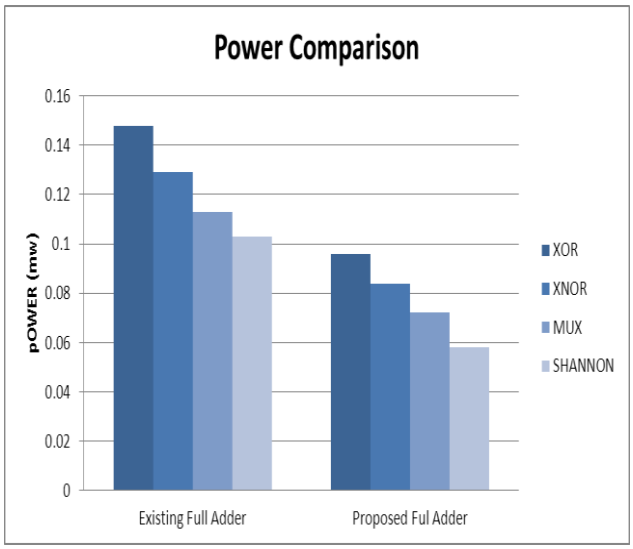

Fig. 12. Power comparison of Full Adders

IV. DESIGN OF VEDIC MULTIPLIER

The regular plan of 4x4 bit Vedic multiplier module is executed utilizing four 2x2 bit Vedic multiplier modules and 10T and 12T full adder module as talked about in figure 13 [2]. The proposed design of 4x4 piece Vedic multiplier module is executed utilizing four 2x2 bit Vedic multiplier modules [1] and 10T and 12T full adder module as discussed about in figure 13.

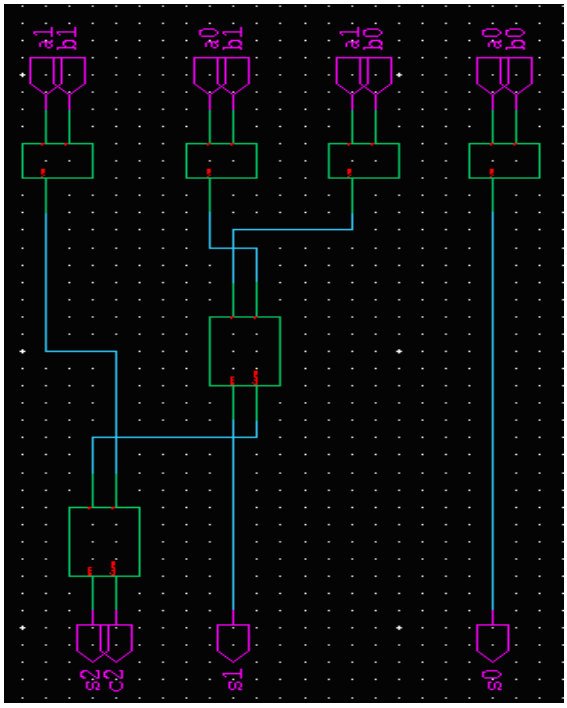

Fig. 13. Conventional Vedic Multiplier (2x2)

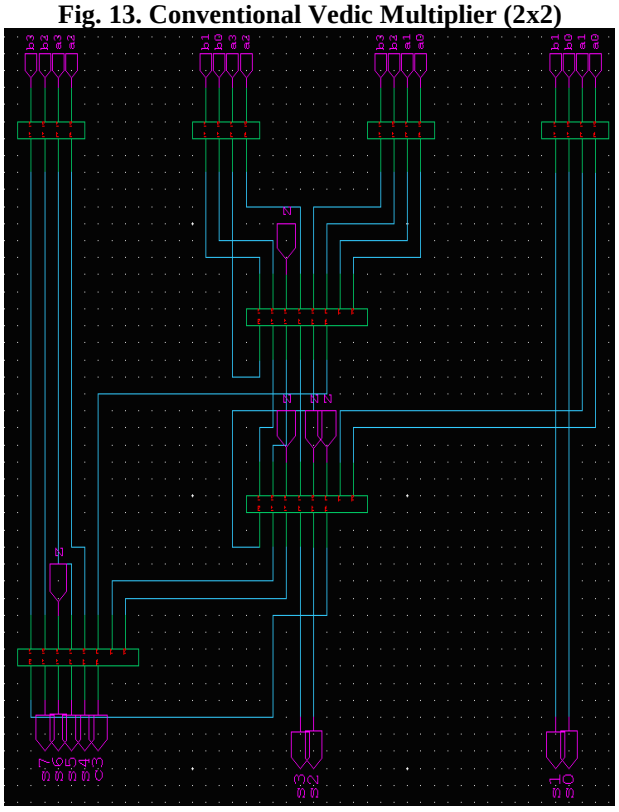

Fig. 14. Conventional Vedic Multiplier (4x4)

The power of different multipliers is analyzed with different adder units. The power comparison of different full adders is done and it is shown in figure. And the power outputs demonstrate to the Shannon full adder is having a smaller amount power utilization than every single other adders [3].

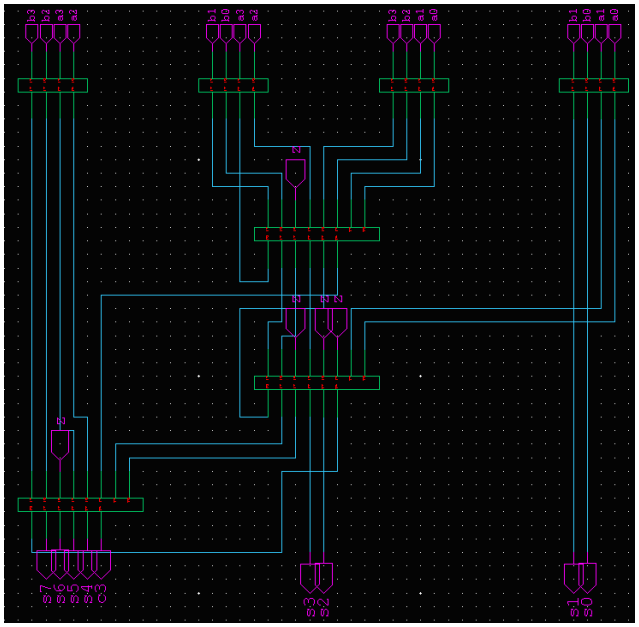

Fig. 15. Proposed Vedic Multiplier (4x4)

The existing and proposed multipliers are designed with different full adders and the power results are obtained and the comparison graph is shown in figure (18). The transistor counts of various unsigned and signed multipliers are different due to the different elements in that. The transistor count results of multipliers are given in table (2)

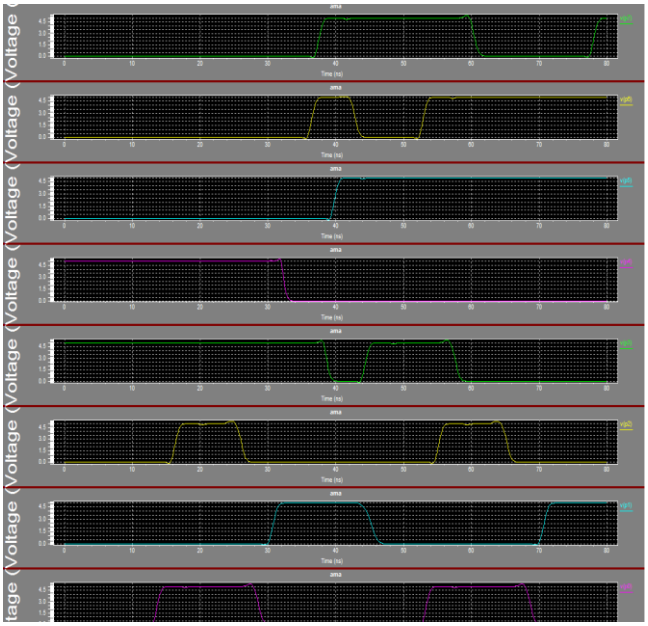

Fig. 16: Conventional Multiplier output waveform

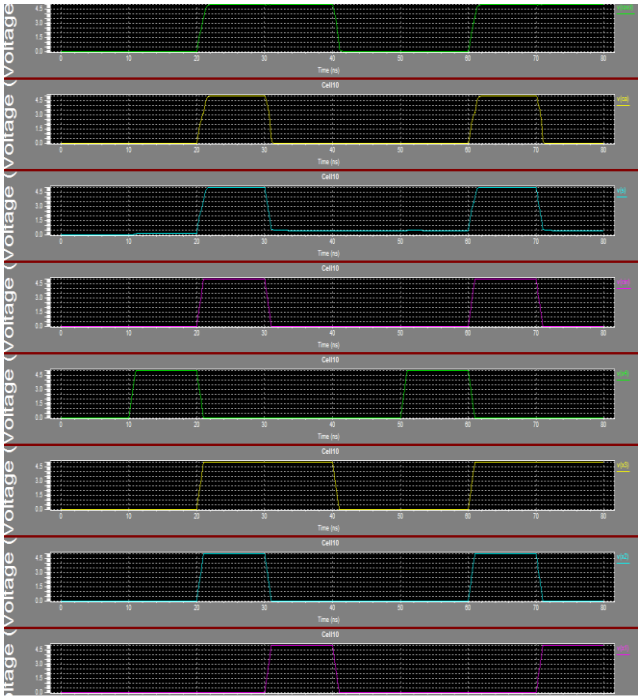

Fig. 17. Proposed Multiplier output waveform

From the above result it is seen that the proposed multiplier with Shannon full adder be observed in the direction of more power productive with furthermore this multiplier is having extremely less transistor count.

Table II: Comparisons of Different Types of Multipliers

Multiplier Type	Adder type	Power (mw)		Transistor count	
		Existing method	Proposed method	Existing method	Proposed method
Vedic multiplier	XOR	10.04	9.08	212	188
	XNOR	9.01	8.12	212	188
	CLRCL	8.25	7.43	212	188
	SHANNON	7.53	6.85	234	188

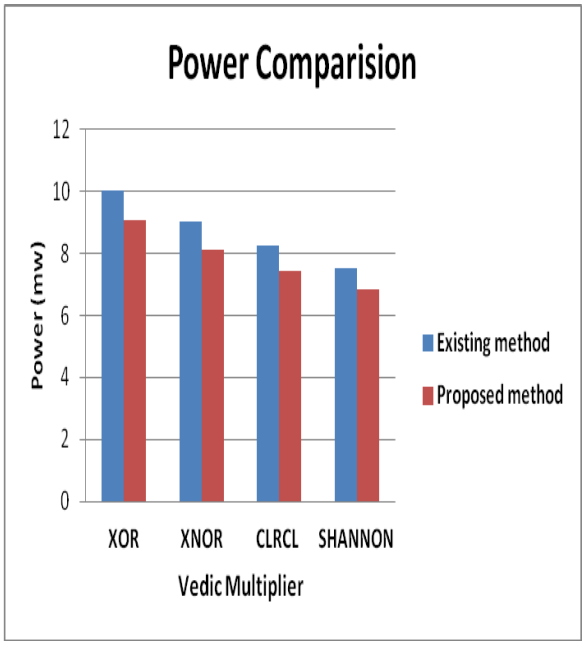

Fig. 18. Power comparison of Multipliers

V. CONCLUSION

The new eight transistor full adder has 30 % power investments as compare with old twelve Transistor Full adders and 36 % control reserve funds when contrasted with 10 TCLRCL adders. The future 8T full have the smallest deferred while contrasted and its companions. Four multipliers have been structured utilizing four distinctive full adders and their exhibition has been analyzed. The multipliers actualized utilizing Proposed8T full viper has least power defer item in every one of the cases Proposed multipliers with the CMOS full adder have 8.6% power reduction in transistor count and about 10.4% power reduction than the existing multipliers with CMOS full adder. Multipliers with 10T full adder have 13.12% transistor count 17.4% power reduction in the proposed than the existing. Finally the proposed multipliers with 8T have 17.9% reduction in transistor count and 8.6% power reduction than the existing multipliers.

REFERENCES

1. P.Sakthi,S.Maheswari, P.Yuvarani, "High Performance Vedic Multiplier using Compressors", International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.20 (2015),pages 16882-16886.
2. P.Sakthi, P.Yuvarani," Multipliers based on Urdhva Tiryagbhyam Algorithm: A Survey",Advances in Natural and Applied Sciences, ISSN:1995-0772, 8(19) Special 2014, Pages: 100-106.
3. S. Kiruthika, R.Nirmal Kumar, Dr. S.Valarmathy, Issue 1, January 2013,"Comparative Analysis of 4bit Multipliers Using Low power 8-Transistor Full Adder cells" International Journal of Emerging Technology and Advanced Engineering (IJETAE) Volume 3, ISSN 2250–2459, ISO 9001:2008.
4. Siddharth S.G, Ramkumar M, Kiruthika.S, 2014, "Railway Track Scanning and Surveillance Robot Using Wireless Technology" Journal of Harmonized Research in Engineering (JOHR) Volume 2, Issue 1, 2014, (pp194-200).
5. S.Kiruthika, A.Vimala Starbino, "Design and analysis of FIR filters using low power multiplier and full adder cells", IEEE 2017.
6. S.Kiruthika, B.Balraj, "Design of Wallace tree multiplier based on 0.12µm CMOS technology using GDI full adder".2018, International Journal of pure and applied mathematics Volume 119, Special Issue.
7. J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," IEEE J.Solid-State Circuits, vol.29, no. 7, pp. 780–786, Jul. 1994.
8. Karunakaran P, S. Venkatraman, I.Hameem Shanavas, and T. Kapilachander. "Power Optimized Multiplier Using Shannon Based Multiplexing Logic", International Journal of Intelligent Systems and Applications, 2012.
9. Deepa, Sampath KumarV, "Analysis of Low Power 1-bit Adder Cells Using Different XORXNOR Gates", 2015 IEEE International Conference on Computational Intelligence & Communication Technology, 2015.
10. "Neuronal Logic gates realization using Vedic mathematics" , 2015 1st International Conference on Next Generation Computing Technologies (NGCT), 2015
11. P. Yuvarani, 2012, 'Image denoising and enhancement for lung cancer detection using soft computing technique,' IET Chennai 3rd International on Sustainable Energy and Intelligent Systems (SEISCON 2012), pp. 1-4.